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April 2016

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Feature Content

Design Engineers and PCB Designers

Some PCB designers say that working with their design engineers is one of their biggest hurdles. Others say it all comes down to a lack of communication. We asked a variety of engineers and designers to discuss the reasons for this divide, and what can be done to address this problem. This month we have feature articles by design instructor Rick Hartley and Analog Home's Steve Hageman, as well as interviews with lead designer Andy Critcher of Total Board Solutions and Randy Faucette, director of engineering at Better Boards Inc.

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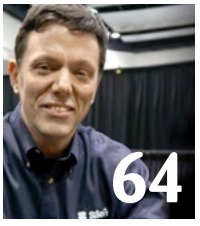

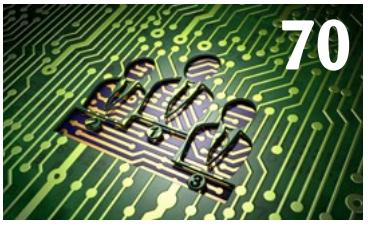

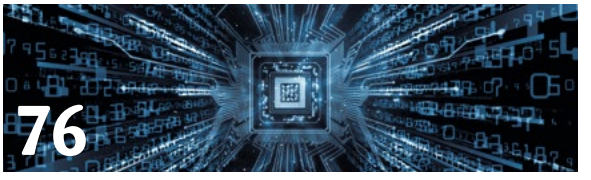

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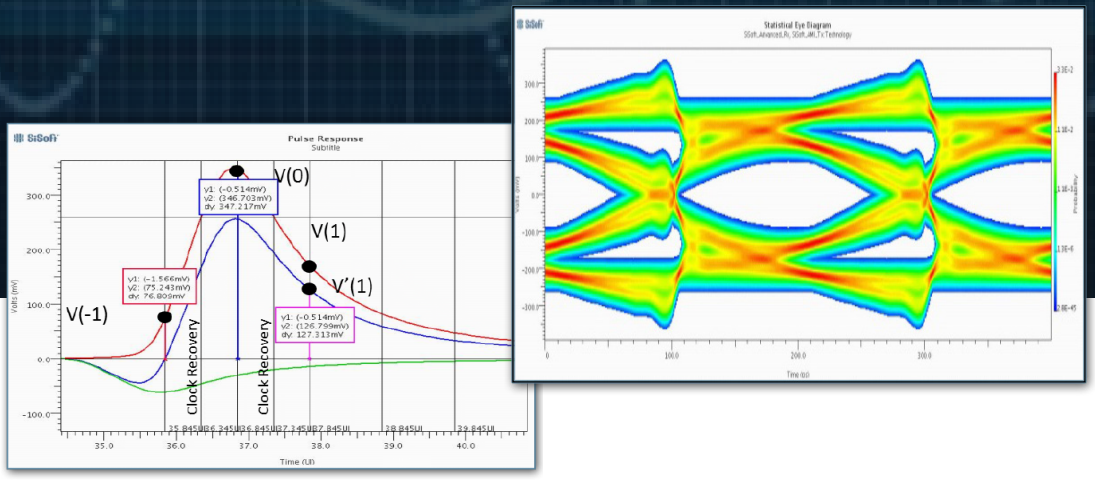

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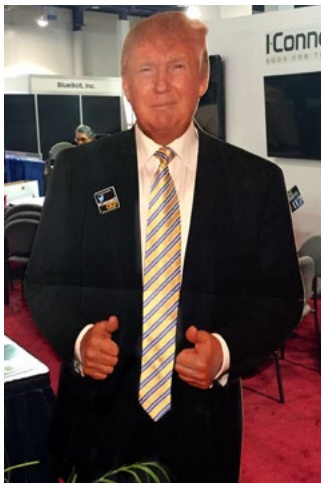


by Andy Shaughnessy
I-CONNECT007

Every show is different, but IPC APEX EXPO 2016 has to be the best trade show I've ever attended. There was just no downside, at least for I-Connect007.

We covered the show from beginning to end, made a lot of new friends, and basically "spread the love," as I like to say.

Our booth was THE place to be on the show floor. Every day, the industry's top technologists and authors could be found in our booth—conducting interviews, being interviewed, or just hanging out and talking about the show.

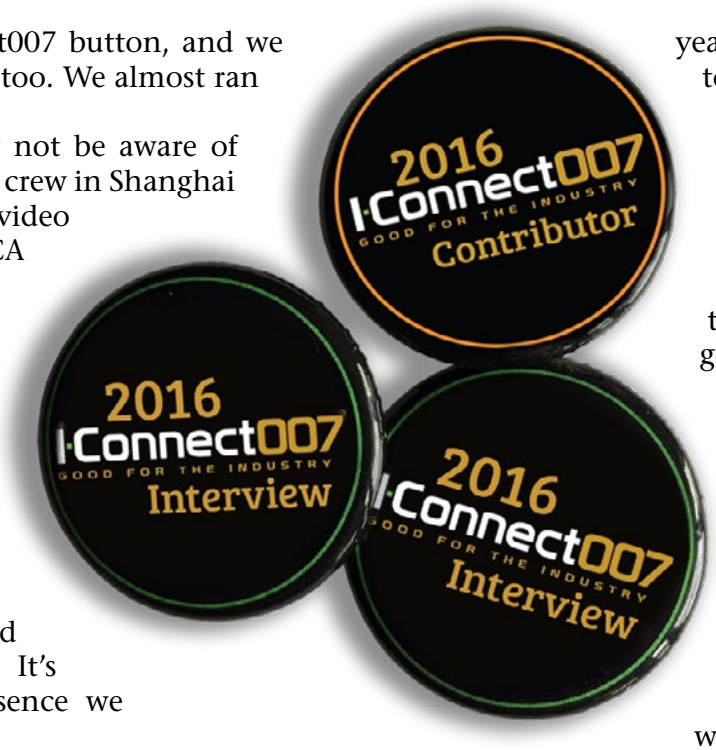
Our booth stayed packed with industry movers and shakers, in spite of our location at the rear of the venue, where the booth numbers were out of order. It helped that we had Donald Trump's cutout standing near the aisle, giving passersby the twin thumbs up. Donald was an unofficial partner of ours; he had people wanting to pose with him, either shaking his hand, or, in Joe Fjelstad's case, attempting to strangle him. We had to keep an eye on Donald. Last year at APEX in San Diego, someone adopted our "World's Most Interesting Man" cutout, and we didn't want Trump to wind up in the trunk of someone's rental car, out in the desert.

Before the show opened, our IT guys successfully conquered the challenges they faced to power the three flat-screen wall monitors that featured our articles, photos, and customers' logos in rotation. The monitors were visible from halfway across the venue, which served us well because our booth was in the back of the venue near the loading dock. Our customers got a kick out of seeing their logos pop up on the screens.

And like a good touring band, we handed out merchandise. Every interviewer and interviewee

received an I-Connect007 button, and we gave out 007 stickers, too. We almost ran out of "merch."

Some of you may not be aware of this, but we also had a crew in Shanghai providing Real Time video coverage of the CPCA Show, which was somehow scheduled the same week as IPC APEX EXPO. There are 52 weeks to choose from. How on earth did those big industry shows end up in the same week? Our production crew worked overtime that week! It's hard to top the presence we have at a show.



On the conference side, the Design Forum was a big hit. Keynote speaker Dale Parker of Google X gave an awesome presentation that focused on Google's driverless cars and other just plain cool stuff. He stressed that Google X won't take on a project unless they believe that it can achieve a 10x increase in productivity, compared to most companies that are excited to see a 10% increase for any project. Parker, a former PCB designer at Shure, then called on the PCB design tool vendors to throw out all of their 1990s-era code and redesign their software from the ground up.

And as Parker pointed out, the EDA companies will eventually have to build artificial intelligence into their flows if they want to truly increase their tools' performance. Would you like to see AI in your favorite design tool? The tool vendors I spoke with were noncommittal when I asked if they'd be scrapping their existing code soon, or introducing AI. Some designers would say there's already too much AI built into their tools.

It was a busy but fun week. And to top it off, our own Patty Goldman, managing editor of *The PCB Magazine,* was inducted into the IPC Hall of Fame. Congratulations, Patty!

Next year, we're back to San Diego for IPC APEX EXPO. It's going to be hard to top this year's event, but it's hard to have a bad time in San Diego.

Of Designers and Engineers

When we survey our readers and ask them to name their biggest challenges, PCB designers sometimes name their design engineers as the main culprits. It happens often enough that it got us thinking. Why is there a split between some PCB designers and their design engineering coworkers? Some designers and EEs blame it on a simple lack of communication. And more engineers are performing PCB design and layout now. Some designers see them as angling to take over their jobs.

So we asked some engineers and designers to discuss the reasons for the divide, and what can be done to address this problem. This month we have a variety of feature articles, including a cover story by design instructor Rick Hartley, a man who's been known to tell it like it is. We also have a feature by Analog Home's Steve Hageman, as well as interviews with lead designer Andy Critcher of Total Board Solutions and Randy Faucette, director of engineering at Better Boards Inc.

This was one of the most interesting topics we've had lately. Is there a schism between your company's designers and design engineers? Read on, and please let me know what you think! **PCBDESIGN**

Andy Shaughnessy is managing editor of *The PCB Design Magazine.* He has been covering PCB design for 16 years. He can be reached by clicking here.

Working with Circuit Design Engineers

by Rick Hartley
RHARTLEY ENTERPRISES

The PCB Design Magazine and PCBDesign007.com receive a lot of feedback from reader surveys. One frequent comment from both PC board designers and circuit engineers involves the frustration of working with each other. Also, a question often asked is, "Are EEs taking over PC board design?"

In 1965, with a two-year college degree, I began life in electronics as an R&D technician. Over a few years I became a circuit designer (EE). Several years later I took another fork in the road, moving into PC board design and layout, making the assumption that, "Being an EE, surely I would be a better board designer than most." Yeah, right!

I quickly learned that PC board design in the 1970s was less a matter of engineering and more a matter of art. Clearly there was science involved but that science was much more about mechanics and manufacturability of bare boards and assemblies than about electronics. People who understood the value of copper balance, pad-to-hole ratio, hole-to-board thickness ratio, how component placement impacted assembly and repair, knowledge of thermal transfer, etc. made better board designers than those with knowledge of only circuit theory. Those who had good analytical ability truly had the ultimate tool needed for board design. But knowledge of electronics, who cared? My education and background meant very little; I was learning everything from scratch.

Is this still true today? We will attempt to answer that question. Why did EE knowledge play such a small role back then? Circuits in those days, with the exception of the RF world, were so low in frequency that board traces had to be several yards long before they were a distributed length, capable of impacting performance. You could, by today's standards, make every mistake under the sun, even in very large boards, and there was a good likelihood the circuit would work anyway. This was not always true, but it

was true most of the time. My electronics background occasionally offered some advantage, but those occasions were rare.

The Seeds of Friction

From the 1950s to the late 1980s, our board design methods were severely bending the laws of physics, teetering on the edge of disaster! A lot of today's grey-haired designers cut their teeth on the layouts of that period and got used to working without input from engineers. Many of those PC board designers were converted technicians, mechanical designers, and artists who learned to read a schematic and mastered artwork taping. EEs would often give their thoughts on what should be done, but you could listen to them or ignore them and the circuit would likely function either way. This era created some tension between board designers and their EE counterparts, mostly because they completely ignored each other's ideas.

"This era created some tension between board designers and their EE counterparts, mostly because they completely ignored each other's ideas."

In the early 1990s, industry as a whole started to see circuits that did not always function as intended or had EMI problems. By the late 1990s, this bad behavior had increased dramatically. It did not take long before we realized that poor board layout was the culprit. The layout practices we used for decades were no longer acceptable in many designs. We had gone from bending the laws of physics to violently breaking them. Why? ICs were getting much faster, due to output rise and fall time getting much shorter. Because of faster outputs, normal line lengths, regardless of clock frequency, were more likely to cause ringing, crosstalk, noise, increased EMI, etc.

During this period many of the PC board designers who possessed little knowledge of electronics grew to rely on circuit engineers to help guide component placement, since many EEs better understood which ICs and circuits were likely to cause problems. This, and the use of multilayer boards, reduced the problem for quite a few years, which gave the perception that "knowledge of circuit theory made a better board designer." Though things were better during this period, I was involved in many designs that failed EMI testing, even though the company circuit engineers and I reviewed and approved the layouts. Though circuit knowledge helped us, it was not enough to stop the problems. Clearly we were missing something important!

IC outputs today are so fast that the problem has become an epidemic. Almost all ICs in production have rise times and fall times well under 1.0 nanosecond, mostly in the range of 300–700 picoseconds. This reality makes any transmission line (trace and its return path) longer than 0.5" to 1.0" (13 to 25 mm) a potential problem. In short, everything is high-speed, capable of causing SI, noise or EMI problems. All this simply means that every PC board of today has to be laid out to satisfy the laws of physics.

What does this have to do with PC board designers and engineers working together? Both groups know there is a real possibility that each design could have problems caused by board layout. Many engineers believe their knowledge of circuit theory is the solution. Many board designers believe the information gained from IC app notes or eval circuits offer a solution. The fact that the two groups disagree says, "At least one party is wrong." My consulting experience has shown that, much of the time, both parties are wrong.

One assumption is often made by both groups: "XYZ layout practice has always worked, so it must be right!" Well, the layouts we did in the '70s and '80s worked but they were far from right. Many circuits work but fail EMI testing, or they work initially but stop working a few years later, after ICs with faster outputs are released. These issues and many others show that the layout did not properly satisfy the laws of physics in the first place. Never use past practice as proof that some method is correct!

It's Hard Out Here for an EE

There is one thing that frustrates many circuit engineers: They are usually held responsible for the entire success of a system. Even though they do not do the packaging design or the board layout, they are held liable when hardware-related problems occur that are caused by those design features. EMI is almost always the result of a physical entity causing resonance and radiation, yet circuit engineers are often not allowed to control these physical items. They want to put in their two cents' worth, and rightly so. Most board designers understand that, but they believe, "If you are going to put in your two cents, make sure you actually know what you are talking about." It is OK to be heard, but it's not OK to tell the board designer to do this or that when you really do not understand the problem. Far too many engineers do not understand the cause of the problems that designers see every day.

This goes for board designers as well. If you are going to push back at your engineer's suggested layout ideas, make sure to base your thinking in physics, not in some half-baked idea that came from an app note or a poorly designed evaluation board (this is fodder for another article).

It is very important to know, schematically, how a circuit will function, "what drives what," "what is dependent on what," and what timing issues are critical. These are things you should understand whether you are a circuit engineer or a board designer. Not having an EE degree does not relieve designers from the absolute need to understand basic circuit behavior. If you do not know, ask! However, knowledge of these things, alone, will not eliminate the risk of SI or EMI problems. There is much more to this issue.

So, what is the solution to good PC board design? One thing has held true over the decades: Understanding how to design to maximize manufacturability, testability, ease of repair, and good thermal transfer has not changed and probably never will. Board designers will always need to know about these issues. Of this, most designers and engineers agree. Is knowledge of electronic circuit theory necessary to lay out sensitive transmission lines and complex power delivery? No! Knowledge of circuit theory does not hurt your cause but, by itself, is not the solution.

What you need to know is elemental electromagnetic field theory. The problem is not about voltage and current; it is about EM waves moving through transmission lines. Folks who understand this have their arms around the real problem.

"What you need to know is elemental electromagnetic field theory. The problem is not about voltage and current; it is about EM waves moving through transmission lines."

Thanks to guidance from friends like Ralph Morrison and Dan Beeker, I have understood this for many years and now know the real solutions. Once this knowledge settled into my little brain, I suddenly realized exactly what causes problems in PC boards and what to do to avoid them. Everything became crystal clear! Where do you stand? Consider the following:

- Current in a transmission line forms in the copper, but the energy of the line is not in the copper.
- Energy in transmission lines moves through the plastic insulation of the board, the space between the copper features.
- Current formed in vias is all on the outside of the via barrel. No current flows on the inside of a via.

Those three simple statements tell us a lot about why problems occur in some boards and not in others. If any of those comments sound foreign to you, whether you are a circuit engineer or a board designer, you must read a good

book about fields in PC boards, or run, don't walk, to the next PCB West Design Conference. This is not a sales pitch for PCB West, but it happens to be a great venue for such training. There are other excellent conferences, as well as books and other publications that can provide this information.

Are engineers taking over board design? Those able to stay awake when Maxwell's equations hit the blackboard, who were conscious when field theory was introduced, do have a leg up over folks who do not possess this knowledge. Many of the new board designers will likely come from the EE community, but it is certainly not necessary to be an EE, as long as you understand the real issues.

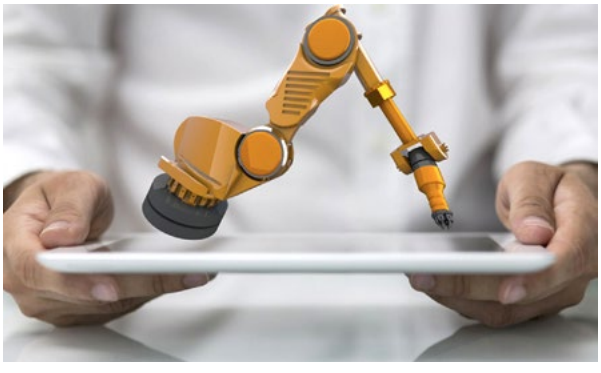
As mentioned, items associated with elemental field theory can be learned at conferences or from books. This and how it applies to PC board design is what you most need to know to be a great board designer, one who lays out 'noise free' circuits. Aside from field theory, as mentioned earlier, every good designer needs knowledge of manufacturability, testability, etc.

So, you want to get along at work? Have the EE and PCB groups collectively learn how and where energy travels in PC boards (field theory). Using that knowledge, decide how the boards should be properly stacked, routed, etc., to take advantage of the natural condition of EM wave movement. Once you do this, designs will work and pass EMI testing and there will be no more tension between the EEs and board designers, at least not over board layout, and you can both stop designing from app notes, rules of thumb and voodoo techniques.

And remember: We're all in this together! **PCBDESIGN**

Rick Hartley is the founder and principal engineer of RHartley Enterprises, through which he teaches and consults to eliminate SI, noise and EMI issues in PC board design. Rick can be reached by clicking here.

Hannover Messe: Industry 4.0 Has Become a Reality



"Integrated Industry - Discover Solutions" is the slogan of this year's Hannover Messe, which will open its doors on 25 April. Member companies and the VDMA can present a great number of solutions for the workings of the factories of the future and for making Industry 4.0 a reality in Hanover. "Industry 4.0 has become a reality with intelligent products, production lines and value chains," says VDMA Executive Director Thilo Brodtmann. New business models for digital and interconnected production are being developed across the board and will be put on display in Hanover. "Anything you see at the stands there can be profitably deployed in your business. Thanks to its specific and profound knowledge of production and customer needs, German mechanical engineering has the edge here," Brodtmann points out.

In numerous presentations, discussions and press conferences at this year's Hannover Messe, the VDMA will make it clear that mechanical engineering stands at the heart of the tremendous changes that will shape commercial life in the years to come.

The modernisation of the economy is also being promoted forcefully in the partner country of this year's Hannover Messe, the USA, under the catchphrase "Internet of Things." "But we have nothing to fear from the Americans," stresses Brodtmann. "We are in a good position in this race, and at some point the approaches on both sides of the Atlantic will coalesce into one giant whole."

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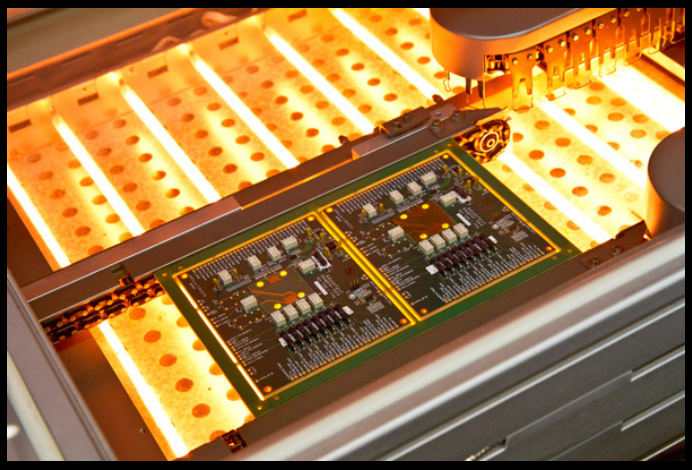

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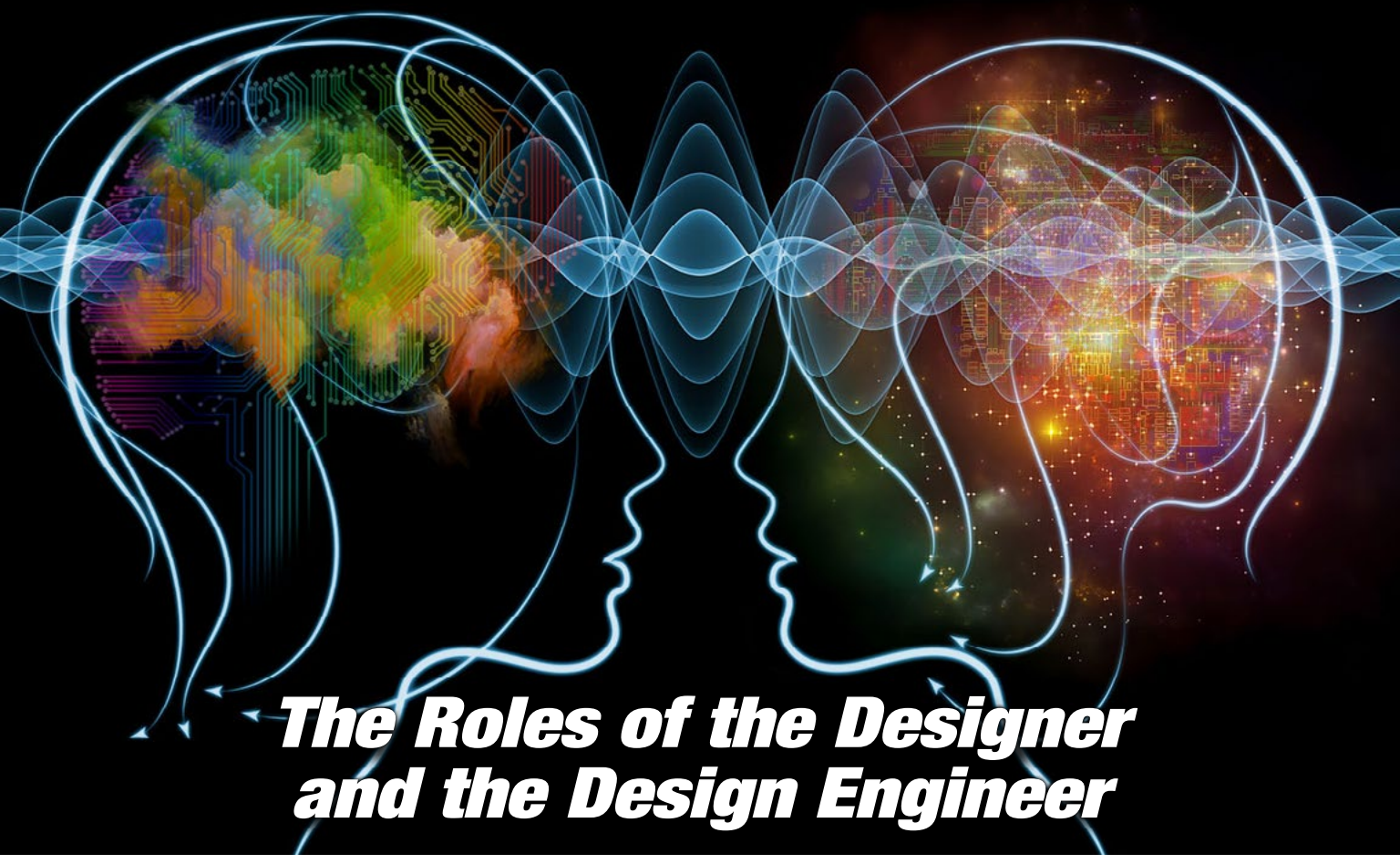

The Roles of the Designer and the Design Engineer

by Andy Shaughnessy

Steve Hageman has been designing electronics since elementary school. An engineer by trade, he has decades of experience performing PCB design and layout. He spent years at HP, Agilent and Calex before hanging out a shingle for his engineering company, Analog Home. As someone who wears engineer and designer hats, Steve was a natural for this month's issue. I asked Steve to give us his opinion about the divide between some PCB designers and their engineers, and what can be done to solve this problem.

Andy Shaughnessy: *Steve, tell us a little bit about your company and how you operate.*

Steve Hageman: I have experience working for companies of 50 people, to working for a company with 10,000 employees, to working as an individual contributor solving my specific customers' problems. As most engineers will agree, solving specific customers' problems is perhaps the most rewarding.

Shaughnessy: *A recent survey of our PCB designer readers found that there's often friction between PCB designers and engineers. Some designers say their EEs are their biggest challenge. Why do you think there's such disconnect?*

Hageman: I remember a quote by David Packard: "Follow the advice that Abraham Lincoln gave himself: 'If I don't like this man, I have to get to known him better.'" I have found that to be very true. Mr. Packard also knew that to get along with others you had to understand what they face as challenges. Taking the time to see the other person's point of view is very hard today with the crush of schedules that we all have.

I think the biggest disconnect is the schedule compression that happens. We all know how this goes: The design takes longer than expected, so the PCB start date is pushed out, but the PCB delivery date is not changed, hence the poor guy that is last on the schedule has his schedule compressed beyond belief. By then, everything is rushed and things fall through the cracks. And what falls through the cracks typically is the EE design constraints.

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The PCB folks are also pushed by manufacturing and these manufacturing rules are oftentimes only vaguely known by the EEs, hence they don't know what to allow for.

At very large companies there is a third entity pushing the PCB layout: the EMC/safety folks. Again, more constraints and rules that the EE may only vaguely know about. All of this comes together with schedule compression and causes the PCB folks to have to redo portions of the design to meet all the known and unknown design constraints.

Redoing work is never fun for anyone, especially when the time demands are so great. The only solution that I know of is to learn from the uncovered serious problems and with the team decide a path forward to try to prevent these from happening again in the future. And then try to stick to the plan.

***Shaughnessy:** What do you think is the proper role for a PCB design engineer?*

Hageman: The design needs to be sound and well specified, and a floorplan of the design needs to have been at least thought about that takes into account all the stakeholders' design constraints. Hopefully then the PCB design can be started. Checkpoints should be built into the system. While this seems to add extra time, I find that it really doesn't if it prevents rip-up and retry on the part of the PCB designer.

***Shaughnessy:** What do you think is the proper role for a PCB designer?*

Hageman: Putting on my PCB designer hat, I would need to make sure that what is given me is complete. The design has been reviewed, that is, the other stakeholders have had a chance to look at the floorplan and have had a chance to make inputs. Then the PCB design can start. I find that having many checkpoints along the way works best. But stuff will go wrong and we all need, as the beer commercials say, "to stay frosty."

***Shaughnessy:** Some PCB design tools are marketed directly to the design engineer, not the PCB designer. Do you think PCB designers are being squeezed out?*

Steve Hageman

Hageman: I'm sure it happens both ways. In the larger companies I have worked where there are PCB layout groups or services, I have found that the PCB groups usually have the most say on tool sets. Basically everyone wants to use the tool that they know and can work with. This is only natural. Making sure that there is adequate training can help those on both sides that feel left out of the loop. Training today can be provided very cost-effectively by the tool set vendor or their FAEs.

***Shaughnessy:** With more and more engineers doing PCB design work (some PCB design and layout classes are 50% EEs), what do you think is the solution to this friction?*

Hageman: I personally like doing my own PCBs; I always have, but some engineers really don't like doing this work. It's a point of personal preference. In small companies you might be forced to do your own designs and in a large company

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you might be prevented from doing your own designs. Companies have broad expectations and rules also. This shouldn't be a point of friction; it should be mutual work toward getting the job done. In my experience this has only been a sore point when the PCB-specific folks felt like their jobs were going away. I don't think this will ever happen as I have found that only about 1/3 of EEs want to do their own layouts. We can and should help each other out in getting to that end goal: solving our customers' problems.

Shaughnessy: *Is there anything else you'd like to add?*

Hageman: My experience at Hewlett Packard was the best as far as teams go. There was no blame, if anyone stumbled and fell, the rest of the team would pick the guy up, dust him off and we would all get on with it. I try to remember and mimic this behavior as much as possible. I also find that keeping focused on who is paying the bills, namely our shared customers, helps in keeping the inter-team friction down. It doesn't always work, it isn't easy and it needs to be worked on continually.

Shaughnessy: *Thanks for your time, Steve.*

Hageman: Thank you, Andy. **PCBDESIGN**

And the Survey Said: What are Your Pain Points?

As you all know, we survey our readers fairly often. We want to know what's going on with PCB designers and design engineers, especially the challenges and pain points that you all face.

After we sift through the percentages, we focus on your comments. The comments are a source of great information. They may be emotional, unscientific, and sometimes rambling comments, but it's accurate and from the heart.

I recently asked my readers to name the biggest challenges that they face every day. Here is a sample of the comments. Do these sound familiar to you?

- Lack of time (too tight production deadlines) and on time feedback from the clients (often resulting in massive amounts of extra work). Not getting timely feedback from initial testing. Our policy against slapping the snot out of idiots.
- Getting people to attend design reviews.
- Things like solder mask defined pads in some areas and copper defined in others, with PCB suppliers using global copper defined rules, lack of understanding of the soldering process in things like wave solder.
- Making symbols and cells for our CAD system.
- Meeting SI requirements for signal integrity. Placement of critical components within very tight areas and still meeting DFA requirements.
- Defining the stackup and impedance critical signals without a good tool. Getting a PCB description direct out of the tool.
- Time to market! Engineers can get too involved in the little details, and fail to achieve time to market goals.
- Feature creep from the customer to the senior engineer and the designer.
- Electrical constraint requirements not described in schematic.
- Not enough man-power.
- Specifying alternative parts (second and third sources). Critical areas (noise, heat, vibration, etc.) indication. Lack of useful communication on what the designer and EE consider important to the design.
- Bean-counter management types who don't understand today's challenges.
- Manufacturability, testability, and reworkable design, as parts get smaller, with high-density pinouts.
- Keeping cost of fabrication reasonable using fine-pitch devices, i.e., avoiding blind and buried microvias for devices 0.5mm pitch or less.
- HDI technology with several via types. Definition of power/ground systems for better EMI. High-speed signals. Ceramic boards with thinner tracks. Embedded parts.
- Real estate, signal noise, and thermal electric offsets.
- More things to pay attention too. Power drop with in the PC board due to low voltages now. Thermal dissipation from small package with higher wattage use.

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Designers and Design Engineers: Two Sides of the Same Coin

Andy Critcher, TBS

by Andy Shaughnessy

Andy and Sue Critcher have been the lead designers at Total Board Solutions Limited, an UK-based design bureau, since its founding in 1998. I asked Andy to share his opinion about the friction between some PCB designers and their engineers, and what can be done to improve communications between these groups.

Andy Shaughnessy: ***Andy, tell us a little bit about your company and how you operate.***

Andy Critcher: Total Board Solutions Limited (TBS) is a design services bureau based in the UK. We fit into our customer's design process, providing whatever is not a core competency. This means that for some customers we perform just the layout portion of their design while for others we enter the schematic, libraries, create the layout and even get the boards fabricated and assembled—no two customers are exactly the same. When working with startups we provide the link between the concept, or idea, and product realization; providing knowledge of design process, fabricators capabilities and our experience when discussing the inevitable tradeoffs between the requirement and what is possible.

Shaughnessy: ***A recent survey of our PCB designer readers found that there's often friction between PCB designers and engineers. Some designers say, only half-jokingly, that their EEs are their biggest challenge. Why do you think there's such disconnect?***

Critcher: Looking solely from the PCB side, I think that the disconnect mainly arises from the lack of understanding of what a PCB designer actually does, it is perceived as a simple task of dot joining and that anyone can do it. I know that this is a bit of a cliché but it does seem to hold true. As an example, in a number of the companies that I have worked with, PCB progress meetings are held and the PCB designer is never asked to attend; their input can be easily be determined by the engineering team/project manager.

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This perception is backed up by the lack of formal qualification for PCB designers—for my generation, we generally started off as mechanical draughtsman in the traditional drawing office and then moved to the PCB section.

This perception means that the status of the PCB designer is quite low, so when they advise the engineer that something is not possible this can be met with a certain amount of derision. The engineer possibly thinks that the PCB designer is just being obstructive, while conversely, the PCB designer thinks that the engineer is very dismissive of his knowledge, capabilities, opinion, etc.

“The engineer possibly thinks that the PCB designer is just being obstructive, while conversely, the PCB designer thinks that the engineer is very dismissive of his knowledge, capabilities, opinion, etc.”

Let’s look at the issue from the engineer’s perspective. By providing design consultancy, we are fortunate enough to be a lot more involved in the engineer’s world, including some of the problems that they have to deal with as part of the overall product development. One engineer explained that the design part was relatively straightforward, but the need to meet cost, functionality, component sourcing, obsolescence, test plans, as well as reading through 150+ pages of documentation on a device’s timing “makes life interesting.” As PCB designers, we tend to have a lot of questions, especially about the newer technology, so we can bombard the engineer with a number of questions concerning unfamiliar topics expecting immediate answers, and normally at this point the pressure to get it finished is already building.

***Shaughnessy:** What do you think is the proper role for a PCB design engineer?*

Critcher: This is a difficult one to answer. There are so many aspects of the design engineer’s role that are not obvious to the PCB designer, such as component selection, obsolescence management, test plans/specs, etc. I thought that I would answer this question in relation to their interaction with the PCB designer.

The definition of the circuit itself goes without saying; the engineer should also drive the PCB layout with the necessary constraints to ensure that the PCB will function to within spec. So, together with the circuit diagram the engineer should also indicate the following (this list is not exhaustive)

a. Impedance requirements
b. Trace length/matching requirements
c. Current handling requirements
d. Stackup requirements
e. Placement constraints
f. Connector locations
g. Board outline (could be the mechanical engineer)

Depending upon the software and the individual company process, the engineer may be able to enter these constraints directly into the schematic capture tool.

***Shaughnessy:** What do you think is the proper role for a PCB designer?*

Critcher: The role of the PCB designer is to take the data from the engineer and create the layout, drawings, fabrication and assembly data while adhering to constraints and the relevant standards, including both company, IPC and any specific to the manufacture.

The PCB has many outside influences such as enclosure, thermal, EMC requirements that may not be under the remit of the engineer so they should also liaise with these people or teams.

Essentially the PCB designer takes all the design requirement inputs from the various sources and then has to find a solution that hits as many as the requirements as possible. At this

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point the PCB designer essentially drives the physical design.

I think that to be effective in this role it helps to have a working knowledge of signal integrity, power integrity, and RF and analogue layout techniques. In my experience, I have found that in larger companies, there is a level of specialization for engineers; this tends not to be the case for PCB designers so they are "au fait" with multiple disciplines.

The PCB designer should also keep up with the latest technologies for components, board fab and assembly.

Shaughnessy: *Some PCB design tools are marketed directly to the design engineer, not the PCB designer. Do you think PCB designers are being squeezed out?*

Critcher: In general the answer is no; in my experience I find that this may be practical for smaller design teams or for less complex PCB layout, but when the design is either mixed-technology (RF, digital and analogue) or a complex layout with large component and net counts, a dedicated PCB designer is the most successful solution.

There are a number of reasons why I think this. Firstly, it is NOT that the engineer is not capable of performing the layout task, but more with regard to the pressures on design teams to deliver on time to meet the time-to-market requirements most design teams need to parallel as many tasks as possible, layout included.

Further to this, the schematic is generally a living document that evolves as the layout proceeds due to marketing requirements or simulation results, etc.—the engineer cannot perform two discrete tasks at the same time—to maximize the time efficiency of the design team as a whole separating the two tasks makes sense.

On a practical side, the electronic engineering teams are generally split via the design disciplines already mentioned—RF, analogue and digital—would this mean that each engineer would take it in turns to layout their section?

The PCB tool set is a complicated environment; although the new breed of tools provide ways to support the entry of the complex data sets such as constraints, the complexity continues to increase ahead of the tools. Essentially the environments are not really for the casual user. The automation of the applications increases but the need to enter the constraint data and drive the tool successfully requires the user to use the toolset day-in and day-out to be efficient. In many instances the engineer could spend a few weeks to over a month away from the tools themselves as they test and commission the PCBs.

"In many instances the engineer could spend a few weeks to over a month away from the tools themselves as they test and commission the PCBs."

Another area that the PCB designer has a certain amount of experience is in the actual fabrication and assembly process; this is generally accumulated over a number of years working with these disciplines. Pre-preg suitability etc., all goes into the pot.

The PCB designer spends a lot of time taking input from different engineers and this helps hone their skill set; taking input from multiple sources helps the designer solve future problems by being able to draw on the gathered experience from the different sources.

In the same way that many companies have a dedicated signal integrity team, the idea of a dedicated PCB makes sense for the same reason.

Shaughnessy: *With more and more engineers doing PCB design work (half of the attendees at some PCB design and layout classes are electronics engineers), what do you think is the solution to this friction?*

Critcher: I think that the solution to the friction is communication, integration and pa-

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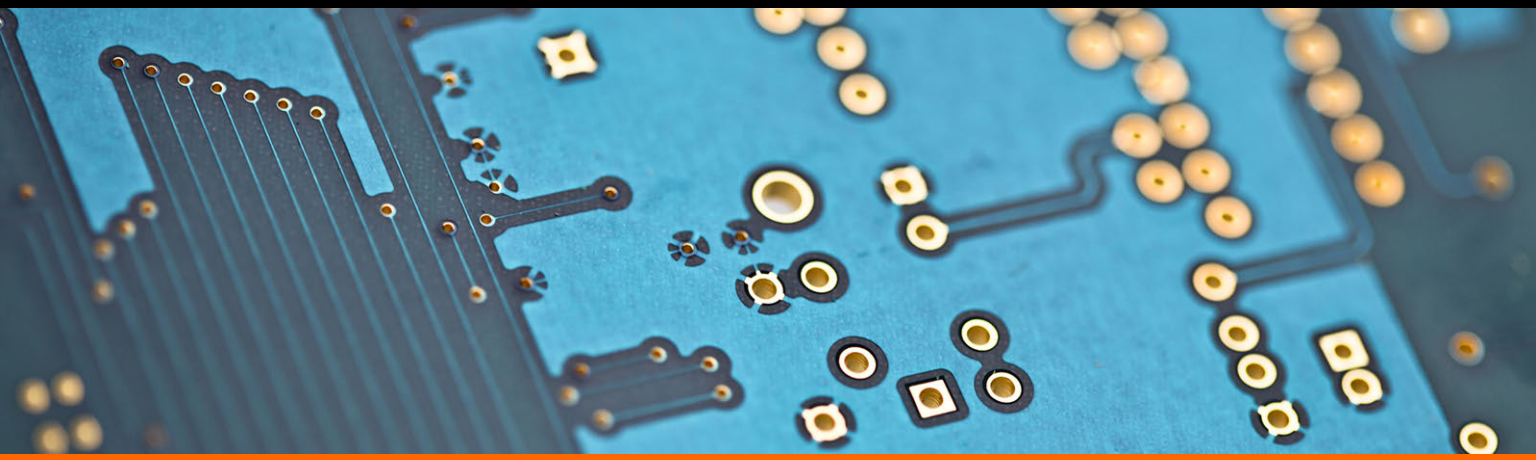

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tience; situations like this cannot be fixed overnight.

Over the years I have noticed that when I work with companies who have a 'design team' comprising electronic engineers, PCB designers, mechanical engineers signal integrity engineers etc. who are tasked with a specific board or product design there is less friction.

I have seen most friction when the 'teams' are divided by function/discipline rather than by project teams. I also tend to see that the team is more effective when the aims/goals are shared; this especially works well where a concurrent design process is needed.

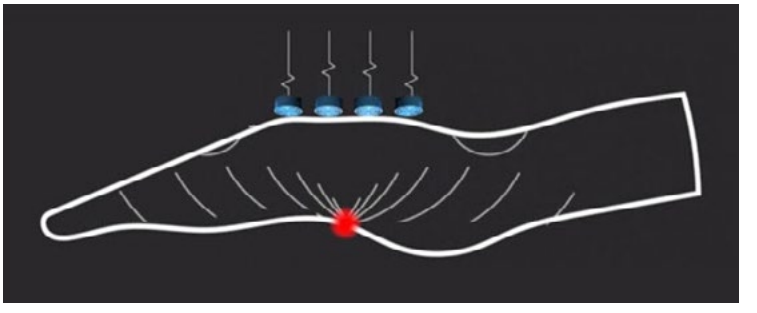
Shaughnessy: ***Is there anything else you'd like to add?***

Critcher: I think that the ability to perform the design of the PCB in parallel across the design team today is critical in many cases. If we have a single person performing each individual task in series this would not help reduce the design time.

Shaughnessy: ***Thanks for your time, Andy.***

Critcher: Thank you. **PCBDESIGN**

University of Sussex Research Brings 'Smart Hands' Closer to Reality



Using your skin as a touchscreen has been brought a step closer after UK scientists successfully created tactile sensations on the palm using ultrasound sent through the hand.

The University of Sussex-led study - funded by the Nokia Research Centre and the European Research Council - is the first to find a way for users to feel what they are doing when interacting with displays projected on their hand.

This solves one of the biggest challenges for technology companies who see the human body, particularly the hand, as the ideal display extension for the next generation of smartwatches and other smart devices.

Current ideas rely on vibrations or pins, which both need contact with the palm to work, interrupting the display.

However, this new innovation, called SkinHaptics, sends sensations to the palm from the other side of the hand, leaving the palm free to display the screen.

The device uses 'time-reversal' processing to send ultrasound waves through the hand. This technique is effectively like ripples in water but in reverse - the waves become more targeted as they travel through the hand, ending at a precise point on the palm.

It draws on a rapidly growing field of technology called haptics, which is the science of applying touch sensation and control to interaction with computers and technology.

Professor Sriram Subramanian, who leads the research team at the University of Sussex, says that technologies will inevitably need to engage other senses, such as touch, as we enter what designers are calling an 'eye-free' age of technology.

"Wearables are already big business and will only get bigger. But as we wear technology more, it gets smaller and we look at it less, and therefore multisensory capabilities become much more important," he says.

"If you imagine you are on your bike and want to change the volume control on your smartwatch, the interaction space on the watch is very small. So companies are looking at how to extend this space to the hand of the user. What we offer people is the ability to feel their actions when they are interacting with the hand."

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The Partnership: Design Engineers and PCB Designers

by Andy Shaughnessy

Randy Faucette is founder, president and director of engineering at Better Boards Inc. in Cary, North Carolina. Founded in 2003, Better Boards provides electrical engineering, PCB design, signal and power integrity analysis, and a variety of other services. I asked Randy to talk about some of the occasional tension between PCB designers and design engineers, and what he thinks can be done to help open the lines of communication.

Andy Shaughnessy: *Randy, tell us a little bit about your company and how you operate.*

Randy Faucette: Better Boards is a PCB design and engineering services company. We specialize in all aspects of PCB design, but also provide electrical and mechanical engineering, software/firmware development, prototype and small-volume production manufacturing, and many types of analysis including failure mode, root cause, thermal, crosstalk and power integrity. We use a breadth of design tools including Cadence Allegro, Altium, Mentor Expedition and PADS. Our customers range from large companies like Lenovo and Cree to small entrepreneurs. We perform finite services our customers define to full development of products from concept to production. We cover many industries, such as medical, commercial, consumer, telco, and space/military.

Shaughnessy: *A recent survey of our PCB designer readers found that there's often friction between PCB designers and engineers. Some designers say, only half-jokingly, that their EEs are their biggest challenge. Why do you think there's such disconnect at some companies?*

Faucette: We have not found that to be true here at Better Boards. We approach PCB design from an engineering standpoint. The PCB designer should not just be a tools jockey hoping that engineering will tell them where to put parts and how to hook them up. The PCB designer should understand how the circuits flow, understand the different types of interfaces and how those need to be treated on the board, and un-

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Randy Faucette

derstand the manufacturing aspects as well (including test). The only challenge we experience with engineering honestly is playing the role of middleman between engineering and manufacturing. Engineering may want parts located too close to another component or too close to a through-hole pin, not allowing a proper wave soldering operation to be performed. Those drive costs and can affect reliability. If the layout designer is effective, engineering is happy and manufacturing is also happy. That makes the boss happy!

***Shaughnessy:** What do you think is the proper role for a PCB design engineer?*

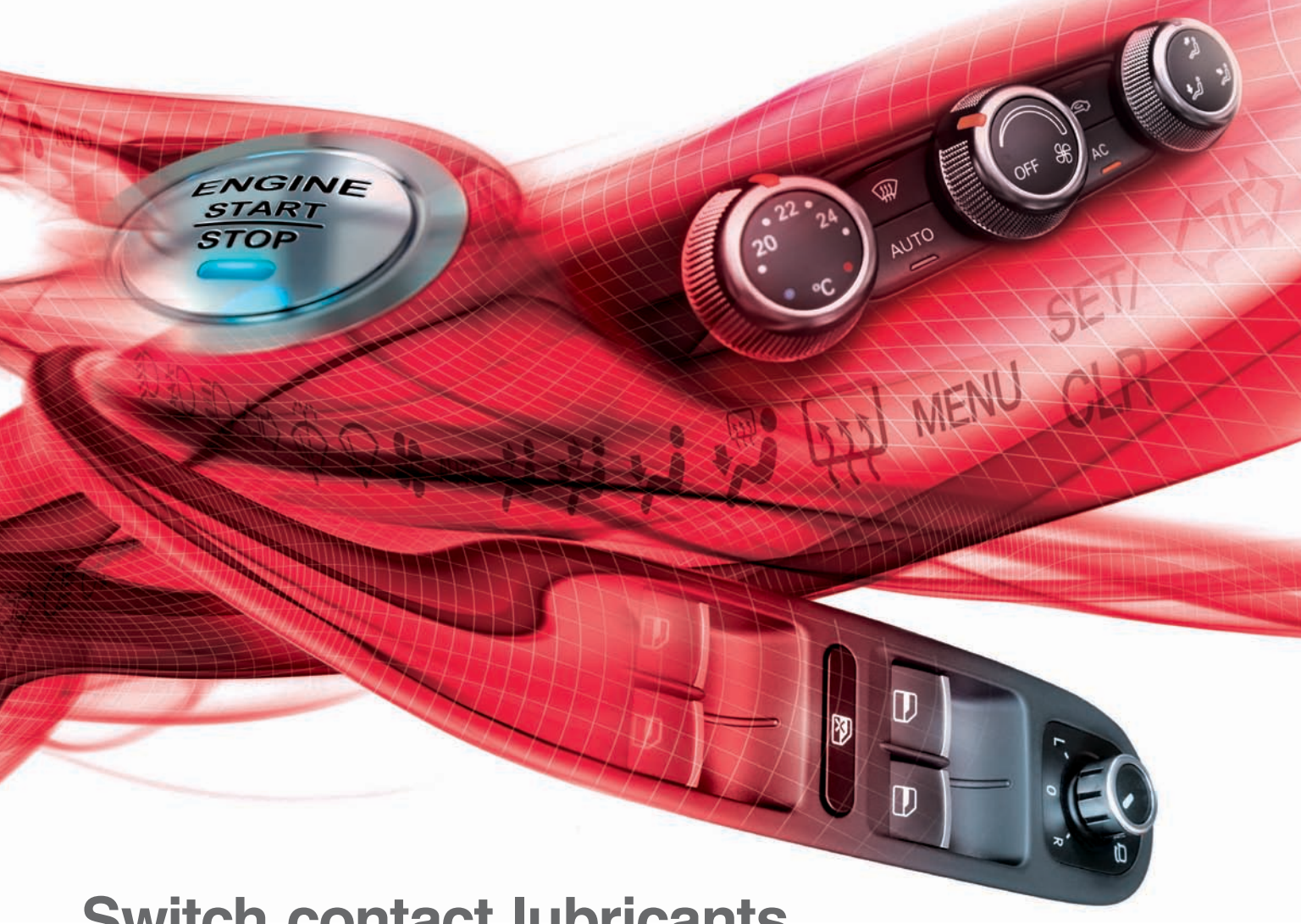
Faucette: Outside of creating a correct schematic, the PCB design engineer needs to effectively communicate ALL of the requirements of the board and then review the board once designed to ensure all the requirements have been achieved. Some examples of requirements would be interface impedances, timing rules, and power requirements. It's also important to identify high-speed nets, clock lines, sensitive nets/circuits, high-current buses, thermally hot nodes, high switching loops. The stackup is critical in most designs today and this must be considered early. One thing that should be communicated early on is the environment of the product and the expected reliability. The temperature and humidity can drive what component packages to use (or more importantly what not to use). The reliability can drive board technology and spacings. The best way to communicate all the rules is in a PCB requirements document. This is the scope of the layout. If it's in the document, it's important. It also removes the flurry of comments, instructions, and "Oh, BTWs" that tend to arrive in various emails and in cubicle conversations. It's a captive, living document to keep everyone straight. It's also it a perfect checklist at review time.

***Shaughnessy:** What do you think is the proper role for a PCB designer?*

Faucette: The PCB designer's role is to take the requirements (hopefully as spelled out in the requirements document) and create a layout that performs as needed electrically, but that can also be manufactured with high yield, and that will be reliable. The PCB designer should pull in all the mechanical requirements (outline, mounting holes, critical component locations, keepouts and other restrictions) and ensure form and fit are correct. The PCB designer should also ask all the questions to spark conversations so that all requirements can be discussed and documented early. At final review is not the time to find out that an ICT fixture is needed.

***Shaughnessy:** Can you give us an example of how your designers and engineers function together?*

Faucette: Early collaboration is key. Hopefully, every design provides the opportunity to learn and that knowledge can be implemented going forward. Learning never stops. As we grow in our careers, we become more and more effective and efficient in our roles. The result should



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Shaughnessy: *Some PCB design tools are marketed directly to the design engineer, not the PCB designer. And more engineers are doing PCB design work—half of the attendees in some PCB design and layout classes are electronics engineers now. Do you think PCB designers are being squeezed out?*

Faucette: If the PCB designers are being squeezed out, it's either because they are not doing their job or they are not being supported by management. If the engineer needs to explain how the flyback power supply should be placed and routed each time, then perhaps the engineer should just perform the work (if it takes an hour to sit with the designer to layout a power supply or it can take them an hour to just do it themselves, why spend two man-hours when one will do?). However, the designer should not be squeezed out. The demand of the board performance is growing and that requires a different set of knowledge. The board need to run faster signals, carry higher currents due to lower voltages, and dissipate more heat due to smaller packages. We don't think it's realistic for engineering to keep up with that and take over the role of layout. The reality is that experience is key here. There are no classes in college that teach proper layout or electronics packaging. You may do a couple of layouts for a class project, but you can't replace 20 years of gained knowledge from having layouts be your primary function. Having said that, PCB designers need to stay up with the latest technologies, materials, manufacturing processes, IPC specifications, and component package trends.

Shaughnessy: *A few designers who work great with their EEs say it all comes down to an unspoken agreement, an understanding of who does what. Is it really that simple?*

Faucette: If they are both seasoned in their roles, then yes. The engineer does their job and delivers a good handoff to the designer and the designer carries it across the finish line. There is no way an engineer can layout a couple of boards a year and be a good layout person. Good layouts don't happen by accident. Sorry, tool companies.

Shaughnessy: *Is there anything else you'd like to add?*

Faucette: Continuous education is critical. This is why Better Boards has gotten very involved in the local chapter of the IPC Designers Council and has been instrumental in the existence of PCB Carolina held in Raleigh each fall.

Shaughnessy: *Thanks for your time, Randy.*

Faucette: Thank you, Andy. **PCBDESIGN**

LOPEC 2016—Printed Electronics: A Key Technology of the Future

From April 5-7, 2016, LOPEC displayed pioneering and innovative products from the field of printed electronics in Munich, Germany. A total of 148 companies made their way from 18 countries to exhibit at the International Exhibition and Conference for the Printed Electronics Industry.

For the first time, Indian, Spanish, and South Korean companies were among the exhibitors. More than 2,000 visitors from over 40 countries attended LOPEC 2016. The key industry markets were also reflected in the most strongly represented nations in terms of visitors, which, besides Germany, were the UK, the USA and Japan.

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PCB007 Highlights

DuPont, Taconic and PFC Team-Up for High-Speed Fle

At DesignCon, I sat down with three flex circuit specialists: Glenn Oliver of DuPont, Tom McCarthy of Taconic, and Steve Kelly of PFC Flexible Circuits. Our discussion covered a lot of territory, most notably the findings they described in the paper they were about to present later that day at DesignCon, and more.

Rex Rozario: The PCB Industry's True Renaissance Man

In this exclusive multi-part interview that was conducted recently, I-Connect007's Barry Matties will introduce you to all of the people that Rex Rozario is, and where he, his team, and Graphic PLC are headed to next.

Happy's Essential Skills: Problem Solving

Related to TQC and a very important role of an engineer is solving problems. Using a problem-solving methodology is a job that all engineers will use sooner or later, but if you are in product or process engineering in manufacturing, it will be sooner! This was the situation that introduced me to printed circuit manufacturing.

Happy's Essential Skills: Design of Experiments

Design of experiments (DOE) is one of the most powerful and influential engineering tools for product yield improvements, new products or processes development, or for problem solving. As mentioned in my last column, process problems led me to a career in printed circuits, and quickly solving those problems led me to a bonus stock award and a great life.

Manufacturing Institutes can Boost the Nation

In his most recent State of the Union address, President Obama highlighted a remarkable trend of recent years: the turnaround in many corners of America's manufacturing sector. Nearly 900,000 new jobs have been created by U.S. manufacturers in the last six years.

Copper Via-Fill Technology in Development

The use of via-in-pad technology is increasing rapidly in today's PCB designs. The need for miniaturization, combined with the rapidly decreasing pitch of component footprints, drives printed circuit board designers here. Via-in-pad requires the vias to be filled, planarized and then over-plated with copper.

The Quiet Mainstreaming of HDI Manufacturing

Advances in technology continue to push the envelope of what's possible. And nowhere has the impact of those advances been felt more profoundly than in the evolution of the current class of mobile devices. Although design engineers have driven this evolution, the push to meet the associated manufacturing challenges has been responsible for a revolution in PCB manufacturing.

Weiner's World

Gene Weiner discusses PhiChem's upcoming open house event at its global HQ and R&D center in Shanghai during SEMICON China 2016, CPCA 2016 and productronica China 2016. He also focuses on the IPC Ambassador Council's plans to produce an executive forum in conjunction with IPC APEX EXPO 2017, IPC's association with NextFlex, and much more.

The Sum of All Parts: The Cost of Quality

Throughout the decades, irrespective of industry or sector, markets have thrived on competition. They have, however, also relied upon some semblance of unity within their respective competitors. Industries rely upon their individual member companies' ability to work together for the greater good.

Rex Rozario, Part 4: A 10,000-ft. view of his Business Ventures, the Industry, and Life

In our final installment, Rex describes the common thread woven through all of his successful business ventures and varied interests: confidence and the fortitude to follow his dreams until they are realized. Rex also takes a look back at the evolution of the global PCB industry, and explains his approach to profitability, which includes building (and rewarding) a successful team.

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DDR3/4 Fly-by vs. T-topology Routing

by Barry Olney
IN-CIRCUIT DESIGN PTY LTD AUSTRALIA

JEDEC introduced fly-by topology in the DDR3 specification for the differential clock, address, command and control signals. The advantage of fly-by topology is that it supports higher-frequency operation, reduces the quantity and length of stubs and consequently improves signal integrity and timing on heavily loaded signals. Fly-by topology also reduces simultaneous switching noise (SSN) by deliberately causing flight-time skew, between the address group and the point-to-point topology signals, of the data groups. To account for this skew, the DDR3/4 controller supports write leveling. The controller must add the write leveling delays to each byte lane to maintain the strobe to clock requirement at the SDRAMs.

T-topology can be challenging to route, particularly double T-topology with four back-to-back SDRAMs as in Figure 1, but it can be advantageous when using multi-die packages. The fly-by topology used in Figure 3 is much easier to route but does not work well with high-capacitance loads, such as LPDDR3 DDP (double die package) and QDP (quad die package) devices. IC fabricators basically arrange dies in parallel (as in Figure 2) to increase package density which can also increase input capacitance by up to four times. Excessive ring-back is often present in the first few nodes of the daisy chain.

This is the reason why the T-topology was developed. However, if you are supporting only SDP (single die package) devices, then the fly-by

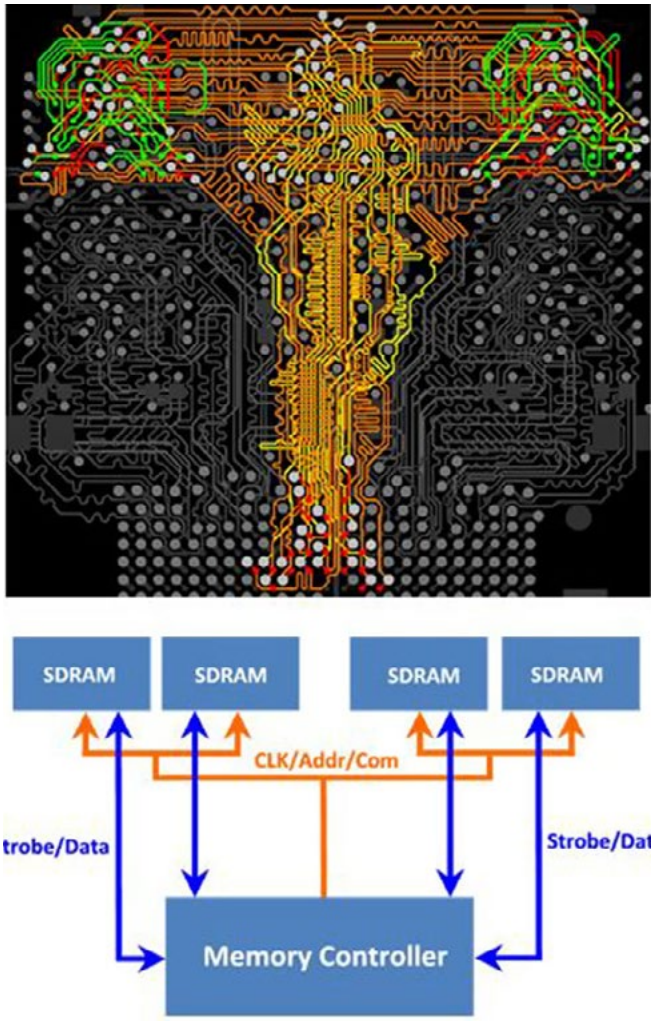

Figure 1: Double T-topology for clock/address/command/control routing.

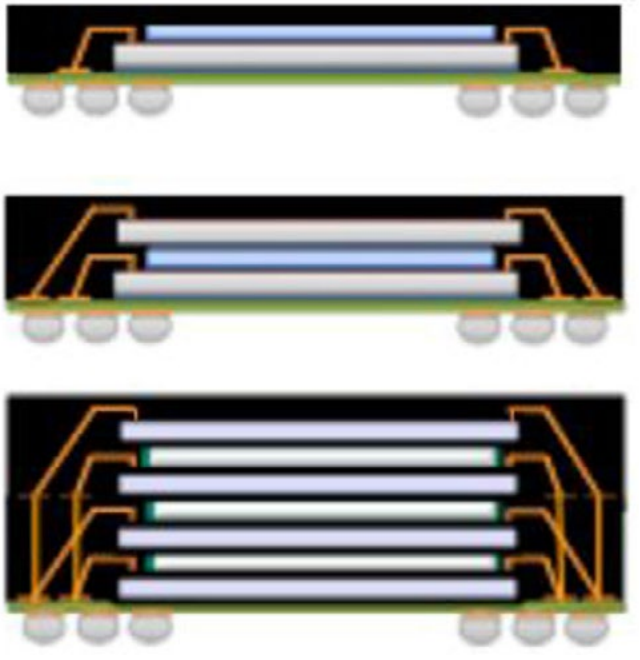

Figure 2: SDP and multi-die DDP and QDP memory devices.

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is the most straightforward approach. It doesn't matter which topology you use, though—both fly-by and double T-topologies should work fine. If you are using a DDP device, then double-T topology works better than fly-by in terms of delivering a better system margin.

During a write cycle, using the fly-by topology, data strobe groups are launched at separate intervals to coincide with the clock arriving at memory components on the SODIMM or PCB, and must meet the timing parameter between the memory clock and DQS defined as tDQSS of ± 0.25 tCK. The PCB design process can be simplified using the leveling feature of the DDR3/4. The fly-by, daisy chain topology increases the complexity of the controller design to achieve leveling but fortunately, greatly improves performance and eases board layout for DDR3/4 designs.

It is not that you have to use fly-by write leveling, because it is a feature of DDR3 and DDR4, but rather that you have to use write leveling in order to allow fly-by routing. There is also no reason not to use the write leveling training for a T-topology in order to optimize the write strobe to clock timing. With this you can adjust slight differences in CA timings and avoid hard coding the skews that you normally have to manually take care of on the strobe to clock delay.

Fly-by topology is similar to daisy chain or multi-drop topology, but has very short stubs, to each memory device in the chain, to reduce the reflections. The double T-topology was used for DDR2 and had a downside in that the impedance discontinuities, due to branching along the traces, caused obvious margin losses. T-topology also tends to have overshoots, while the levels for fly-by are terminated and therefore do not reach the full swing voltage rails. Also, the length of the stubs has an effect on the maximum bandwidth of the transmission line. If you are employing high-frequency DDR4, then the bandwidth of the channel needs to be

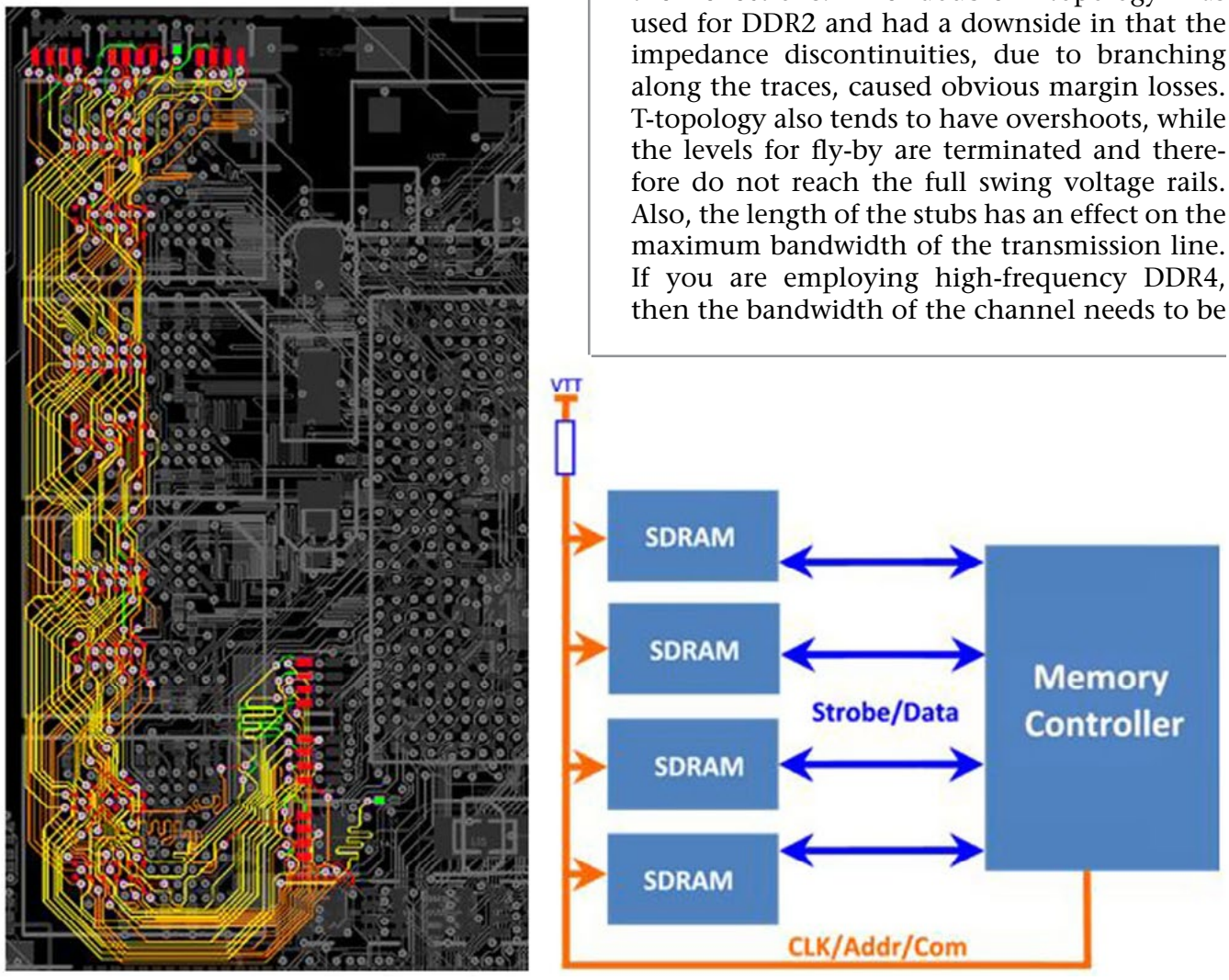

Figure 3: Fly-by topology for clock/address/command routing.

as high as possible. With conventional T-topology, the trace stub is lengthened with an increase in the number of memory device loads. In some cases, there can be as many as eight memory devices connected to the processor. The resonant frequency or bandwidth is inversely proportional to the stub length.

$$fo = \frac{c}{4\ x\ (stub\ length)\ x\ \sqrt{Er}}$$

where fo is the resonant frequency, c is the speed of light and Er is the dielectric constant

The clock traces should be routed to a longer delay than the strobe traces per byte lane. This is necessary because:

1. The write leveling is capable of adjusting the clock to write data strobe alignment over a wide range, assuming the clock trace has a longer delay than the strobe traces.
2. The read leveling is capable of adjusting the read data eye to read the data strobe over a wide range. The adjustment is per byte, so board skew between the data and data mask signals should be minimized.
3. There is no automatic training for aligning command/address signals to the clock, but a fixed offset is programmable, in the processor, and can be used if necessary. Skew between the clock and address/control signals should be minimized.

Designing a memory interface is all about timing closure. Each signal's timing needs to be compared to the related clock or strobe signal in such a way that the data can be captured on both the rising and falling edge of the strobe—hence the term double data rate (DDR). The increase of data rates, to 4266MT/s for DDR4, has made the timing margin associated with each rising and falling edge much tighter. Even though a direct successor is not currently planned, sources speculate that the 5th generation DDR5 will use a serial interface to eliminate the issues associated with parallel busses. Serial busses are easier to scale up and have fewer connections, making PCB design less demanding.

It seems that every datasheet or reference standard you read on DDR design quotes different allowances for the timing budget. At a basic level, the differential clock is the reference signal for the address/control and command

Parameter	Setup (ps)	Hold (ps)
Open window from simulations	456	631
SDRAM setup and hold times from datasheets	25	100
Slew rate derating if >1V/ns	2.3	2.8
Timing offset with respect to Vref CA	13	11
SDRAM derating	88	50
Crosstalk	47	42
Controller error - skew	200	200
Clock error - jitter	30	30
PCB routing tolerance	10	10
Margin	41	185

Table 1: Example of the overall DDR3-1066 timing budget allowances and resulting margin.

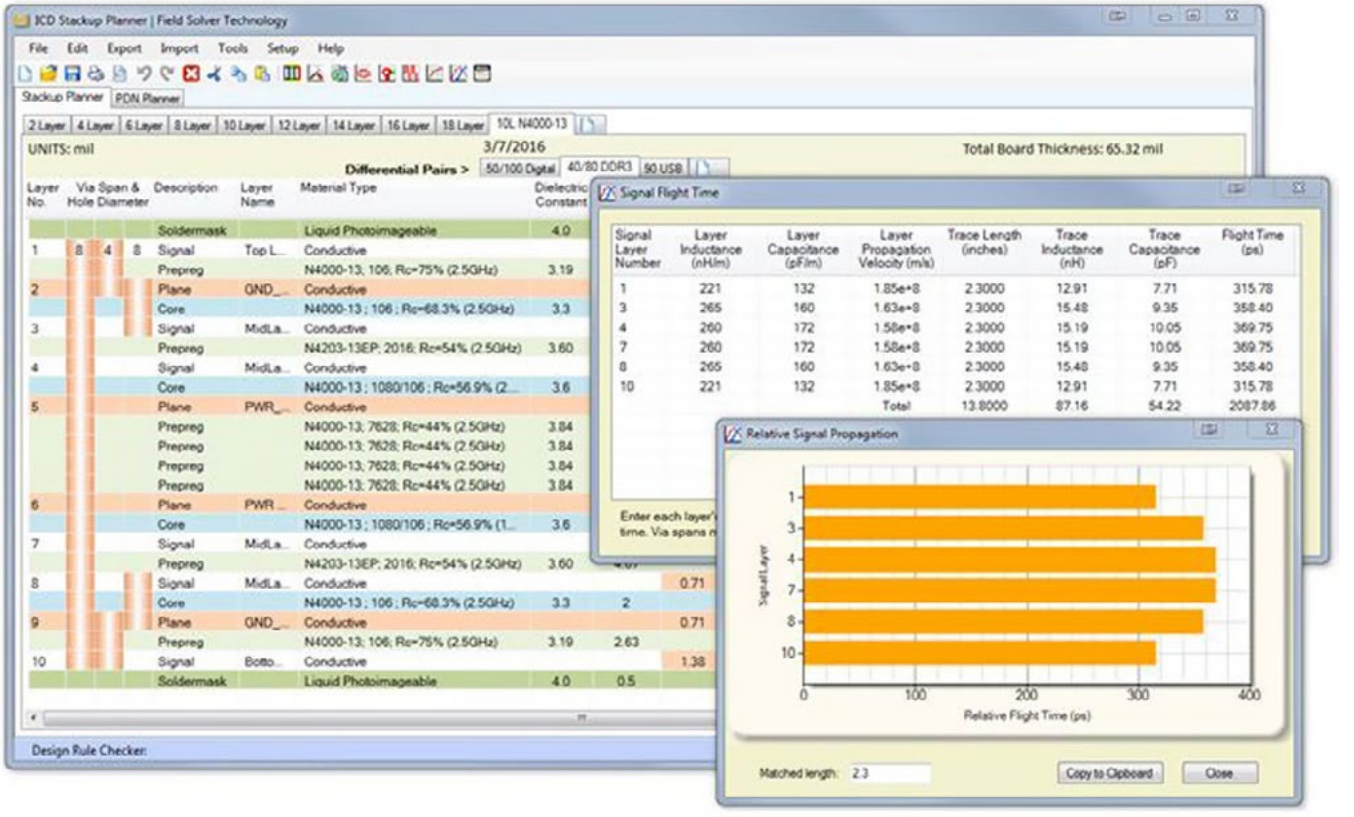

Figure 4: Relative signal propagation for each signal layer on a 10-layer DDR3 stackup.

signals. Whereas, the differential strobe is the clock for the data and data mask signals. The timing budget for the data byte lanes and the address group need to be determined and must be spread across the processor package, PCB interconnect and the SDRAM packages. The portion of the timing budget, consumed by the controller IC and SDRAM devices, is fixed and cannot be influenced by the PCB designer. The amount of timing budget remaining, after subtracting these fixed portions, is all that is left for the board interconnect—which is not much!

For a DDR3-1066 SDRAM for instance, data from the JEDEC, JESD79-3E DDR3 standard specifies 25ps for Setup and 100ps for Hold time as in Table 1. Ideally, one should use a simulation tool, such as HyperLynx, to measure the setup and hold times to ensure they are within the timing budget. However, if you do not have access to an analysis tool, work on 10ps delay, for the routing tolerance, and you can be assured that you are within the margin allowing for any derating. That is, providing the transmission lines are matched to 40/80 ohms single-ended/differential impedance, the correct drive currents are being used and the waveforms are not distorted. Let's face it, it is not that difficult to route each signal to the exact propagation delay given that you have access to each layer's flight time. It is also worth noting that the margin limits can be increased, if the memory interface is not operating at the maximum frequency and/or if a fast memory device is used.

Now let's consider a typical 10-layer DDR3 stackup as in Figure 4. There are six routing layers and all the DDR3 signals are routed to 40/80 single ended/differential impedance and matched to 2.3 inches in length. In my 2014 column Matched Length does not equal Matched Delay, I cited the difference between the propagation delay of the layers on a PCB. The most dramatic is that of microstrip (outer layers) compared to stripline (inner layers). In this case, the delta between

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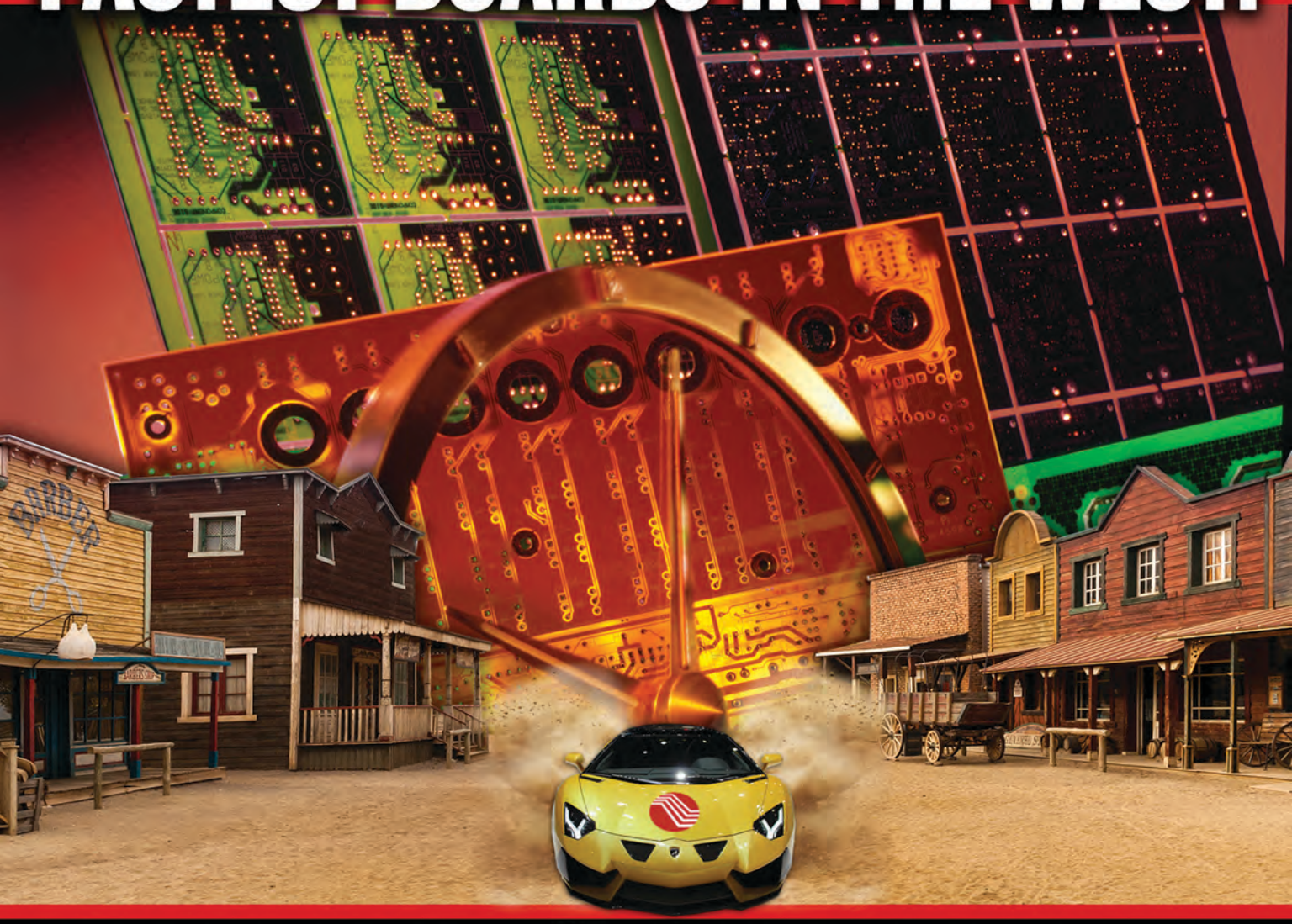

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layers 1 and 4 is a massive 54ps—way outside the setup margin.

Whilst stripline layers 3 and 4 have an 11ps difference, even though they are routed to the same length. This is due to the variance in dielectric constant of each layer which changes the velocity of the signals propagation. The difference is graphically displayed in the ICD Stackup Planner's new Relative Signal Propagation dialog. Even the 11ps stripline variance is more than enough to offset the timing, particularly using high-speed DDR3 and DDR4 devices, regardless of the routing topology.

In conclusion, fly-by topology supports higher frequency operation, reduces simultaneous switching noise, reduces the quantity and length of stubs and consequently improves signal integrity and timing. And, most importantly, from a PCB designer's point of view, it eases routing of memory devices dramatically. However, no matter what topology is implemented, one should pay strict attention to the signal propagation, on each layer, ensuring the total flight time of the critical signals match, regardless of length.

Points to Remember

- Fly-by topology supports higher frequency operation, reduces simultaneous switching noise, reduces the quantity and length of stubs and consequently improves signal integrity and timing.
- The controller must add the write leveling delays to each byte lane to maintain the strobe to clock requirement at the SDRAMs.
- T-topology can be challenging to route but it can be advantageous when using multi-die packages with high capacitance loads. Whereas, fly-by topology eases routing of DDR3/4 devices.
- The double T-topology was used for DDR2 and had a downside in that the impedance discontinuities, due to branching along the traces, caused obvious margin losses.
- With conventional T-topology, the trace stub is lengthened with an increase in number of memory device loads.
- The clock traces should be routed to a longer delay than the strobe traces per byte lane.
- Designing a memory interface is all about timing closure.
- The portion of the timing budget, consumed by the controller IC and SDRAM devices are fixed and cannot be influenced by the PCB designer.
- If you work on 10ps, then you can be assured you are within the margin allowing for any derating.
- The margin limits can be increased, if the memory interface is not operating at the maximum frequency and/or if a fast memory device is used.
- Matched length does not equal matched delay. The most dramatic difference being that of microstrip (outer layers) to stripline (inner layers). **PCBDESIGN**

References

1. Barry Olney's Beyond Design columns: PCB Design Techniques for DDR, DDR2 & DDR3 Parts 1 & 2; Matched Length does not equal Matched Delay

2. JEDEC Specifications JESD 79F, JESD79-2E, JESD79-3F & JESD79-4

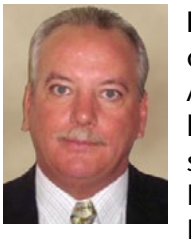
3. The Xilinx Zynq-7000 PCB Design Guide

4. EDN article by Chang Fei Yee: DDR4 memory interface; Solving PCB design challenges

5. Micron's TN-41-08: Design Guide for Two DDR3-1066 UDIMM Systems Introduction

6. The SI List, available at Freelists.org

7. The ICD Stackup and PDN Planner software can be downloaded from www.icd.com.au



Barry Olney is managing director of In-Circuit Design Pty Ltd (ICD), Australia. This PCB design service bureau specializes in board-level simulation, and has developed the ICD Stackup Planner and ICD PDN Planner software. To read past columns, or to contact Olney, click here.

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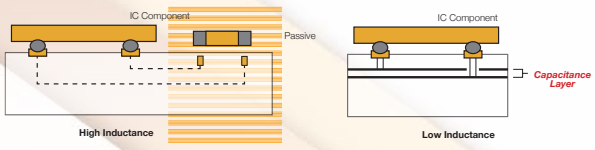

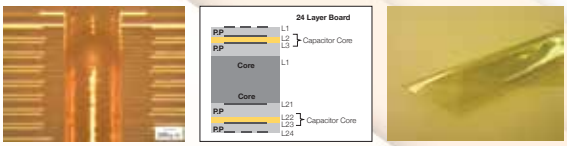

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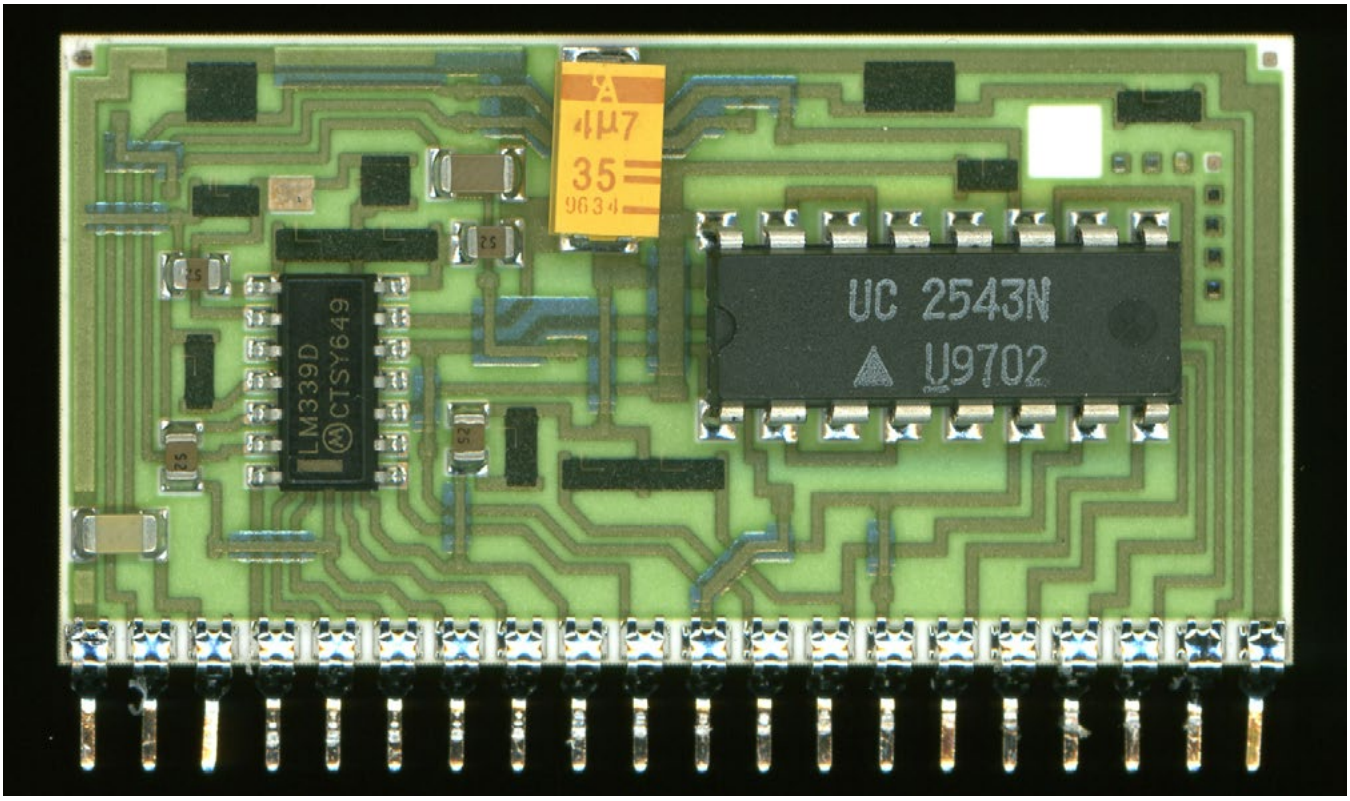
The Basics of Hybrid Design, Part 2

by Tim Haag
INTERCEPT TECHNOLOGY

In the first part of this series, we discussed the basics of hybrid design from the PCB designer's perspective, and here we will continue that discussion. We are seeing more and more of our customers exploring the world of hybrid design, and we are getting new customers for whom hybrid design is their sole focus. The world of hybrid design is growing and we have lots of hybrid specific functionality built into our software that helps designers meet and conquer the unique hybrid design requirements that they are faced with.

And yet many designers out there (and I used to be one of them), have no idea of what is meant when people start talking about hybrid design. It is therefore not uncommon for designers to avoid the subject directly while hoping to pick up little cues and pointers from others indirectly so that they are no longer in the dark. If that description sounds uncomfortably close to where you are, then read on! My hope is that this three-part series will help you by serving as a basic introduction into the world of hybrid design.

If you haven't had a chance to read the first column in this series in last month's issue, please go back and give it a read. To summarize, a hybrid design is an alternate to the standard PCB. Hybrids are generally smaller and more robust than PCBs, making them better suited for extreme environment conditions such as moisture, vibration, or heat. We are focusing the discussion in these columns on LTCC hybrids (low-temperature, co-fired ceramics), although there are other hybrid types as well. Another topic we covered last month was substrate materials and



Example of a hybrid integrated circuit on a ceramic substrate. (Source: Eigener Scan, WikiCommons)

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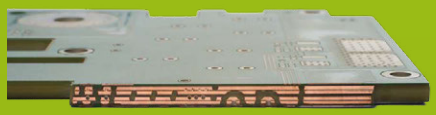

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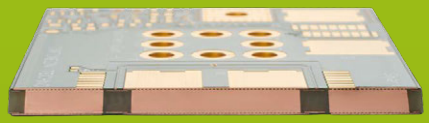

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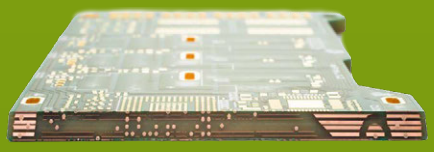

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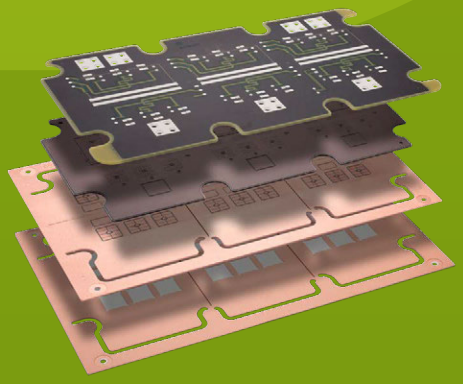

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operating temperatures. We also talked about how hybrids are manufactured using an additive screen print process. This differs from the standard PCB manufacturing process which is a subtractive (copper etching) process. And now, let's press on.

Design software for hybrids is similar to design software for PCBs, albeit with some important differences and enhancements. Due to the differences in fabricating hybrids from regular PCBs (screen printing conductors and dielectric materials onto a substrate instead of compositing separate layers of copper and dielectric material), the need for a specific CAD layer to match a specific board layer does not apply. However, a hybrid design still requires separation between the different conductive and dielectric materials, so the standard method of setting up layers in design software is still the foundation of the design database. Therefore a hybrid design still has layers designated in the layout application, but the names of the layers will be different then what you might see in a PCB layout. Instead of "Top," "Bottom," and "Inner" signal layers, you will instead see layers described as "Metal_Top," "Wire_1," "Wire_2," and "Metal_Bottom." There may also be layers devoted completely to power or ground as in a PCB, but remember that they will be conductive material that is screen printed on instead of being an actual copper layer.

"Design software for hybrids is similar to design software for PCBs, albeit with some important differences and enhancements."

Routing conductors (wires) in a hybrid design on positive layers is done essentially the same way as routing traces in a standard PCB design. The conductors will carry intelligent net information the same way as a trace does in a PCB design, and the CAD application will account for their connectivity and net rule requirements. But instead of only designing layers for connectivity as a PCB would require, a hybrid also requires the design of its dielectric material as well.

Just as in a PCB, hybrid conductors need to be isolated from other conductors that are printed above or below them. And just as in a PCB, a dielectric material is used to provide this insulation. The difference is that in a hybrid the dielectric material will not be an actual composited layer as it would be in a PCB. Instead it will be added by another screen printing process. Once it is in place, screen printing of conductive material can be added on top of it to continue the hybrid buildup.

Solid layers of dielectric material are designed in the CAD application in a similar way to how an area fill or a power plane is designed for a PCB. Therefore the positive area fill or negative power plane algorithms in PCB design software lend themselves well for this, with one exception: They must be enhanced to account for the lack of intelligent net information that they would carry in a PCB. Remember, this is dielectric material which has no need for net information to be assigned to it. The key here for PCB designers is to remember that when you are looking at a hybrid design's dielectric layers in your CAD application, they are not fills or planes even though they may look like what you are traditionally used to seeing as a fill or a plane. And to further complicate matters, there may still be layers in a hybrid design that are devoted to being an actual conductive power fill or plane.

One thing that PCB designers may not be aware of that is very different in hybrid design is the use of crossover dielectric material. As we have discussed, full layers of dielectric material can be designed into a hybrid. But in a hybrid design you may have a situation where there are only a few spots between two adjacent conductor layers where wires are crossing over each other. Obviously these points need to be isolated from each other with dielectric material to keep them from shorting, but to add another layer of full dielectric material for only these

few locations would be unnecessary. Instead, hybrid designers have at their disposal the ability to add crossover dielectric material.

Remember that, although we are using the term "layers" when talking about our CAD application, the actual hybrid design will be fabricated by screen printing material from the bottom up. Therefore if we have shorts in only a couple of locations between two adjacent layers of conductors, we can instead insert a small amount of dielectric material to isolate those shorts in only those specific locations. To do this within our CAD application we will designate a new CAD layer for this dielectric crossover material, but it will only have an image on it in those specific locations where the isolation is needed. When the hybrid design is fabricated, those areas of crossover dielectric material will be screen printed over the wires on the bottom that would otherwise be shorted, and then the next layer of wires will be screen printed over the top of that.

Hybrid design CAD software has built-in routines specifically for generating crossover dielectric areas. These areas will match the area of wires that are shorting together to provide full insulation, and they can be applied manually or generated automatically depending on the needs of the design.

Designing hybrid vias is also significantly different than what most PCB designers will be used to. In a standard PCB design, the board is usually drilled after the layers are composited together. In a hybrid design, however, vias are not drilled. Remember, the hybrid design is built from the substrate up by a screen printing process that prints both conductive material and dielectric material. Therefore vias are created by either screen printing a spot of conductive material, or by not screen printing dielectric material at that same location leaving a void. Because of this, standard drilling files are not needed in a hybrid design as the creation of vias is managed completely by the screen printing processes.

And with that we have reached the end of Part 2 of this series. Today we have discussed the layer structure of a hybrid design and how those layers are managed in a CAD application. We have also discussed how conductive layers and dielectric layers are designed and the unique differences that hybrid design tools need over standard PCB design software for this.

But there is still more to come: components on a hybrid design, wirebonds, and ink resistors. So please look for Part 3 next month. See you then. **PCBDESIGN**

Tim Haag is customer support and training manager for Intercept Technology.

The Automotive Market is Turning Electric

Yole Développement (Yole), the "More than Moore" market research and strategy consulting company, has released the report Power Electronics for EV/HEV 2016: Market, Innovations and Trends. With this new report, the company proposes updated market metrics and forecasts for electrified vehicles and a comprehensive geographical analysis. Yole's analysts highlight the related incentives and deterrents for market growth.

Within its new report, Yole is considering 4 converters in one electric/hybrid electric vehicle. Sales of battery electric cars doubled between 2014 and 2015. Pushed by aggressive targets in terms of CO_2 emissions, electrification is undoubtedly the "greenest" option for car makers, with "diesel-gate" strengthening this impression and improving the public's opinion of electric cars.

Design Tips for Easier Conformal Coating

by Phil Kinner
ELECTROLUBE

Thoughtful design will pay huge dividends down the line, and you will have friends for life among your production colleagues if you make their jobs just that little bit easier! So having started the conversation about the importance of making sound early-stage design decisions, for my third column, let's look at some of the issues that the production department is likely to face when applying conformal coatings.

We'll start with board layout. By the "simple" act of placing connectors and components that must not be coated along one edge of the assembly, the conformal coating application process will be simplified. This might allow dip coating to be explored as a potential alternative methodology, speeding application times and reducing costs. Also, avoid large arrays of discrete components, which can pose a huge coating challenge due to the high levels of capillary forces present. The net result is often areas of no coverage or protection on the board as well as areas of excessive thickness prone to stress-cracking, de-lamination and other coating defects. Similarly, tall components present challenges of their own by the creation of shadowed or hard to reach areas. Splashing is another associated problem. The trick is to avoid placing tall components next to 'must-coat' components in order to avoid this eventuality.

Adhesion results with conformal coatings can vary from supplier to supplier and this can create problems when applying solder resists. A quick and very effective solution to this is by specifying a surface energy of >40 dynes/cm on incoming bare boards and ensuring that each batch is religiously tested and rejected if they do not meet this minimum value.

Conformal coatings are usually liquid when applied, and will flow with a combination of gravity and the capillary forces present. Whether you are masking or relying specifically on selective conformal coating, leaving a buffer of at least 3 mm clear between the area to be coated and uncoated areas will make the production process easier.

That old adage, "If some is good, more is better" doesn't necessarily hold true with conformal coatings, which are designed to be applied at the thickness specified on the datasheet. Exceeding the recommended thickness is unlikely to provide better protection, but may introduce a range of production issues ranging from dramatically increased cycle time to solvent-entrapment, stress-shrinkage, de-lamination and cracking, to name just a few!

If you need to apply a thick coating, two thin coating applications are better than a single thick one. Additionally, if you need more thickness than specified, use a coating that is designed to be applied thickly or consider a resin product.

Conformal coatings should not be used as under-fill materials, as they generally contain no filler and have relatively high Z-axis thermal coefficients of expansion. Make this mistake and you could see the lifetime of ball grid array (BGA) and quad flat no-lead (QFN) terminations

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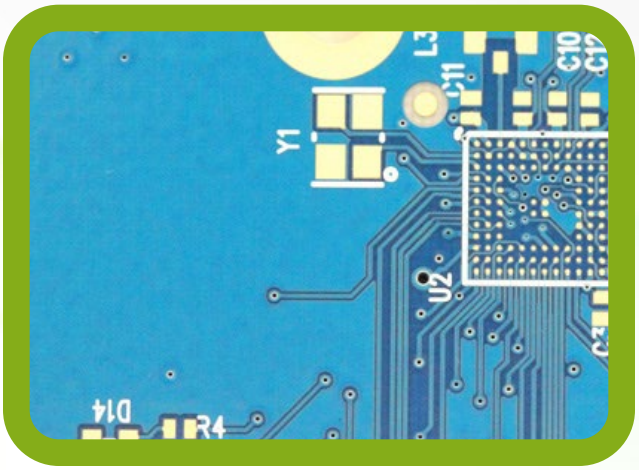

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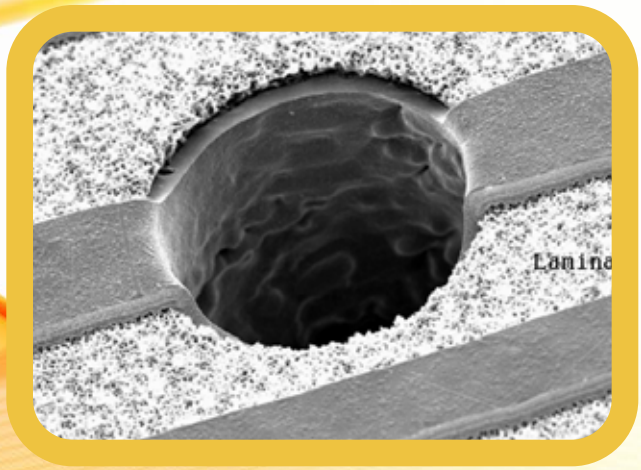

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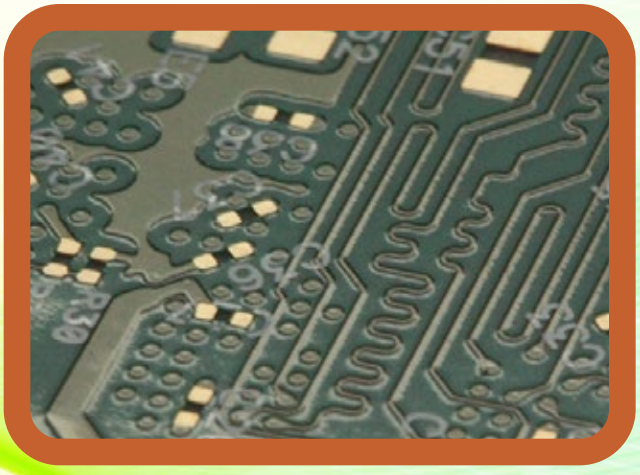

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considerably reduced when exposed to thermal cycling conditions. If you need to under-fill a device, use one of the many under-fill formulations especially designed for this purpose.

To summarize, this month's five top tips for design engineers are as follows:

1. Conformal coatings are not waterproof, but having said that, we have just developed a hydrophobic two-part coating system that is water-resistant. But as a rule of thumb, coatings are NOT waterproof. The housing around the assembly can often act as a water-trap due to condensation and poor drainage. Boards that are conformal-coated and subjected to long-term immersion in condensed water probably won't operate as you might expect. Airflow and drainage are important considerations during the design of the housing.

> **"Boards that are conformal-coated and subjected to long-term immersion in condensed water probably won't operate as you might expect."**

2. Speaking of airflow, coatings can be abraded by particles drawn from the environment by cooling fans. Once the coating is abraded, unprotected parts of the circuit will be vulnerable to high humidity and condensation, which will lead ultimately to failure. If these operating conditions are expected, it is well worth considering the use of a breathable membrane or particulate filter, or choosing a more abrasion resistant coating.

3. The interaction between solder paste, solder mask, fluxes and coatings is not easy to predict and should always be tested for each design. The geometry and thermal profile of assemblies can significantly affect these interactions; just because it worked on the last assembly is no guarantee it will work on the next.

4. Returning to the subject of housings, many boards are qualified without their housings as presumed worst case exposure. However, mechanical fasteners and fixtures in the housing can significantly affect the behaviour of the board during thermal shock or cycling by causing additional stresses on certain areas and changing the expansion and contraction dynamics of the system. Remember: condensation in the housing can lead to worse environmental conditions than testing outside of the housing.

5. Getting liquid coatings to cover sharp edges of components can be difficult. Poorly coated edges, leads etc., can be worse than not coating, due to the formation of "micro environmental hotspots" where the effect of contamination, corrosion and so on will be maximised. Try to avoid the use of high, sharp cut ceramic components in large arrays, since this will increase the difficulty of achieving good coverage through a combination of capillary flow, and the tendency of the coatings to pool. This is particularly true for ceramic capacitors, which are extremely susceptible to corrosion due to the chemicals used in their manufacture.

It is no easy task to choose the correct conformal coating for your product, let alone have confidence that, in applying it, you will have achieved the ultimate goal of protecting your electronics. Conformal coatings are available in many generic types; each has its strengths and weaknesses. Choose the right coating for the intended use and operational environment, rather than one that is used by your subcontractor or qualified on another product line for a different end-use environment. Don't forget: Test your design to ensure that it has sufficient robustness for the intended application.

Look for my next column in the May issue of *The PCB Design Magazine.* **PCBDESIGN**

Phil Kinner joined Electrolube in May 2014 as the technical director for the company's Conformal Coatings Division, which is represented in more than 55 countries across the globe.

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Outsourcing PCB Design: How it can Help

by Mark Tinkler
VISION CIRCUITS

Most of the companies that we work with have in-house PCB design capabilities, and occasionally we encounter a potential customer who asks, "Why do I need to outsource my PCB design if I have in-house resources that do that?"

Even if you have in-house designers, a close look at outsourcing PCB design is definitely warranted if you want to improve time-to-market, product quality and reliability, flexibility, customer satisfaction, or the bottom line.

To be clear, PCB design represents the conversion of electronic schematic diagrams into sets of data that are then used to create fully developed, manufactured, assembled, tested, and qualified printed circuit boards. This total PCB design process is also known as PCB layout.

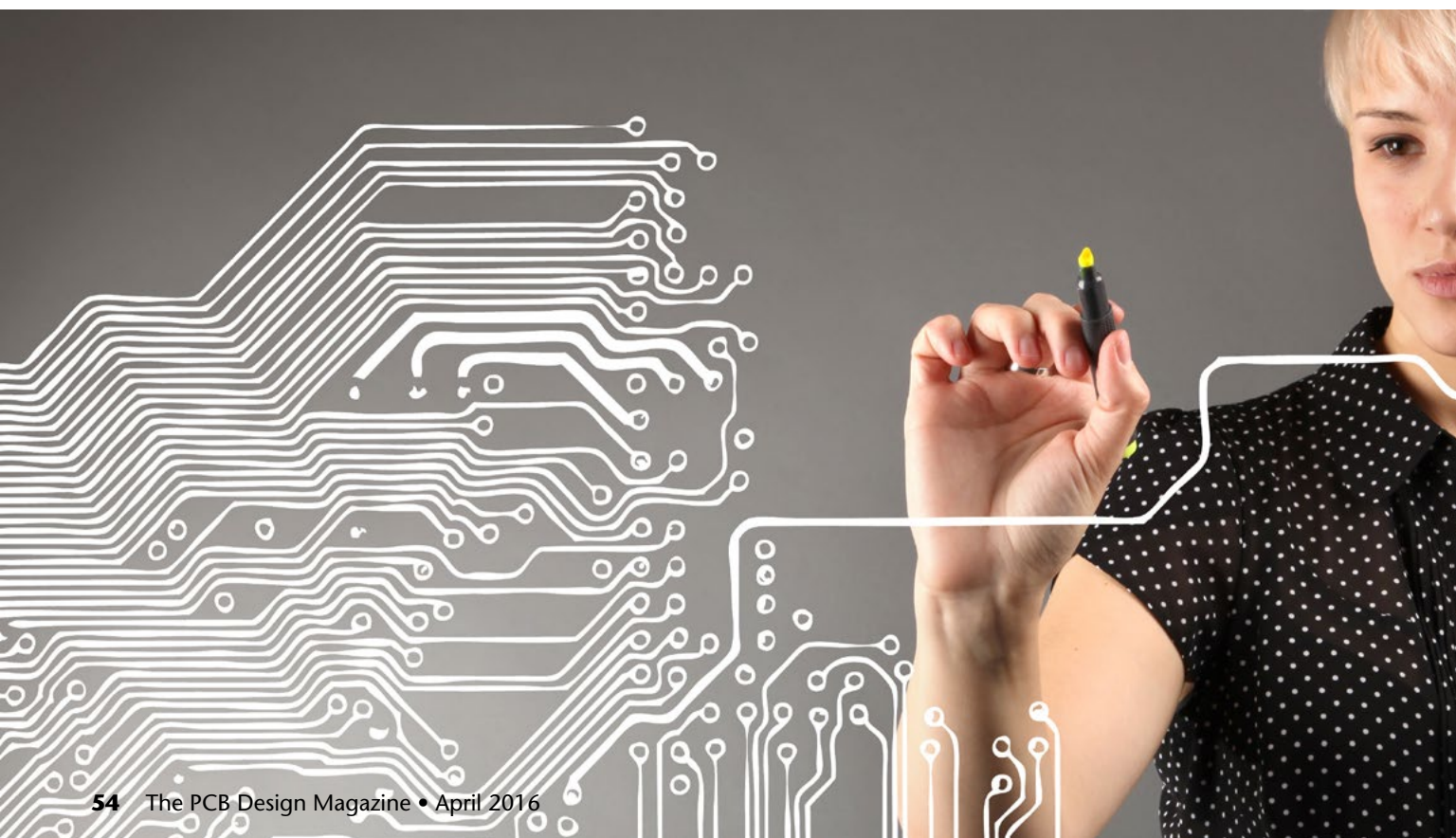
Two key elements must be considered in any improvement: PCB design capacity and PCB design capability.

PCB Design Capacity

Resources: Are you getting the most out of your in-house electronic design talent? Some companies use an electronics design engineer (one who engineers the electronic design and creates the schematic) to also create the PCB design.

By subcontracting the PCB design to a qualified PCB design firm, you can free the electronic design engineer to focus purely on electronic design. By making this change, you will significantly increase the capacity of new product development at your company.

Growth: Is your organization in a growth phase? Do you plan on entering one soon? During a growth phase, companies will hire more PCB design talent to meet the demand. Unfortunately, PCB design talent is then dismissed after the growth phase has plateaued. This is disruptive to an organization and to design professionals.



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Become a member of the OML Community where PCB Assembly industry professionals have FREE full access to the OML specification, white papers written by industry experts, and a place to share ideas in our community forum.

Visit http://www.omlcommunity.com and join the community!

By using a PCB design firm, you will increase your company's flexibility during periods of growth and reduce involuntary employee turnover. By developing a solid partnership with a qualified PCB design firm, you ensure access to ready and reliable PCB design resources when you need them.

Transitions: Change is constant. Some companies move from one design software tool to another, at times driven by PCB design staff/engineering leadership changes. Companies also merge. In these cases, previous PCB designs need to be transitioned to a new common PCB design software tool. Different iterations of PCB design software tools and library data/structures can also exist within a company; in many cases the format and control is questionable. A qualified PCB design firm can help you to close these gaps and will enable your PCB design system to create better products, faster.

PCB Design Capability

Design Software: Some companies fail to realize that PCB design has a huge impact on overall performance, reliability, and cost of finished product. Some PCB designers use low-cost PCB design software tools or older versions of PCB design tools (both have limited capabilities) that will create costly constraints further in the design and manufacturing process.

The best practice is to engage with a qualified PCB design firm that fully uses the latest PCB design software tools and has formed strong relationships with their design software providers. This will benefit all involved, most importantly, your customers.

Collaboration: Improve your in-house capabilities through collaboration. A qualified PCB design firm will help companies improve their PCB design capabilities by working collaboratively with your in-house designers. This is a great resource to have in order to explore and implement best practices or to bounce ideas around. The end result is better PCB design.

Technology Expansion: Is your company specialized in one segment of the industry? Are you looking for the best PCB design practices for a specific industry? Are you expanding into a new technology area? A qualified PCB design firm can help. Work with a PCB design firm that has the depth of experience in many industry segments and technologies for best results.

Library Improvement: Companies can always improve their PCB design libraries. Libraries are the foundational building blocks of any great PCB design. Libraries often are not kept in order or have rogue elements included in them. This often results in challenges in final PCB design quality and translates into manufacturability and reliability issues (and costs) downstream. Look to a solid PCB design firm for best practices and assistance in improving your libraries.

DFM/DFA/DFX: Improve your PCB designs for manufacturability, assembly, test, and overall design excellence. Some companies place this responsibility with downstream entities such as bare PCB manufacturers and assembly shops. Critical design rules and validation/verification elements must be incorporated early in the process and include information integral to the design, manufacturing, and testing processes. Look for a PCB design firm that has great relationships (and active communication) with component manufacturers, bare PCB manufacturers, assembly companies, and testing firms. You will experience improved time-to-market and less overall cost.

Finally, remember that there are caveats to consider when using an outsourced PCB design firm. For your product development process to be a success, the firm must have a great reputation, be trusted, and be strongly aligned with your company.

Keep these tips in mind when sending out your next PCB design. **PCBDESIGN**

Mark Tinkler is in business development and sales with Vision Circuits in Markham, Ontario.

April 7
The Changing Landscape of REACH — Workshop
Herndon, VA USA

April 13
Wisdom Wednesday — for IPC Members ONLY — Webinar

April 18–20
IMPACT Washington, D.C. 2016 — Meeting
Washington, D.C. USA

May 17–19
IPC Reliability Forum — Conference
Dusseldorf, Germany

May 19
Europe Government Regulation Workshop — Workshop
Co-located with IPC Reliability Forum
Dusseldorf, Germany

May 25
Wisdom Wednesday — for IPC Members ONLY — Webinar

June 6
ITI & IPC Conference on Emerging & Critical Environmental Product Requirements — Conference
Boston, MA USA

June 8
ITI & IPC Conference on Emerging & Critical Environmental Product Requirements — Conference
Chicago, IL USA

June 10
ITI & IPC Conference on Emerging & Critical Environmental Product Requirements — Conference
Silicon Valley, CA USA

June 14–15
IPC Manufacturability Forum — Conference
Chicago, IL USA

June 29
Wisdom Wednesday — for IPC Members ONLY — Webinar

July 19–20
IPC Technical Education — Workshop
Chicago, IL USA

July 27
Wisdom Wednesday — for IPC Members ONLY — Webinar

August
IPC Education Online: Summer School — Webinar

August 31
Wisdom Wednesday — for IPC Members ONLY — Webinar

September 21
Wisdom Wednesday — for IPC Members ONLY — Webinar

September 24–30
IPC Fall Committee Meetings — Meeting
Co-located with SMTA International
Rosemont, IL USA

September 26
EMS Management Meeting — Meeting
Rosemont, IL USA

October 19
Wisdom Wednesday — for IPC Members ONLY — Webinar

October 25–27
IPC-SMTA Cleaning and Conformal Coating Conference — Conference
Chicago, IL USA

November
IMPACT Europe 2016 — Meeting
Brussels, Belgium

November 2
PCB Carolina Presented by the RTP Chapter of the IPC Designers Council — Conference and Exhibition
Raleigh, NC USA

November 2–3
IPC Technical Education (in conjunction with PCB Carolina) — Workshop
Raleigh, NC USA

November 7–11
IPC EMS Program Management Training and Certification — Certification
Chicago, IL USA

November 16
Wisdom Wednesday — for IPC Members ONLY — Webinar

December
IPC Education Online: Winter Semester — Webinar

December 7–9
HKPCA International Printed Circuit & IPC APEX South China Fair — Conference and Exhibition
Shenzhen, China

December 14
Wisdom Wednesday — for IPC Members ONLY — Webinar

Questions? Contact IPC registration staff at registration@ipc.org or +1 847-597-2861

What is Signal Launch and Why Should You Care?

by John Coonrod
ROGERS CORPORATION

Signal launch is a term often used to describe how the signal is introduced to the PCB. Many times the signal may be coming to the PCB by a cable and the transition from the cable to the PCB is done through a connector. In the case of RF applications, the cable is typically coaxial and the connector has the same coaxial configuration. The orientation of the electric fields in the connector are different than the orientation of the electric fields in the PCB.

The PCB is a planar structure, and typically the electric fields are perpendicular to the copper planes within the PCB. The fields are generally described as a rectangular coordinate system. In the case of a coaxial structure, the electrical fields are between a center conductor and the surrounding ground sheath. The electric fields are typically described in a cylindrical coordinate system. The interface where the coaxial connector meets the PCB, sometimes referred to as the signal launch, will cause the electric fields to transition from cylindrical orientation to rectangular orientation and this transition can cause many signal integrity issues.

In general, at microwave frequencies well below 3–5 GHz, signal launch is simple with few critical issues arising from time to time. In contrast, signal launch is quite critical as we begin to operate at higher frequencies or high bit data rates. At these higher frequencies/data rates, the signal wavelength is small enough that the connector launch/circuit board trace transition physical dimensions will impact the wave properties as it changes from radial to planar distribution. For example, at 1 GHz the wavelength of the signal on a double-sided PCB using material with a dielectric constant (Dk) of 3 is about 6.8 inches (173 mm). When the signal launch transition is 0.3 inches, the physical dimension is well below 1/8 wavelength (~0.8 inches) which will have an insignificant effect on electromagnetic fields. A general rule of thumb is that a physical dimension at the

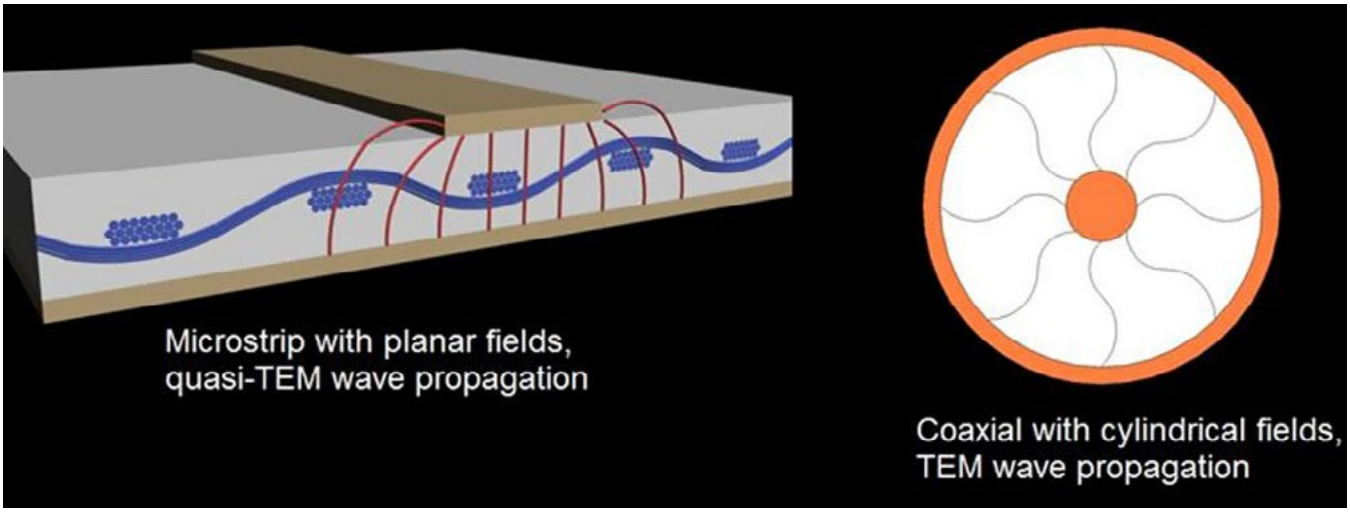

Figure 1: Depiction of electric field orientations for a microstrip double-sided circuit and a coaxial connector.

When failure is not an option, don't leave your high tech PCBs to chance.

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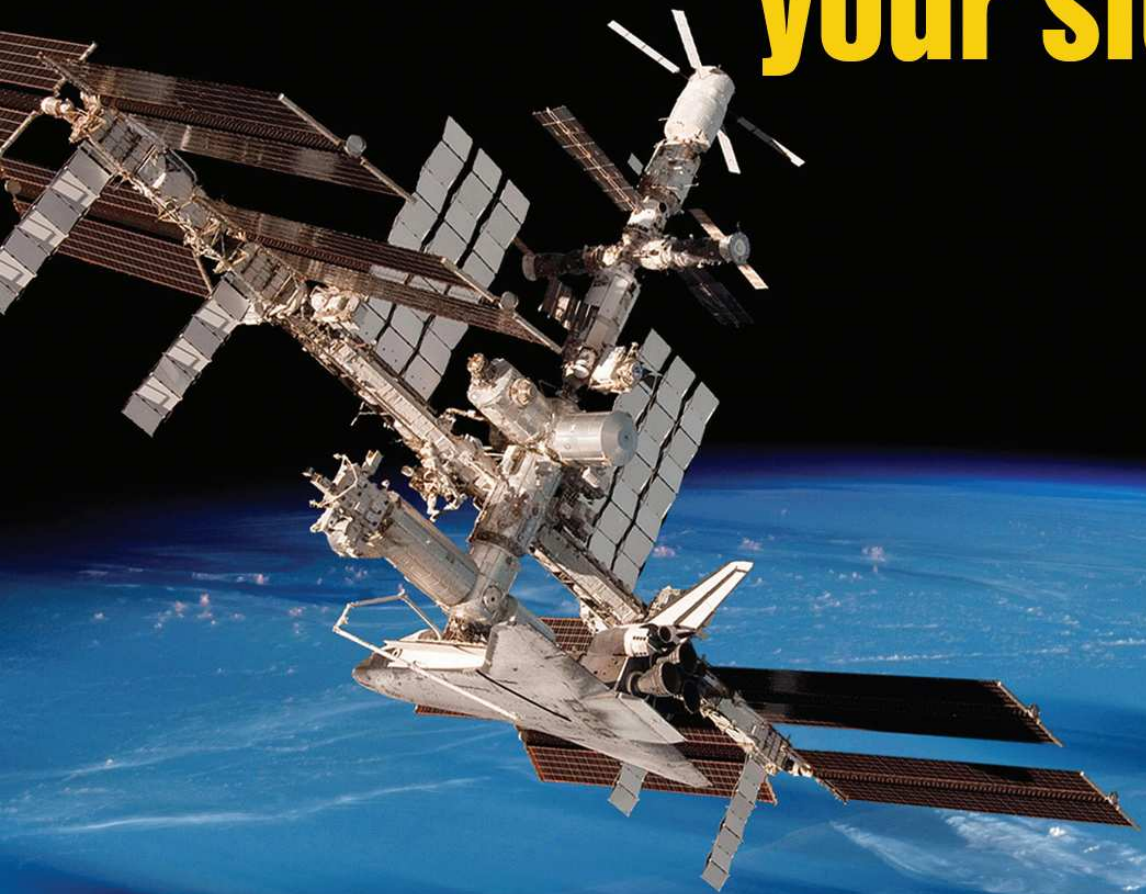

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transition which is 1/8 wavelength or larger can cause signal launch disturbances.

However, for this same example operating at 3 GHz or 5 GHz, the 1/8 wavelength is 2.3 and 1.4 inches, respectively. The 0.3 inch transition is now close to 1/8 to 1/4 inches in dimension, which will have repercussions in the electromagnetic fields at this transition and would need to be compensated for by the RF engineer.

There are several things that can be done regarding the PCB and connector design to minimize the signal launch issue. One of the simplest ways is to use a smaller connector. In the RF industry, there are many different types of connectors and each type has a range of frequencies capable of being used with minimal electromagnetic field disturbances. The range of frequencies at which these connectors are rated are usually based on the connector not having resonances that interfere with the signal integrity, but in general, higher frequency-rated connectors are smaller. To show the relationship between connector size and frequency use, Table 1 lists some common connectors.

When considering the details about signal launch, it can get pretty complicated. The electric field transition from the connector to the PCB will have a change in the ground return path. There are isolated phase velocity differences, small impedance variations, and often there are reflections and radiated energy.

Connector Size	Cutoff Frequency
3.5 mm	34 GHz
2.9 mm	46 GHz
2.4 mm	50 GHz
1.86 mm	67 GHz
1.0 mm	~110 GHz

Table 1. Connector size vs. cutoff frequency.

As more applications are moving to higher frequencies and higher speeds, signal launch is often misunderstood by designers who have worked at lower frequencies or speeds. This can be frustrating and it is recommended that the designer work with both connector and material supplier to try to find an optimized solution for the particular design. **PCBDESIGN**

John Coonrod is a senior market development engineer for Rogers Corporation. To read past columns, or to reach Coonrod, click here.

Survey: Consumers Seeking Higher Value Proposition for Home Internet of Things

Network entertainment applications are the stepping stone to a broader home Internet of Things (IoT) experience, even as consumers remain skeptical of the value proposition behind the home Internet of Things, wary of their cost and uncertain of their utility, according to a recent survey of U.S. consumers by International Data Corporation (IDC).

About 28% of people who own a home network stream online videos to their televisions, and they are much more likely to express high interest in and adoption of home IoT applications than other home network owners.

Moreover, one out of five people who use home automation, monitoring and control devices say their home IoT applications solved a problem they didn't know they had.

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MilAero007 Highlights

FTG Circuits Qualified to MIL-PRF-31032

The FTG Circuits, Chatsworth, California facility has been qualified to the Department of Defense performance specification MIL-PRF-31032/3 (flexible printed wiring boards) and MIL-PRF-31032/4 (flex-rigid printed wiring boards).

API Technologies to be Acquired by PE Firm

API Technologies Corp., a leading provider of high-performance RF, microwave, millimeter-wave, power, and security solutions, announced a definitive agreement providing for the company to be acquired by an affiliate of private equity firm J. F. Lehman & Company (JFLCO), which specializes in the aerospace, maritime and defense industries.

PCi Purchases Polar CITS880s Controlled Impedance Tester

Rigid flex circuit board manufacturer, Printed Circuits Inc., purchased a CITS880 controlled impedance tester from Polar Instruments. Polar Instruments' software and testing equipment is the most popular solution in the PWB manufacturing industry for predicting and verifying controlled impedance circuits in circuit boards.

BAE Systems, Shengyi Receive IPC Corporate Recognition Awards

IPC – Association Connecting Electronics Industries bestowed its highest corporate honors to two member companies, BAE Systems and Shengyi Technology Co. Ltd. During a luncheon at IPC APEX EXPO, the IPC Stan Plzak Corporate Recognition Award was presented to BAE Systems and the IPC Peter Sarmanian Corporate Recognition Award to Shengyi Technology Co. Ltd.

PrecisionHawk Explores Extreme-Weather Testing of Drones at ACE

PrecisionHawk has successfully completed the world's first extreme-weather testing of unmanned aerial vehicles (UAVs) in the ACE climatic wind tunnel at the University of Ontario Institute of Technology (UOIT).

Robots: Eliminating the First Contact with an Enemy Force

"We should be thinking about having a robotic vanguard, particularly for maneuver formations," said Dr. Bob Sadowski. "There's no reason why the first contact with an enemy force should be with a man-platform, because it means that platform is at the greatest risk."

PNC Purchases Universal Pick and Place Equipment

Sam Sangani, president and owner of PNC, has announced that his company recently added a new Universal pick and place machine, model Genesis GI-07, to its fast-growing assembly department.

Configurable Analog Chip Computes with 1,000x Less Power than Digital

Researchers have built and demonstrated a novel configurable computing device that uses 1000x less electrical power—and can be built up to 100 times smaller—than comparable digital floating-gate configurable devices currently in use.

IPC APEX EXPO 2016: Glenn Oliver on His IPC "Best Paper" on High-Frequency Materials

Glenn Oliver of DuPont discusses his award-winning paper, "Round Robin of High-Frequency Test Methods by IPC-D24C Task Group." Co-authors include Jonathan Weldon of DuPont, John Andresakis of Park Electrochemical, Chudy Nwachukwu of Isola, John Coonrod of Rogers Corporation, David L. Wynants of Taconic Advanced Dielectric Division, and Don DeGroot of Connected Community Networks.

Harris Signs Definitive Agreement to Sell Aerostructures Business

Harris Corporation and Albany International Corp. today announced a definitive agreement under which Albany International will acquire Harris' aerostructures business for an enterprise value of $210 million, including $187 million in cash at closing and the assumption of a $23 million capitalized lease.

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SiSoft: Optimizing the State of the Art

Todd Westerhoff, SiSoft

by Andy Shaughnessy

In the 20 years since its founding, SiSoft has been at the forefront of signal integrity analysis tool development. Now, the company is leading the way with a new technology called OptimEye™ and tools for creating accurate IBIS-AMI models. At DesignCon, I caught up with Todd Westerhoff, VP of semiconductor relations, and asked him to give us an update on the company's newest technologies.

***Andy Shaughnessy:** Todd, for anybody who's not familiar with SiSoft, why don't you give us a little bit of background about the company?*

Todd Westerhoff: SiSoft has been focused on system-level signal integrity since 1995, providing both automated signal integrity tools and high-speed design consulting services. We started as a consulting company, using scripts to create an automated methodology to make ourselves more productive. Our customers noticed how quickly we were able to get complicated jobs done and began asking how we did it. It wasn't long before our customers asked us to package those processes and sell them as commercial tools. One of the things that really sets SiSoft apart is that we continually prove our tools through real-world use on customer designs. We design and test everything from the high-speed designer's point of view—how should our software work and what kind of output should it produce?

I know that sounds cliché, but it's incredibly important. I've worked for a number of EDA companies. I have actually been using simulation tools since before the term "EDA" was coined, and I've repeatedly seen that most EDA companies do very little, if any, real work with their own tools. Think about that for a minute. Would you buy a car from a company where no one drove their own brand? Would you eat at a restaurant if none of the staff would eat there? Yet, that's exactly what many customers do: buy EDA tools from companies that have almost no practical experience using those tools in real world situations. SiSoft has been built on the business model that I have always believed EDA companies should use: collaborat-

ing with leading-edge customers to develop and prove new capabilities on working projects before bringing those capabilities to market. We use our own software on complex real-world applications every day, because that's how you make products great. Anyone can come up with a canned demo that makes their software look good, but creating software that works well day-in and day-out on real world problems is another thing entirely.

***Shaughnessy:** You have a couple of new things you're showing here at DesignCon. Why don't you tell us about what's new at SiSoft?*

Westerhoff: We're introducing a new technology called OptimEye that automatically co-optimizes transmitter and receiver settings in AMI simulations to maximize eye height. This lets users replace the hundreds or thousands of "blind sweep" simulations they use to figure out equalization settings today with a single OptimEye run.

***Shaughnessy:** Is this kind of capability new to the industry?*

Westerhoff: EDA simulation tools have had different types of optimization capabilities before, but none of them have ever been specifically designed for SerDes equalization. When people talk about a simulation tool having an "optimizer," they're typically talking about a generic set of algorithms that vary a set of control inputs to affect some output, or goal. Those algorithms run different simulations to determine how different settings affect the output and then attempt to adjust the control inputs to achieve some goal. But—and here's the important point—those generic algorithms don't really have any understanding of the technology they're trying to optimize. They approach every problem the same way, with no application knowledge.

SerDes links and AMI analysis, however, represent a very specific class of problem. If you focus on how signals propagate from a SerDes transmitter to a receiver and how equalization affects those signals, you can do a much better job of developing algorithms that will address that specific problem. This is what SiSoft has done with OptimEye: developed a new co-optimization technology specifically targeted at IBIS-AMI simulations. This technology is something that SiSoft has been working on for a long time, and OptimEye is actually the third generation of that technology.

***Shaughnessy:** What design problem does it solve?*

Westerhoff: Designers need to determine which combination of Tx and Rx equalization settings produces the biggest eye in the receiver. That's true in both AMI simulation and in the lab with actual hardware. Even though many receivers have a "full automatic" mode where they determine the best Rx settings based on the incoming signal, transmitter equalization is still something that the user needs to program. And, as it turns out, determining optimal Tx settings,

"Even for a moderately complex Tx, the number of combinations can be 200 or more. So aside from trying each possible combination in sequence, how do you choose?"

even with a fully automatic receiver, isn't that simple. Even for a moderately complex Tx, the number of combinations can be 200 or more. So aside from trying each possible combination in sequence, how do you choose? There's a definite science to how you select the set of transmitter settings that will give you the best performance out of the receiver, but it requires a detailed understanding of the transmitter's equalization capabilities, the receiver's equalization capabilities and the characteristics of the serial channel. Evaluating the tradeoffs gets complicated quickly.

So what a lot of designers do is just try as many combinations of Tx settings as possible,

then pick the best one. When that process is done with simulation, it's something we call a "blind sweep". So, for example, if we have a Tx with 3 taps that have 10 settings each, that's 1,000 combinations. So, for each channel they want to optimize, users run 1,000 different simulations and pick the one that gives them the best results.

***Shaughnessy:** That seems like a lot of simulation to optimize just one channel.*

Westerhoff: Absolutely, but that's really just scratching the surface, because no one has just one channel or runs simulations just once. In fairness, people usually don't analyze all combinations of settings, because all those simulations would take too long and there are a number of combinations that can be ruled out anyway. But, even if you reduced those 1,000 combinations down to 100, you still have to multiply those 100 simulations by the number of channels you need to equalize and the number of design changes that require re-running the analysis. And thus, the number of simulations required across the design cycle climbs into the tens or hundreds of thousands pretty quickly and that's the problem to be solved.

Those simulations consume a lot of time and compute cycles today using blind sweep methods. I ran a case study for a customer the other day, where optimizing Tx settings for one channel involved 1,120 simulations and 624 CPU-hours (26 CPU-days) – and that was just for one uncoupled channel. If we can replace those 1,120 simulations with a single OptimEye simulation run, there's an enormous savings there. Even if that one OptimEye run takes 10 times as long as one of those 1,120 blind sweep runs, that's still a savings of about 100 to 1.

***Shaughnessy:** So, how does OptimEye work?*

Westerhoff: OptimEye is an application-specific technology that combines three key things to determine the best combination of equalization settings: simulation results using the vendor's actual IBIS-AMI models, information about the equalization capabilities of the specific SerDes Tx/Rx, and knowledge of IBIS-AMI models and IBIS-AMI simulation methodologies

OptimEye is able to take a set of simulation results using baseline Tx/Rx settings and determine whether or not those results are optimal. If they are not, OptimEye predicts what the best settings would be and re-runs the analysis to see if the vendor models behave as predicted. If not, OptimEye adjusts its prediction and the process iterates until it converges. One of the best parts of this technology is that the SerDes vendors don't have to rewrite their models for OptimEye to work with them—a separate control file describes the SerDes device so that OptimEye can predict the best settings and run simulations using the vendor model to verify those predictions. There's more to how this works than I can describe here, but readers can go to our website to get more information about how OptimEye works and watch videos on the subject.

"OptimEye is able to take a set of simulation results using baseline Tx/Rx settings and determine whether or not those results are optimal."

***Shaughnessy:** I saw that you're also presenting a paper with MathWorks on creating IBIS-AMI models. What's that about?*

Westerhoff: We're presenting methods for leveraging SerDes data for AMI model generation. This has long been considered the Holy Grail of IBIS-AMI model development, being able to take the schematics and code created during SerDes design and use them to generate IBIS-

AMI models without having to modify the design data in any substantial way.

Too often what happens with IBIS-AMI models is that the model development only takes place after the SerDes design is done and the glue is dry. The IBIS-AMI model developer has to create a model that describes the SerDes behavior by literally redeveloping it from scratch.

It's not a development process; it's a redevelopment process in the classical sense. The question has always been, "Can we take a snapshot of the current SerDes design at any point in the design process, and without rewriting it, use it to generate C code and make AMI models?" What we're presenting with MathWorks is exactly that, using the combination of Simulink and MATLAB code that are characteristic of SerDes design to generate IBIS-AMI model code. The generated code is compliant with the IBIS-AMI interface and runs in commercial IBIS-AMI simulators.

There are a number of interesting things that now begin to happen. You can say at some intermediate point in the SerDes design cycle, "Let's give this model to some key customers to see if it's going to work for them." This gives you the ability to take critical SerDes design decisions and find out if they are going to work on the types of channels your customers are designing in their next generation systems. Normally, the only way you know that is by building silicon and giving it to a customer, but by then it's too late to do anything about it.

If we reduce the effort needed to create an AMI model down to the point where SerDes designers can create AMI models in real time during the active SerDes design cycle, it becomes possible to give intermediate models to customers, who can say whether that design will work for them. If it won't work, those same customers can use that intermediate model to identify what changes are needed—more taps, different adaptation loop bandwidth, or whatever it happens to be. That, we think, is a game-changer.

One other key point in developing good AMI models (an AMI model always has two parts): an analog part that models insertion and return loss, and an algorithmic part that models equalization and clock recovery. You need to design the two parts of the AMI model so they work together to produce the correct overall result. We see too many AMI models where everything has been put in the algorithmic model, and the analog component is "idealized" with an ideal resistance and no capacitance. That's just wrong—there's no way a simulator can correctly predict reflections and ringing if the analog model doesn't correctly reflect the silicon impedance. It comes down to this: If you don't get the analog model right, you don't get the insertion loss and return loss right. If you don't get those right, you don't get ISI right. If you don't get ISI right, you don't get the waveforms right, and you don't get the eye diagram right. That's the knock-on effect of not handling the analog model properly.

The flow that we put together with MathWorks basically ensures that your analog model is correct as you start building the algorithmic behavior, and allows you to refine both of them over time. They're always being evaluated together, so the combined model is going to work correctly. You're going to have the right analog behavior, you're going to have the right algorithmic behavior, and the two of them together are going to give you the right model. We think it's a big deal just because we know how many AMI models we've gotten from other people where the analog part is compromised and has affected the simulation results.

***Shaughnessy:** Well, that sounds really promising. Todd, thanks so much for sharing this with us today.*

Westerhoff: Thank you, Andy. **PCBDESIGN**

FURTHER READING

1. To attend the webinar "A SerDes Balancing Act: Co-Optimizing TX and RX Equalization Settings to Maximize Margin," click here.

2. For more information on OptimEye, click here.

3. For an OptimEye evaluation request, click here.

4. To downloand the technical paper "New SI Techniques for Large System Performance Tuning," click here.

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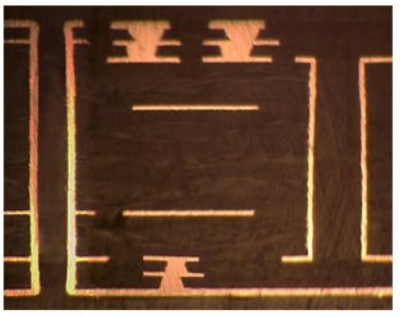
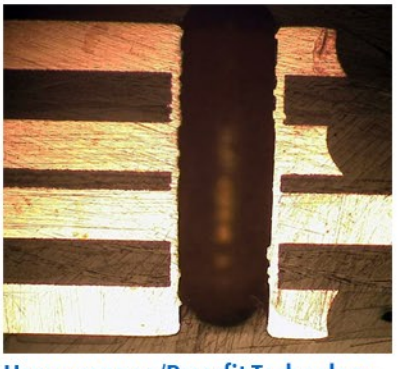
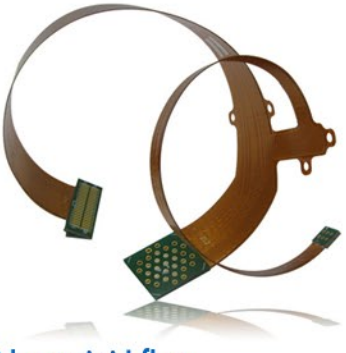


Blind/Buried/Stack via technology



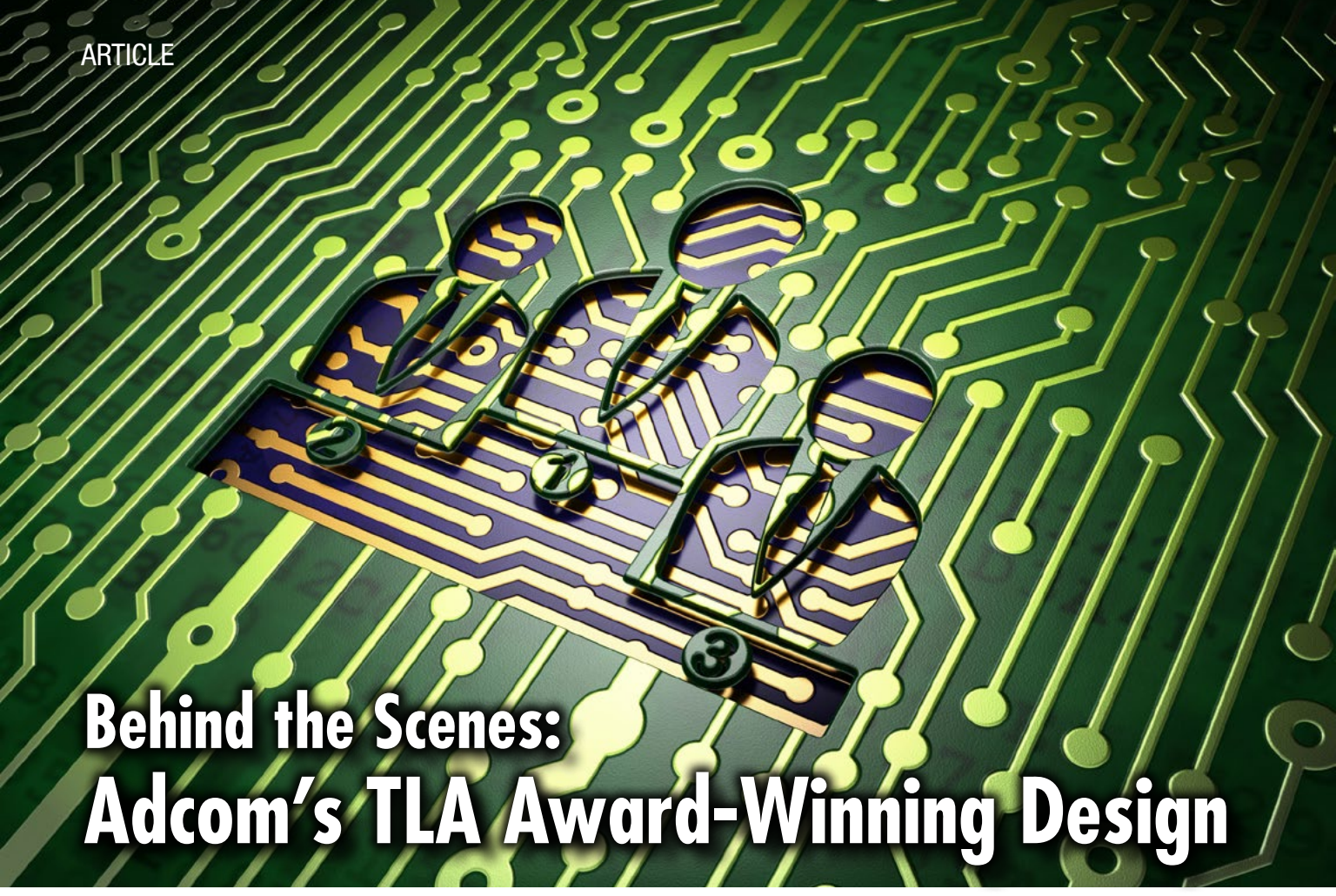
Heavy copper /Pressfit Technology

Multi-layered aluminum board
lead-free HAL



8 layer rigid-flex
30mm flexible finished thickness

UL IPC RoHS



Behind the Scenes: Adcom's TLA Award-Winning Design

by Ruth Kastner
ADCOM

Many of you are familiar with Mentor Graphics' Technology Leadership Award program. Adcom's design team placed first in this year's TLA program, taking the top spot for the category of "Computers, Blade & Servers, Memory Systems." This article will focus on the development of that board.

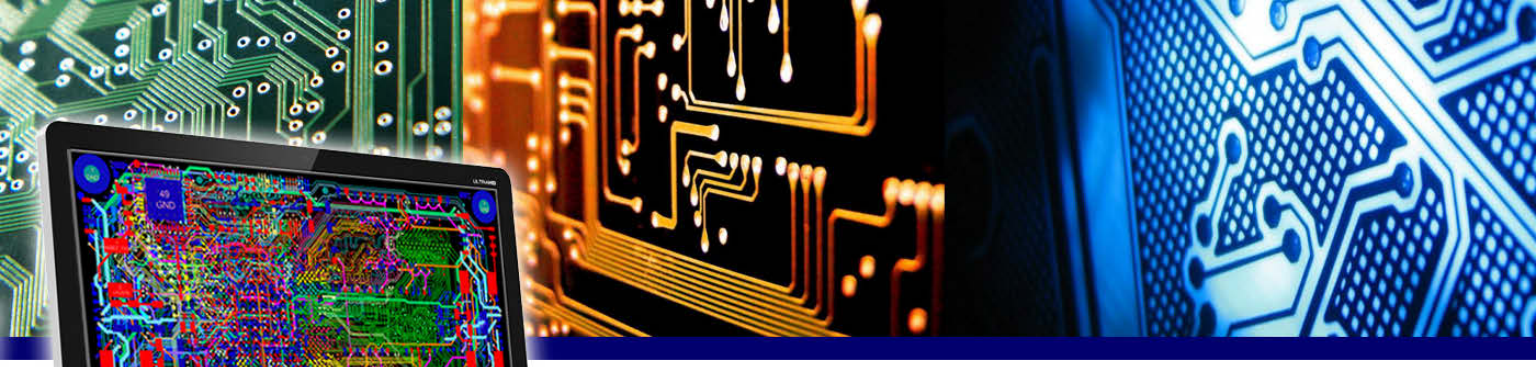
This board, like most PCBs today, is a complex system designed by a multi-disciplinary team of designers, striving to bring an operational product to the market on schedule. In the case reported here, the deadline for a fabricated feasibility board was set to eight months. Within this time frame, the team had to design a product complying with demanding specs, such as the Arria 10 FPGA, PCIe 3.0, Hybrid Memory Cube (HMC) and Avago MicroPOD, as well as complying with IPC class 2 manufacturing standards.

Challenges arrived in many forms. For example, as data transfer rates are continually increasing, PCIe now runs at 8GHz. Also, operating IC voltages are lower and power requirements for various components are higher. More challenges lay in the form of small form factor of ICs and high-speed transceiver protocols. All of this requires advanced PCB fabrication technologies. The design teams need to work in union over a short design-cycle time, and provide early proof of concept. The work flow should incorporate the processes of modeling, optimization and analysis.

The outcome of this process was the delivery of an almost flawless feasibility board on the first shot. There was no need for a second version, thanks to the effort invested in overall simulation at the design and layout phase.

Requirements Implemented in Design Flow

This board was developed as a proof of concept for a very high-density data processing unit using high-speed memories and interfaces. Components included a 20 nm FPGA, advanced memory devices such as DDR4 and HMC transceivers of 15Gbps, 10Gbps and 8Gbps, and power circuits, all connected to a PCIe device. The area provided for the design was 200 mm X



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200 mm with PCB thickness limited to 1.6 mm.

The major design challenges that had to be tackled were the 100A current consumption of the FPGA core, the routing of 16 HMC transceivers operating at 15GHz, and the clock tree design for optimal frequency programmability.

The design team included one FPGA designer, one librarian, three PCB designers, two layout designers, and a mechanical designer (outsourced).

Xpedition Enterprise was used for board design. The simulation tools used throughout the design phase were Hyperlynx SI, due to their ability to simulate all high speed PCI-Gen3 transceiver channels. For simulations of the optical fiber MicroPOD channels, we used IBIS-AMI channel analysis models. We entered the fast transceivers' constraints into the CES. Package delay was calculated to match all DDR4 to net groups on the PCB. Power integrity simulations were used to verify the PDN structure as designed and to recalculate all required capacitance values. Thermal analysis was done off premises and in parallel to the design.

Component Selection

All active components used in the design were either engineering samples or new ones at the upmost updated level of technology available off the shelf. Out of several challenges, the two outstanding ones were also in conflict with each other. The first one involved the incoming power from a 12V ATX external PS which had to generate a large variety of sensitive programmable power supplies on board. In total, we had to distribute 100A to the FPGA core, resulting in a desire for many power layers in the design and stack-up.

The second challenge involved the HMC's smallest BGA pitch of 0.65 mm. This small BGA pitch required microvias of 0.41 mm pad, a 0.2 mm hole, and capping requirements that were in contrast to the requirement to use as many power layers as possible. In between, there were also additional parts such as DDR4 2166MHz devices connected to the FPGA core, an HMC memory Gen2 part and optical fibers of 12 lanes to the FPGA. The requirement for very strict and precise power-up and power-down sequences and monitoring features led us to choose Linear Technology modules as a solution.

The PCB Stackup

Following the design, the next phase is implementation. To this end, we contacted about five PCB manufacturers in order to find one that

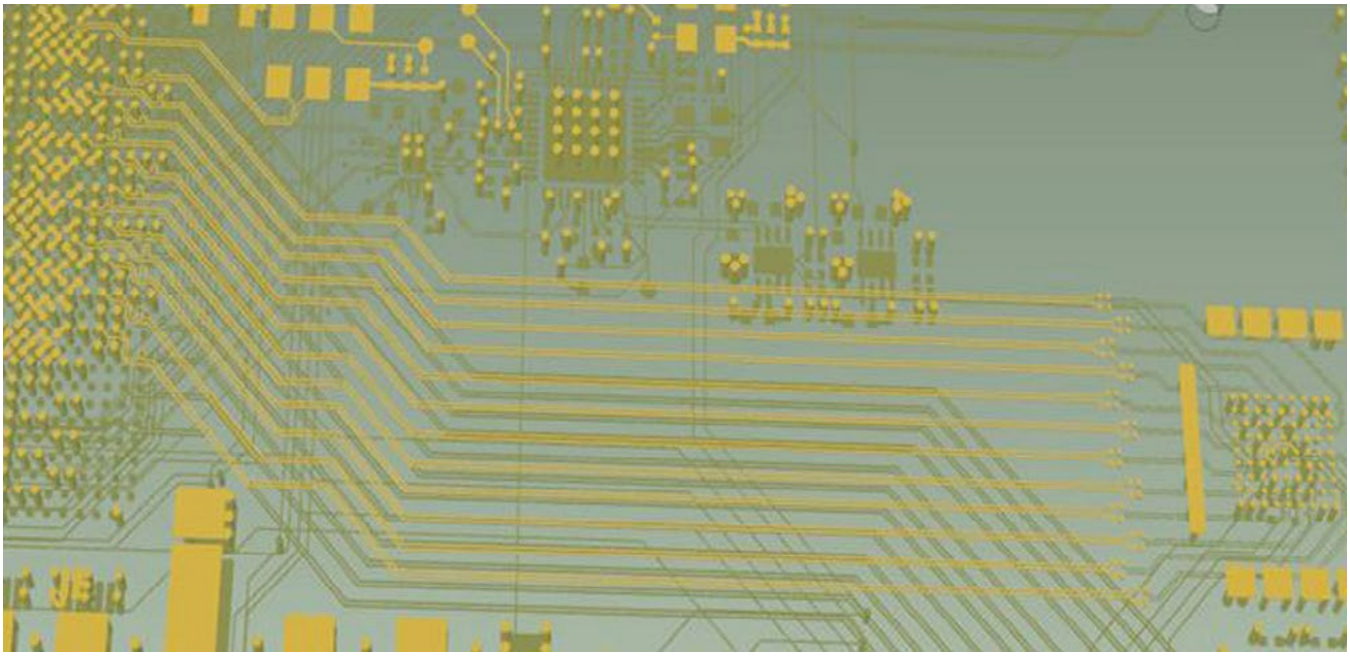

Figure 1: A MicroPOD transceiver.

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Board Types: Single-sided, Double-sided, M ltilayer, Flex, Rigid-Flex, Other: Microwave, etal Core

Mfg Volumes: Prototype, Small, Medium, Larg

C Assembly, CAD, Consulting, Desig Quick turn-around, R&D, Stencils, er: ircuit Design, Product Design

ind/buried vias, Backplanes, Bonded s, rbon contacts, Edge plating, Filled/pl s, avy copper, Printed Electronics, RF, T d PCBs, Thermal management

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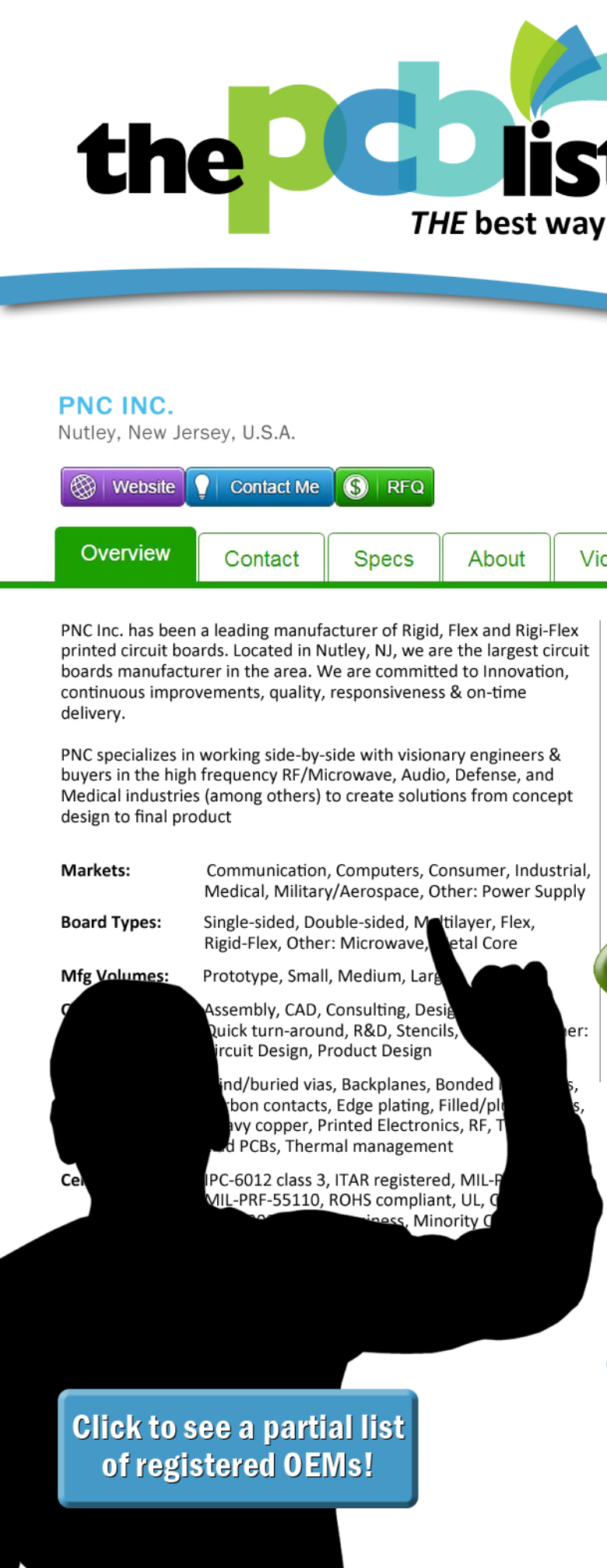

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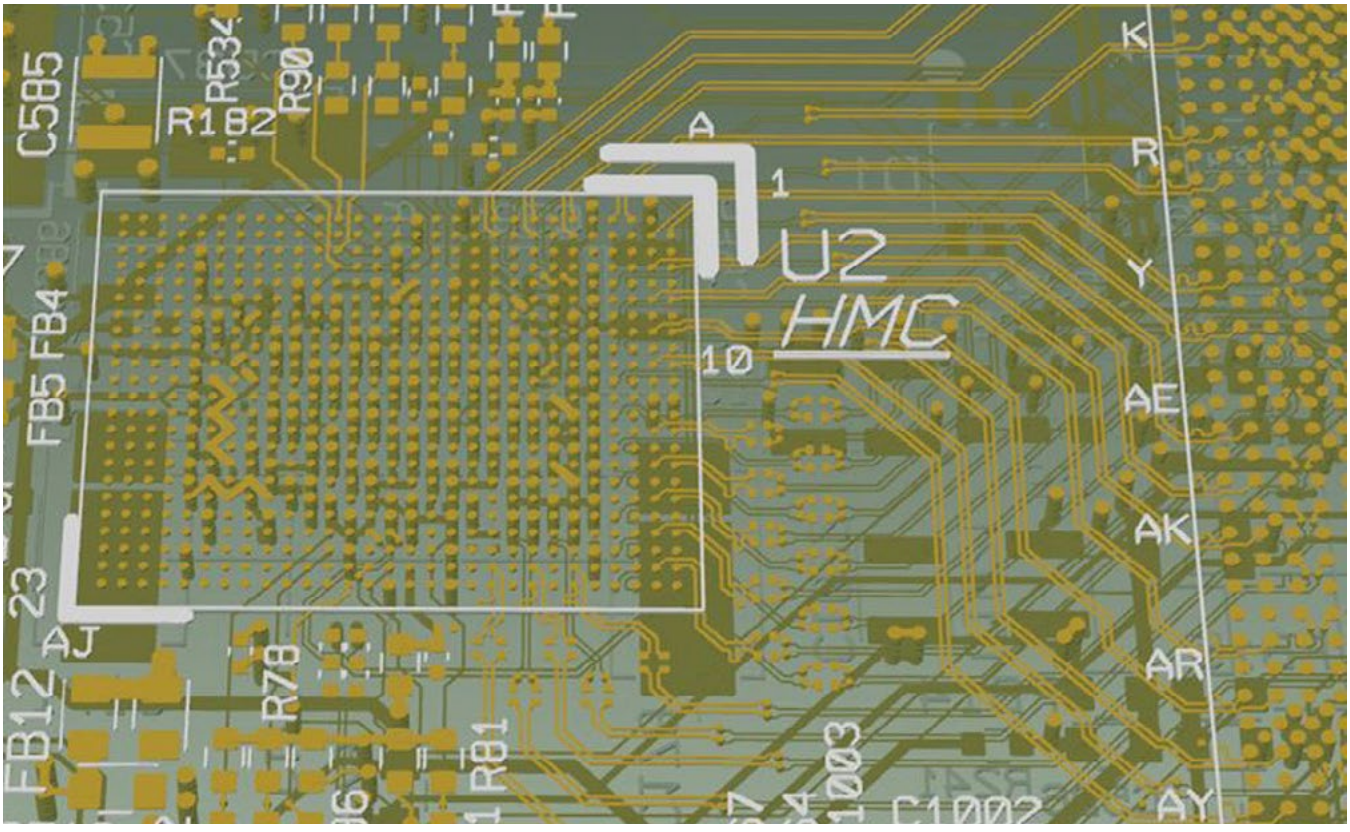


Figure 2: An HMC transceiver.

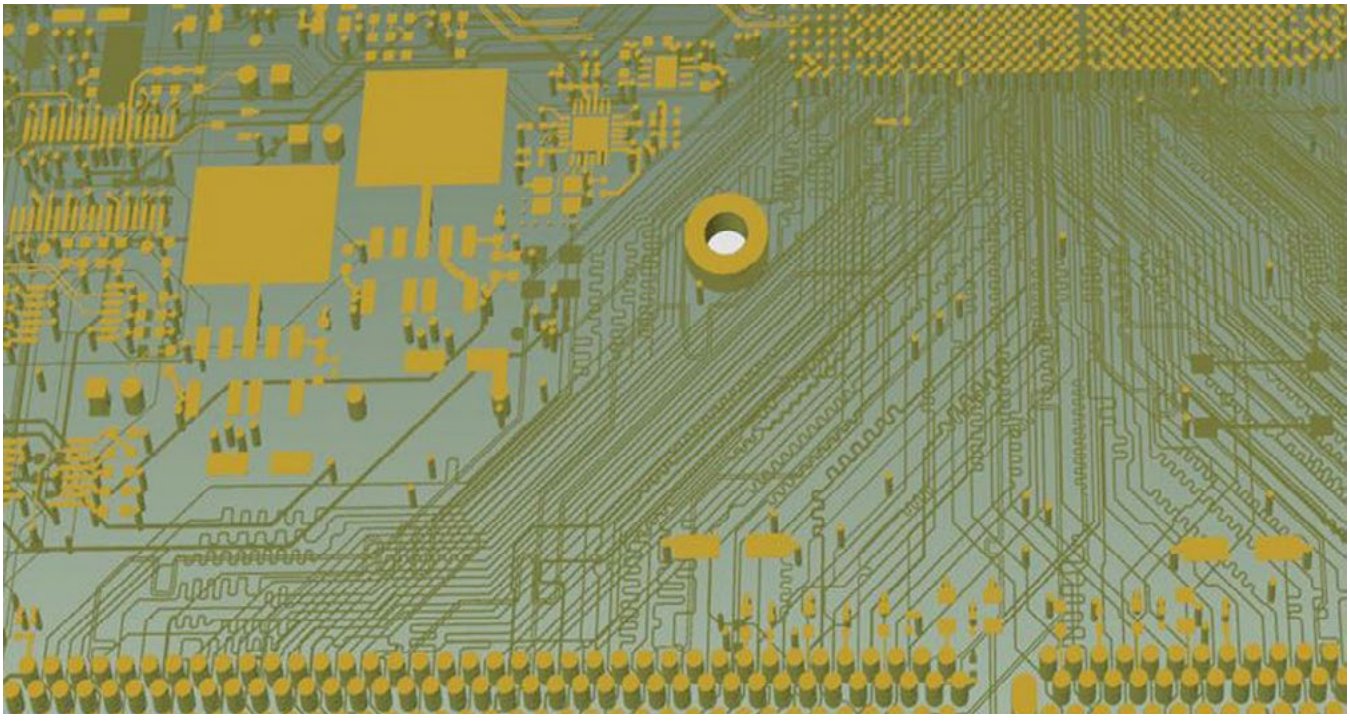


Figure 3: DDR4 on the subject board.

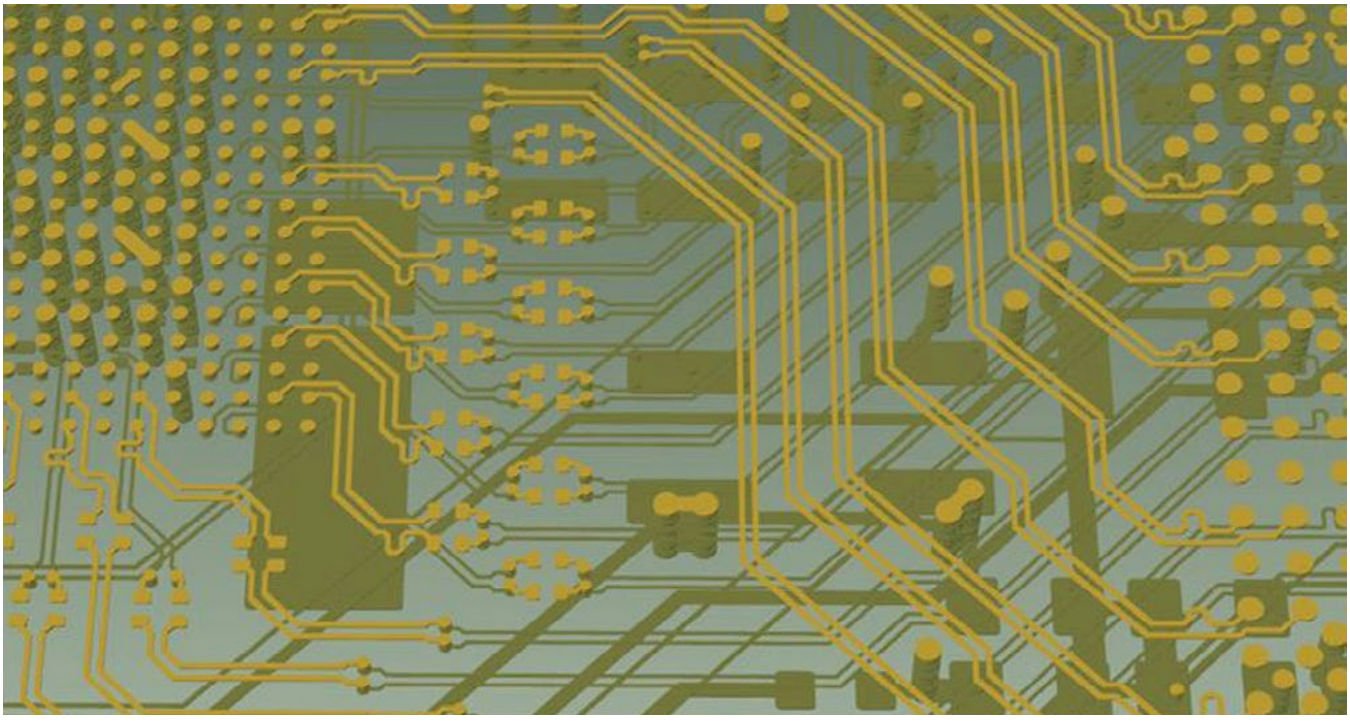


Figure 4: HMC layer, top view.

could fill all of our needs. The three most important criteria for selecting the manufacturer were their ability to support the 100A FPGA core requirement, to support the smallest device pitch of 0.65 mm microvias and capping, and to build good capacitance into the board. At Adcom, we believe in embedded capacitance.

Together with the PDN impedance requirement of 0.5 mohm, we calculated and implemented 1 ounce and 1 mil thickness. The manufacturer was selected, and a stable stackup with Megtron6, DuPont HK04, and HP-Gould performance foil materials was established and implemented.

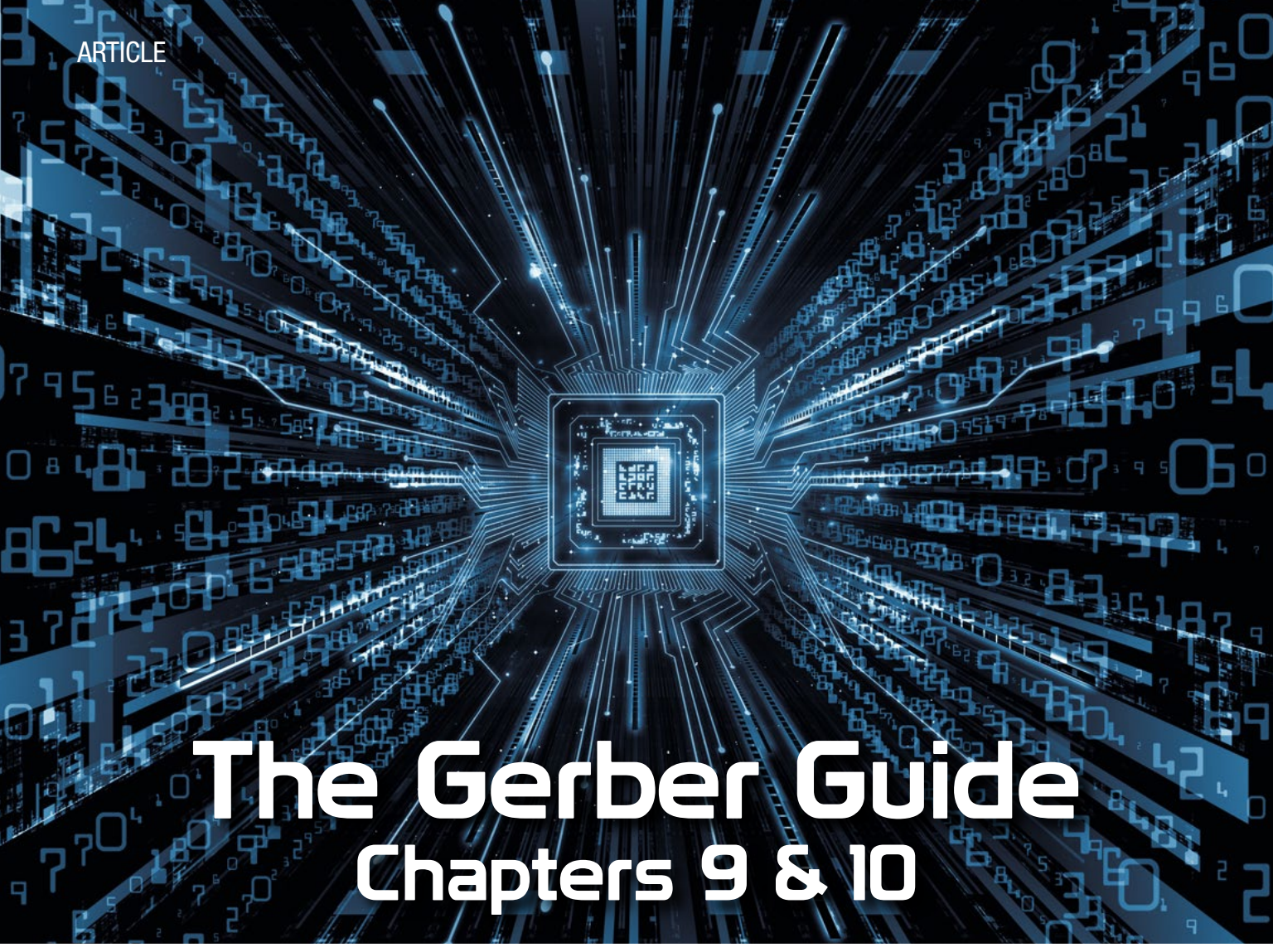
The Test Flow

The final phase in this feasibility project was test and integration. Here, we verified, validated, measured, and analyzed the performance. To this end, a test suit was built and scripts were written. First, we tested a board only with power supplies to confirm their sequence correctness, and then the clocks for frequency, duty cycles and jitter. After verifying their functionality and programming sequences, we assembled the main components and started the bring-up phase. The CPLD loaded, and I2C interfaces were tested first, then the transceivers, followed by the FPGA, memory devices, MicroPOD and finally a load test for the FPGA device was implemented.

Summary

Being a Mentor Graphics Technology Leadership Award nominee is good, but being a winner is even better. Recognition for Adcom came just in time, while we were starting the next best design for 2016. The TLA contest gave us the opportunity to present our PCB design team's work to the rest of the design community. **PCBDESIGN**

Ruth Kastner is COO of Adcom Ltd., specializing in PCB design and manufacturability, new technologies and new materials.



The Gerber Guide
Chapters 9 & 10

by Karel Tavernier
UCAMCO

It is possible to fabricate PCBs from the fabrication data sets currently being used; it's being done innumerable times every day all over the globe. But is it being done in an efficient, reliable, automated and standardized manner? At this moment in time, the honest answer is no, because there is plenty of room for improvement in the way in which PCB fabrication data is currently transferred from design to fabrication.

This is not about the Gerber format, which is used for more than 90% of the world's PCB production.There are very rarely problems with Gerber files themselves; they allow images to be transferred without a hitch. In fact, the Gerber format is part of the solution, given that it is the most reliable option in this field. The problems actually lie in which images are transferred, how the format is used and, more often, in how it is not used.

Each month we look at a different aspect of the design to fabrication data transfer process. In this monthly column, Karel Tavernier explains in detail how to use the newly revised Gerber data format to communicate with your fabrication partners clearly and simply, using an unequivocal yet versatile language that enables you and them to get the very best out of your design data.

Chapter 9: Drawings are no Substitute for Data

Drawings may be a useful part of a PCB fabrication data set, but they are no substitute for digital data. There must be a digital data file for each pattern in the PCB: copper layers, drill-and-route files, solder masks, legends, peelables and whatever other patterned layers are present.

For example adding a drill map may be useful but it is not a substitute for a proper drill file. Drilling is done with a CNC drill machine,

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—David Dibble

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which needs CNC data that has been generated by CAM. If the fabricator only has a drill map, how do you expect him to generate the drill data? Visually, by measuring the drill map on an XY table and typing in the coordinates?

Another example is the excellent profile drawing in Figure1. This drawing defines and illustrates the profile perfectly. The profile drawing may still be useful as a check, but it does not replace digital data specifying the profile, which can be read in automatically (see Chapter 3 in this series). Note that while the drawing does not specify the exact position of the profile with regard to the copper layout, profile digital data does.

Remember, drawings are no substitute for digital data.

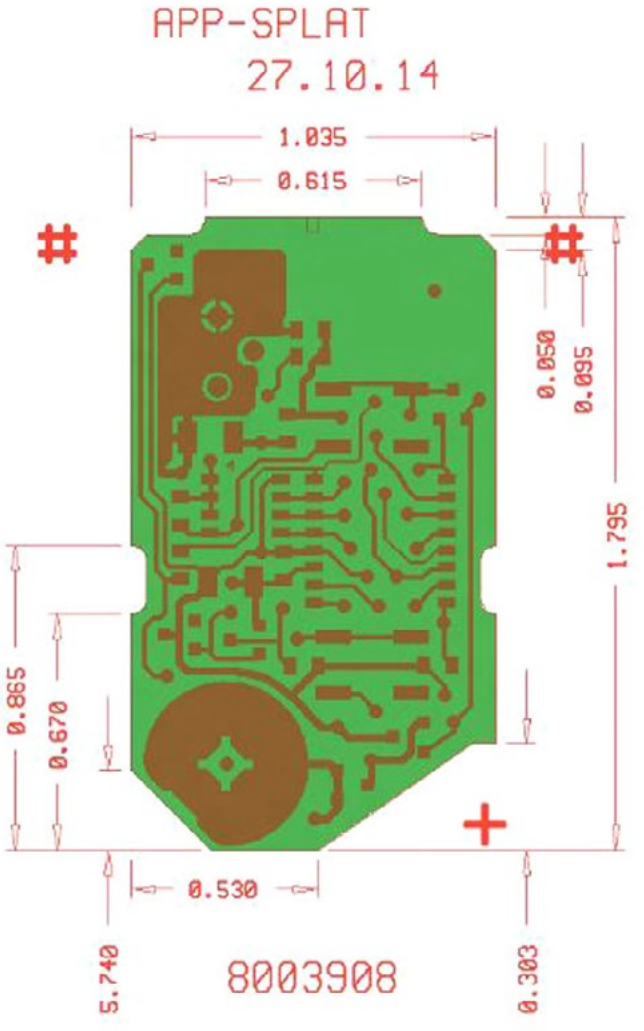


Figure 1: A profile drawing.

Chapter 10: Use only the Gerber Format for your Image Data

Keep data formats to a minimum, using only those that are truly needed. Every extra format used adds output and input processing requirements and increases the risk of bugs and version problems. Mixing formats also increases the risk of misalignment between files (see Chapter 2 in this series).

Copper layers must be expressed in Gerber, so Gerber is a given. Consequently, what can reasonably be expressed in Gerber must be expressed in Gerber.

Drawings are images, so they can—and must—be transferred in Gerber. Other formats are often used for drawings: PDF, HPGL, DXF, DWG etc. These may be fine formats, and DPF is definitely a first-rate data exchange format, but for PCB fabrication data drawings, Gerber is the better choice: Your fabricator needs to read your drawings into his Gerber-capable CAM system to relate it to, and shed light on, the image data—which is, after all, the very reason why you sent the drawings at all. His CAM system is definitely proficient in handling Gerber data but it was not designed to handle other formats. So, although PDF may be a better choice for other workflows, Gerber is the format for drawings in the PCB workflow.

Avoid complicated formats such as DXF and DWG like the plague. You cannot expect your professional CAM operator, who is highly skilled in the Gerber format, to have access to, and be familiar with, the high-end professional software that would be necessary to handle such formats. Simpler software is often of mixed quality, and not safe or reliable enough to faithfully transfer your professional work.

Definitely do not use DXF or DWG for data files such as copper layers. These formats were neither designed for, nor suitable for, PCB data. Indeed, such files are loathed by CAM operators.

In fact, the number of formats needed is very limited. Copper, drill, rout, solder mask, legend must all be expressed in Gerber, and so must the drawings. The netlist cannot be expressed in Gerber, IPC-D-356A must be used. The informal data intended for human eyes—delivery

info, for example, can be expressed in plain text or PDF files. More formal data is expressed in structured text files such as CSV, XML or YAML. Consequently the only formats you need are:

- Gerber
- IPC-D-356A
- Text files
- PDF, possibly

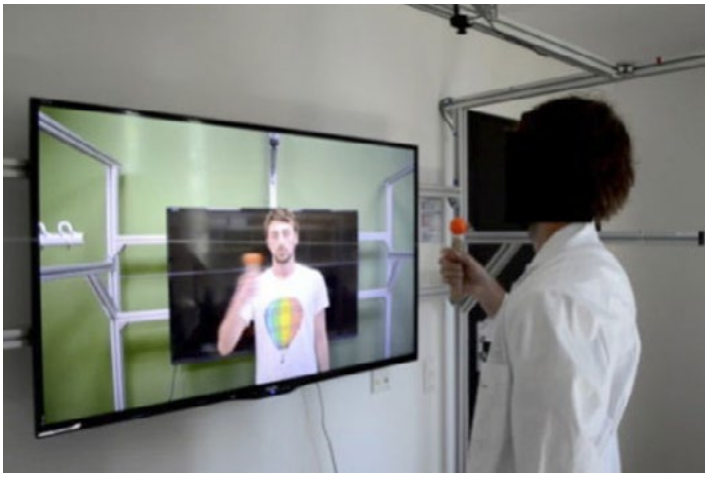
Always output all your drawings in Gerber.

This column has been excerpted from the Guide to PCB Fabrication Data: Design to Fabrication Data Transfer. **PCBDESIGN**

Karel Tavernier is the managing director of Ucamco.

Humanoid Robotics and Computer Avatars

A collaborative research team has found humanoid robotics and computer avatars could help rehabilitate people suffering from social disorders such as schizophrenia or social phobia. It is thanks to the theory of similarity, which suggests that it is easier to interact socially with someone who looks, behaves or moves like us.



Researchers from the University of Bristol, in collaboration with colleagues at the Universities of Exeter, Montpellier and Naples Federico II, have developed a system to enable a robot or computer avatar to interact with a patient whilst playing a version of the mirror game, in which two players try to copy each other's motion whilst playing with coloured balls that can move horizontally on a string.

The paper, part of the EU-funded AlterEgo project, is published in the Journal of the Royal Society Interface.

Initially the avatar is like an alter ego, created to look and move like the patient to enhance his or her feelings of attachment. Over time the avatar is slowly altered to become less similar, therefore helping with social rehabilitation.

The results show that players sharing similar movement features, or motor signature, interact and co-ordinate better. This can be used for rehabilitation of patients with serious social disorders as an avatar can be created to act like an alter ego, programmed to look and move like the patient to enhance his or her feelings of attachment.

Mario di Bernardo, Professor of Nonlinear Systems and Control from the Department of Engineering Mathematics at the University of Bristol, said: "It is very challenging to build an avatar that is intelligent enough to synchronise its motion with a human player, but our initial results are very exciting."

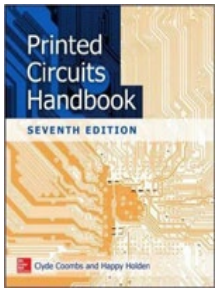
The research used the principles of dynamical systems and feedback control theory to embed the avatar with enough 'intelligence' to synchronise and respond to the motion of the human player.

The researchers now wish to build on the technology and set-up multiple human-machine interaction for social rehabilitation and make groups of people and avatars interact with each other to perform joint tasks together.

TOP TEN

Recent Highlights from PCBDesign007

1 'Printed Circuits Handbook' Features New Chapter by Andy Shaughnessy



The seventh edition of the Printed Circuits Handbook is now available, with a new chapter by Andy Shaughnessy, managing editor of The PCB Design Magazine and PCBDesign007. Edited by Clyde F. Coombs and Happy Holden, this marks the most comprehensive edition of the book to date.

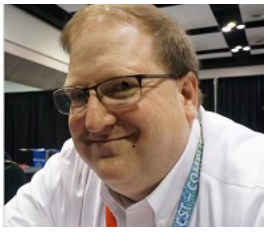
2 IPC APEX EXPO: Gary Carter on First Board Manufactured With IPC-2581B

Gary Carter, senior manager of CAD engineering for Fujitsu Network Communications, discusses the first board fabricated and assembled using IPC-2581B. This 20-layer board features 21,000 component pins and 15,000 holes, with controlled impedance on all layers. He also gave a presentation on IPC-2581B during the Design Forum.

3 Mentor Graphics Releases Newest HyperLynx

Mentor Graphics has announced its newest HyperLynx release, which integrates signal and power integrity analysis, 3D electromagnetic solving, and fast rule checking into a single unified environment. This product for the first time offers designers a complete set of analysis technology sufficient for designing any type of high-speed digital PCB.

4 IPC APEX EXPO: Glenn Oliver on His IPC 'Best Paper' on High-Frequency Materials



Glenn Oliver of DuPont discusses his award-winning paper, "Round Robin of High-Frequency Test Methods by IPC-D24C Task Group." Co-authors include Jonathan Weldon of DuPont, John Andresakis of Park Electrochemical, Chudy Nwachukwu of Isola, John Coonrod of Rogers Corporation, David L. Wynants of Taconic Advanced Dielectric Division, and Don DeGroot of Connected Community Networks.

5 Altium to Release Integrated Documentation Solution for Altium Designer

Altium is scheduled to release a new documentation workflow available exclusively in their flagship PCB design platform, Altium Designer 16.1. Draftsman provides PCB designers with a unified documentation solution with customizable drawing views, documentation templates, and a fully complete design to documentation workflow in Altium Designer 16.1.

6 Mark Thompson: It's All about Communication

In engineering support at Prototron Circuits, Mark Thompson has seen it all. He ensures that each design is manufactured the way the designer intended, even if the CAD data is not crystal clear. Barry Matties and Andy Shaughnessy talked with Thompson about why communication is paramount when designing and prototyping boards.

7 IPC APEX EXPO: Electrolube to Educate PCB Designers on Coatings

Columnist Phil Kinner, technical director of coatings for Electrolube, discusses a paper on condensation testing that he presented at IPC APEX EXPO, and his company's plans to educate PCB designers about conformal coatings to help them avoid problems during manufacturing.

8 EDA Industry Revenue Down 1.9% in Q415; PCB/MCM Drops 6.2%

According to the EDA Consortium (EDAC) Market Statistics Service, EDA industry revenue declined 1.9% for Q4 2015 to $2.06 billion, compared to $2.10 billion in Q4 2014. But PCB/MCM revenue dropped 6.2% during the same period. The four-quarters moving average, which compares the most recent four quarters to the prior four quarters, increased by 5%.

9 IPC APEX EXPO: Hofer Discusses the Pros and Cons of Backdrilling

General Manager James Hofer of Accurate Circuit Engineering discusses the process of backdrilling vias, including the benefits and drawbacks. Backdrilling can improve signal integrity, but it can create stubs that may act as unwanted antennas.

10 Beyond Design: Faster than a Speeding Bullet

In optical communications, electrons don't carry the signal—photons do. And we all know that photons travel at the speed of light. So surely, optical fibers must transmit information much faster than copper wires or traces on a multilayer PCB? Actually, photons and electrons transmit data at the same speed. The limiting factor is the relative permittivity (dielectric constant) of the medium in which the signal propagates.

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Events

For the IPC Calendar of Events, click here.

For the SMTA Calendar of Events, click here.

For a complete listing, check out The PCB Design Magazine's event calendar.

Thailand PCB Expo 2016
April 19–22, 2016
Bangkok, Thailand

Tehnici de Interconectare in Electronica (TIE) 2016
April 20–23, 2016
Suceava, Romania

KPCA-KIEP Show 2016
April 26–28, 2016
KINTEX, Gyeonggi-do, S. Korea

JPCA Show 2016
June 1–3, 2016
Tokyo Big Sight
Tokyo, Japan

IPCA EXPO 2016
August 18–20, 2016
Delhi, India

IPC Fall Meetings
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