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I-Connect007

DESIGN007 MAGAZINE

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Manufacturing Know-how

This month, we asked our expert contributors to share their thoughts on the absolute "must-know" aspects of fab, assembly and test that all designers should understand. In the end, we're all in this together.

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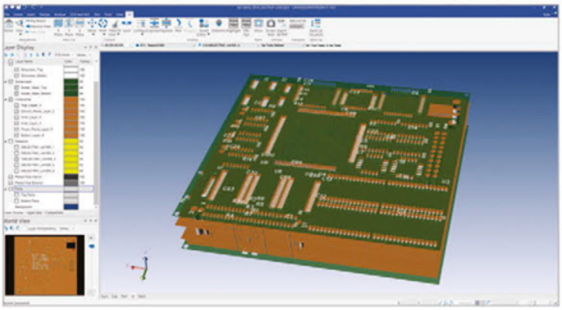

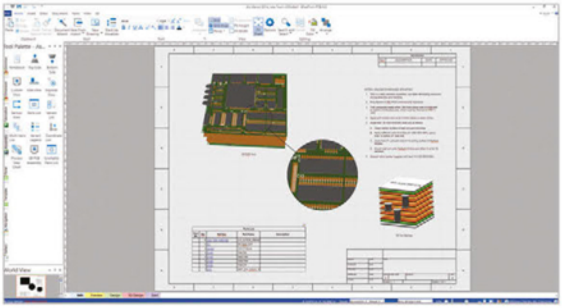

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Pulling Together

The Shaughnessy Report

by Andy Shaughnessy, I-CONNECT007

Our cover image for this month's issue is a great representation of the PCB development process: Design, fabrication, and assembly are all beautifully intertwined. All three disciplines must be integrated to have a successful end product. As a result, all these stakeholders need to know something about the other stakeholders' processes.

The axiom, "We're all in this together," comes to mind.

But designers, sitting at the front end of the entire development cycle, must have more than a passing understanding of the processes downstream from them. PCB designers and design engineers need to know quite a bit about the chemical and mechanical processes taking place after data handoff to design a circuit board that can survive manufacturing stresses and be used by the end customer. Designers should be

well versed in fab and assembly processes just to do their jobs.

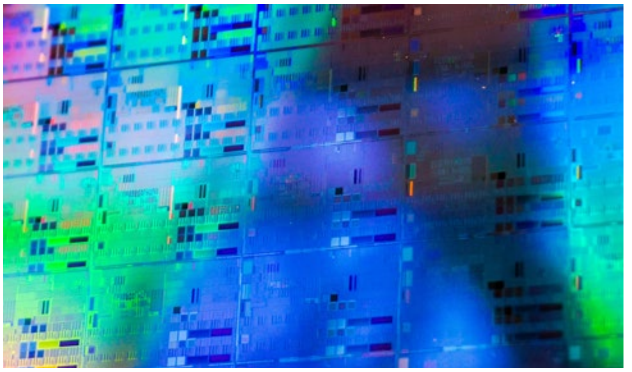
As our contributors often point out, designers really are the first step in the manufacturing process, not a separate, standalone entity. Designers and design engineers have a lot of responsibilities; they wield the power to affect change, good or bad, in the manufacturing process. Some analysts estimate that 70% of the cost of the final board is determined during the design cycle. That's a lot of responsibility for designers.

Many design for manufacturing (DFM) issues can be avoided if designers communicate with their fabrication and assembly providers before and during the design cycle. But designers often operate in a vacuum; they may have no idea where their board is being prototyped, much less where it's going for volume production. So, designers need to arm themselves with as much knowledge about fab and assembly as they possibly can.

This month, we asked our expert contributors to share their thoughts on the absolute "must-know" aspects of fab, assembly, and test that all designers should understand. We have interviews with APCT's Tony Bell, Summit Interconnect's Laura Martin, The Test Connection's Bert Horner, and Aster Technologies' Dean Poplett. We also have a feature article by Lea Maurel of ICAPE Group, and feature columns by Vern Solberg, Tim Haag, Istvan Novak, and Martyn Gaudion. You'll also find regular columns by Matt Stevenson and Joe Fjelstad.

The new year is here, and trade show season is upon us. In the next few months, we'll be covering DesignCon and IPC APEX EXPO. I hope to see you all on the road. DESIGN007

Andy Shaughnessy is managing editor of *Design007 Magazine*. He has been covering PCB design for 23 years. To read past columns, click here.



Earthquake Temporarily Halts Silicon Wafer, MLCC, and Semiconductor Facilities in Japan

TrendForce's investigation into the impact of the recent strong earthquake in the Noto region of Ishikawa Prefecture, Japan, reveals that several key semiconductor-related facilities are located within the affected area.

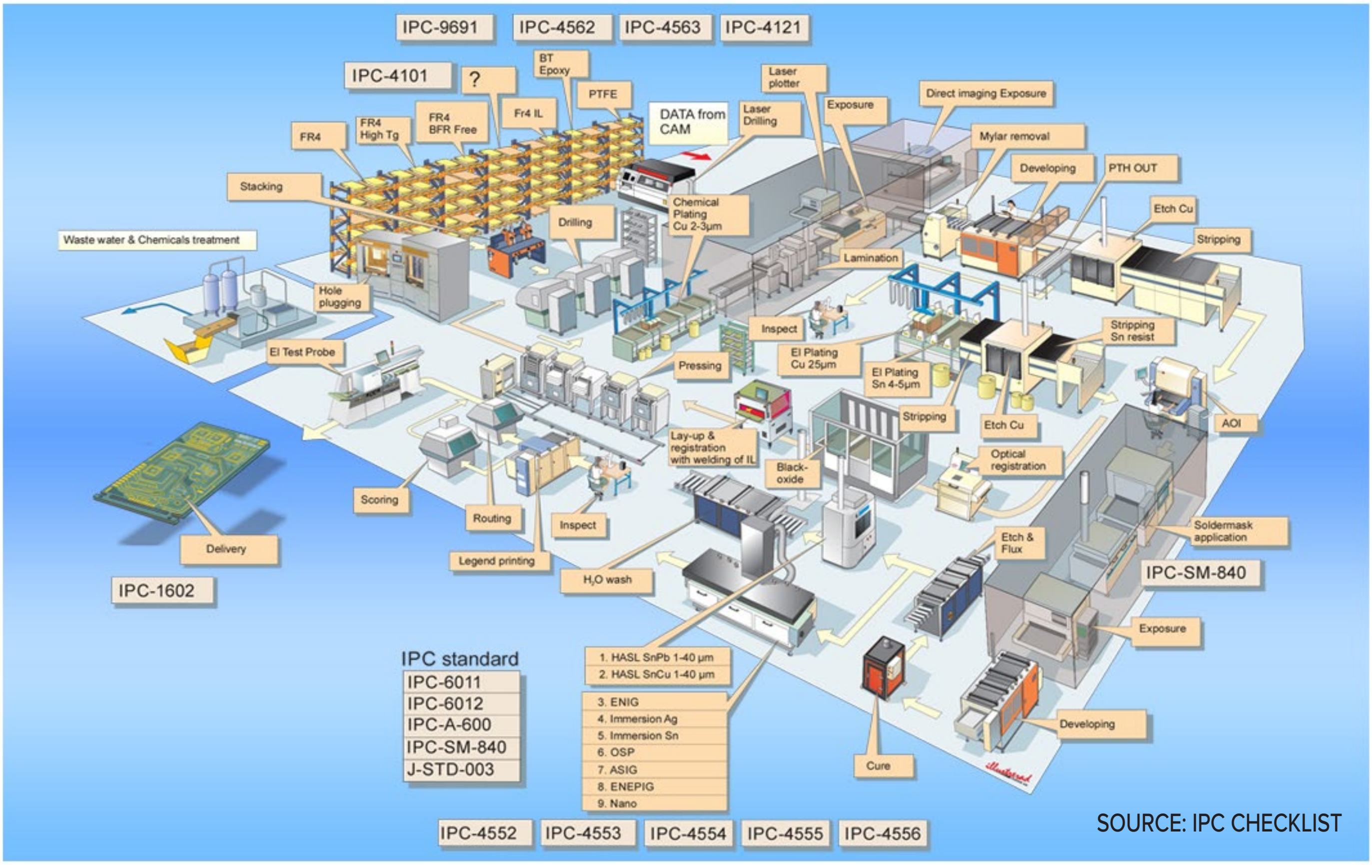
Given the current downturn in the semiconductor industry and the off-peak season, preliminary inspections indicate no significant damage to the machinery, suggesting the impact is manageable.

In terms of silicon wafer production, Shin-Etsu and GlobalWafers' facilities in Niigata are currently shut down for inspection. However, most of Shin-Etsu's crystal growth operations are primarily in the Fukushima area, thus experiencing limited impact from this earthquake. SUMCO reported no effects.

On the semiconductor front, Toshiba's Kaga facility in the southwestern part of Ishikawa Prefecture is currently undergoing inspections. Additionally, the three TPSCo factories in Uozu, Tonami, and Arai are all undergoing shutdowns for inspections. In contrast, USJC was not affected.

MLCC manufacturer TAIYO YUDEN's new Niigata plant, designed to withstand seismic activity up to level 7, reported no equipment damage. Murata (MLCC fabs only) and TDK's MLCC plants experienced seismic intensities below level 4 and were not notably affected. However, Murata's other factories in Komatsu, Kanazawa, and Toyoma, which are in the areas with seismic intensity above 5, were closed for the New Year holiday, and staff are currently assessing any damage.

(Source: TrendForce)



SOURCE: IPC CHECKLIST

What Do You Know About PCB Manufacturing?

Feature Interview by the I-Connect007 Editorial Team

Much of a designer's job involves creating a product that is compatible with the capabilities of their chosen fabrication and assembly providers. But very few PCB designers have visited a board shop or assembly facility in decades, if ever, and seemingly simple DFM problems continue to dog our industry. What manufacturing concepts are designers missing?

We posed this question to Tony Bell, division manager of San Diego PCB Design, which was acquired by APCT in April 2023 and continues to operate under its original name, with plans to transition to its official new name of APCT Design. Tony has experience in PCB design, fab, assembly, and test, so we asked him what PCB designers need to know about manufacturing. He points out the need to continue learning about fab and assembly processes throughout their careers, and asking questions is not bothersome, it's necessary for the job.

Andy Shaughnessy: Tony, you have a pretty wide background in this industry. Tell me about that.

Tony Bell: I've been in this industry for a while, and am fortunate to have a diverse background that got me to where I am now. I came to San Diego PCB Design from Plexus in October 2021. At Plexus, I learned assembly process flow and I was an in-circuit test technician. Later, one thing led to another, and I moved into Plexus' Engineering Solutions, where I managed the North American region's PCB design team. There, 12 designers reported to

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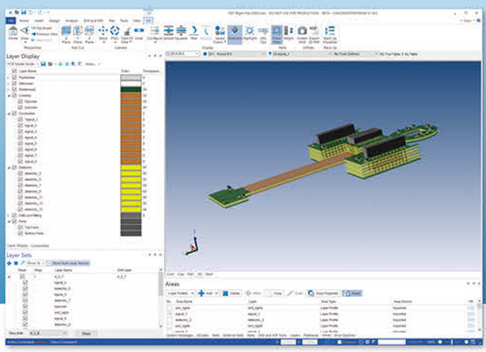

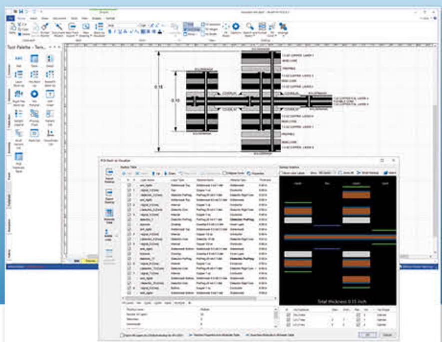

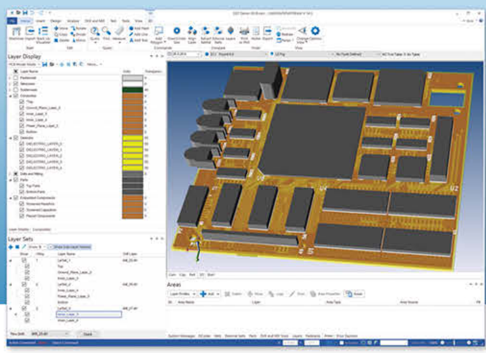

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For more information visit downstreamtech.com or call (508) 970-0670 me in Neenah, Wisconsin; Guadalajara, Mexico; Raleigh, North Carolina; and Boulder, Colorado. Now that San Diego PCB Design has been purchased by APCT, I'm enjoying learning more about advanced fabrication as a design manager on the fab shop side.

Shaughnessy: What do you think designers and design engineers need to know about manufacturing processes?

Bell: They need to know that the manufacturing process is ever-changing. This goes for electrical interfaces, fabrication, assembly, and test. Designing in a vacuum without a desire to learn new things can be stifling to a designer's ability to grow in their capabilities as well as their ability to contribute to their organization.

Tony Bell

Barry Matties: We've been talking for years about this disconnect between designers and fabricators, and how many designers have never been in a fabrication facility. If I'm looking to contract a designer, the smartest strategy might be for me to find a designer who actually works in a fab facility, because that's where the best DFM would come from.

Bell: Sure. You know, there's not a one-size-fits-all answer, of course. In this industry, there are three main categories of designers. First, I'm guessing at least half the designers in the U.S. are attached to an OEM. Maybe I'm just a bit naive, because I've spent my career on the contract side, but we interface with OEM designers on quite a few of our customers' projects. The designers often interface with a small subset of fabricators and CEMs.

On the contract side, we're working daily with different customers, a multitude of fab houses that we need to interface with, and different CEMs, so we have to be agile. There are noticeable differences between these two designers, the largest of which is the pace. At an OEM, the work can be concentrated to hardware cycles and timelines. On the contract side, I'm working on my next project before I'm finished with the previous one, and I maybe have two or three other smaller designs that I'm squeezing into review cycle times.

The third group of designers are at startups, which tend to be in prototyping. These organizations often utilize contracted design help as pace is often targeting concentrated time-to-market goals. Many hire on contractors for a more focused approach to their design needs. These designers often need to prioritize schedule over cost and design optimization or minimized technology.

I remember the first time I went into a fab shop; it was a very eye-opening and nostril-opening experience. It changed how I looked at design. My first fab shop tour was at Multicircuits in Oshkosh, Wisconsin. Their capabilities were sufficient for most designs, but more limited in advanced technologies. The second shop was the TTM facility in Chippewa Falls. Talk about the two extremes: a smaller and more focused PCB shop and then a high-technology, complex shop.

Seeing those two facilities up close really put the puzzle pieces together for me. Seeing the size and hearing the hum and cadence of a drill helped me understand how this process can realize the large number of drill hits in each design. Seeing and smelling the plating baths put to reality the chemical side of fabrication, how different finishes are realized, and why a fabricator may not be able to have a multitude of different plating processes. Seeing boards travelling down a conveyor in the etching lines and watching copper disappear as the board is slowly sprayed with the etching chemicals gives credence to the necessity to give our fabricators margins that are not arbitrarily small. This all made me realize that there was a lot of physics going on inside any PCB. It was shortly after that I started building my Rolodex of people whom I would reach out to when I didn't know something. Fab shops are just rife with people who want to help you design boards that will go through their facilities smoothly.

Matties: What did you learn in a few facility visits that changed your approach to design?

Bell: It changed my perspective, which of course changes your approach. It shifted again once I became attached to APCT. As a designer at Plexus, we designed boards and had all kinds of process written around designing for manufacturability (DFM), designing for fabrication (DFF), and designing for assembly (DFA). We called our preferred and qualified fab houses, asking about their capabilities. But on the assembly side, we didn't have 10 different CEMs; we had one: "Here at Plexus, we design for assembly, and these are the rules that we use. If we can't implement these minimums, we won't be able to build it efficiently." We had to take painstaking efforts to make sure that our DFA was in very good shape.

We called our preferred and qualified fab houses, asking about their capabilities.

That said, there are three main aspects for a successful design: You design for electrical characteristics, for your ability to fabricate it, and for your ability to assemble it. At Plexus, electrical characteristics and assembly techniques got prioritized. If we needed to build complexity into the design, we had a matrix to select fabricators' capabilities to fit the design. The reality was that if a smaller shop couldn't build this board, we could go to a shop with greater capabilities. Your perspective changes when you've visited fab shops and talked with the engineering and sales folks at fab shops who really know their processes. They want to help you. It is okay to ask for grace when getting technical questions from the fabricators. They are building, in most cases, the most expensive component to any PCBA BOM, so it's good to have a relationship with your fabricators. Push when necessary, but give them what they need if it isn't impactful to other aspects of the design.

Shortly after I became the manager of the team, we implemented a training program for junior engineers that talked about those provocative questions in fab. For example, we would ask a junior hardware engineer, "If everything else on the board is the same, and you have a 0.5 mm pitch component and a 1 mm pitch component, which one will you pick?" Most of the newer hardware engineers would pick the smaller pitch, because that means that the designer could have more room to do what they do. But inadvertently, this can drastically increase the cost and complexity of the fab by simply making an uninformed decision early in component selection or concept convergence.

Happy Holden: I've seen many PCB design problems that were related to the assembler. I especially dislike assemblers doing printed circuit design, because they favor assembly, and when they favor a certain pitch or process capability, they push it off to the fabricator. The assembler is simply refusing to improve his process. Instead, he wants every board to cost 15–20% more. He saves 5%, which gets distributed over the entire volume, but now every board will cost more. Of course, assemblers don't like me saying this. For instance, at HP, we started using microvias, and we developed an assembly

process to fill them. But contract manufacturers insisted that microvias be plated shut, which is a 15% cost-adder. They refused to improve their process and instead pushed it onto the fabricator at a 15% increase in price that was not necessary.

Bell: Happy, I think there are some assemblers who wouldn't mind charging 15% more for process steps, especially process steps they're good at. The reality is that many customers won't pay that 15%. The mature CEMs will continually refine their process, and train their people so that their offerings can be agile to the board that comes to them. I believe the less mature assemblers or CEMs that have fewer capabilities are getting to the point of just no-bidding a design that they can't reasonably build. Now, that doesn't mean they don't have the capability, but they likely don't have the people to refine the process such that it can handle those very small parts.

A lot of OEMs have a large hardware team, but only one or two on their team will do design. Some OEMs will have a dedicated design staff or offload design responsibilities to a contract agency. Some companies have a person who they'll train specifically (organically) as a designer, and this allows them the ability to truly develop design techniques, whether that be learning the IPC rules (CID and CID+), fabrication capabilities, etc. These are areas where a designer becomes the liaison between your hardware team and your fabricators.

A lot of OEMs have a large hardware team, but only one or two on their team will do design.

Nolan Johnson: Tell me about your hiring process for designers. What do you want designers to know before you hire them?

Bell: If I'm going to go hire a designer, I'll ask, "What is your main tool flow?" Most of the time, they say they are primary in one specific tool. Then you can dig in and ask, "What would you do if you were implementing particular types of solutions? What would be your approach in this or that situation?" DDR is one example, but it's a good question, and it's used all the time to find out a designer's approach to more complex solutions. Most junior-level designers haven't designed many DDR circuits, while intermediate designers have done dozens of them. Do they truly understand the digital design process, or do they only understand how one EDA tool flow addresses it?

You can find out whether their approach to DDR is tool-agnostic by asking, "What's your process for DDR design?" If they say, "I'll go into the constraint manager and set up net groups," then this sounds like tool-specific verbiage. But a designer who understands a tool-agnostic approach might say, "I need to understand the interface. Is it an FPGA or an ASIC? Are there pin package delays that need to be implemented from the processor or DDR substrate? How far apart will the parts be from each other? What is the implied topology? What do the via structures look like on the board?" You need to know how to use the tool to implement the right solutions, of course, but these are provocative questions that I am looking for a potential designer to ask.

Shaughnessy: What final advice do you have for new designers about manufacturing processes?

Bell: Never stop learning about fabrication, assembly, and test. Learn everything you can. Don't be afraid to ask if you don't understand a certain process or industry nomenclature. Just ask. If you don't get the answer from the first person, you need to ask another person until you find someone who has the answers. Keep learning and keep asking questions.

Shaughnessy: Thanks for your time, Tony.

Bell: Thank you. I enjoyed it. DESIGN007

What Designers Need to Know About Manufacturing, Part 1

Designers Notebook

Feature Column by Vern Solberg, CONSULTANT

The designer needs to have a working understanding of two key manufacturing operations: basic circuit board fabrication procedures and assembly process practices. For printed circuit board manufacturing, the number of steps required to produce the printed circuit board correlates to the circuit board's complexity. Greater process complexity in fabricating the circuit board equates to increased costs. To develop any portion of the electronic product, the designer must apply the design for manufacturing (DFM) principles established in the industry. In fact, DFM should always be the goal of the design engineer. It encompasses a wide range of disciplines that must be considered during the planning phase of any product.

The critical elements of DFM principles include:

- Design for fabrication efficiency (DFF)
- Design to enable electrical test (DFT)
- Design for assembly processing (DFA)
- Design for end product reliability (DFR)

Planning for PCB Fabrication

Printed circuit boards may be as simple as having a single- or double-copper layer or require a more complex multilayer construction. The fabrication processes implemented will commonly use the same basic materials, but fabrication processing can differ a great deal from one manufacturer to another. Although many circuit board fabricators will use similar chemistries and process systems to build the board, there can be significant differences in how they manage and control their processes.

There are four primary material elements for PCB fabrication:

1. **Substrate.** The first and most important is the base substrate, usually made of woven glass-fiber reinforcement and epoxy. This material is used for the majority of circuit board applications because it provides a physically stable dielectric platform for both circuit interconnect and component mounting.
2. **Copper layer.** Depending on the substrate base material, this electrically conductive layer will be a copper foil laminated to one or both surfaces of the dielectric core.
3. **Solder mask.** Applied on the outer surfaces after circuit imaging and chemical etching, a polymer coating applied over the bare copper circuit features on the circuit board surface.
4. **Surface marking.** Silkscreen and ink-jet printing (also known as legend or nomenclature printing) is applied on the component side of the board to furnish the assembly part numbers, source identification, material content, and component reference.

Circuit design engineers must also consider several governing criteria: minimizing unnecessary complexity, specifying the most suitable base materials, and applying proven circuit design principles that will enable efficient assembly processing. The goal is to provide an end product that meets its intended performance criteria and furnishes reliable operation throughout its life cycle.

Circuit Complexity Assessment

When assessing printed circuit board design complexity, first consider the component area and board area ratio. While the less complex circuit may only be the single- or double-copper-layer circuit, the component area to circuit board surface area ratio may not be workable. Conductor routing follows component placement. Clearance protocols must be established in advance: the space separating via-hole lands, microvia lands and/or component attachment lands. Spacing provided between surface mount land pattern and hole lands is referred to as "channel width." The channel widths for routing active and array-configured semiconductors will be mathematically calculated using the terminal pitch (center-to-center distance) and the size of the land pattern. This provides the maximum number of conductors that can be routed between each channel (conductors per channel). The spacing separating the circuit conductors must consider the established minimum electrical clearance required for fabrication process variables, solder-mask surface adhesion, land pattern features, via-hole lands, and other fixed elements on the board.

Narrow conductors routed in parallel may have a space equal to the conductors' width; however, wider current-carrying and ground conductors will probably require a significantly wider spacing between adjacent conductors. Three circuit routing complexity levels for the multilayer printed circuit board are compared in Table 1.

The width of conductors that function as power and ground paths will increase to accommodate the level of current flowing through them. The best guide for establishing conductor width and copper thickness is detailed in IPC-2152, *Standard for Determining Current-Carrying Capacity in Printed Board Design.*

Table 1: Complexity factor related to conductor width and spaces

	Complexity Level 1		Complexity Level 2		Complexity Level 3	
Circuit layers	Outer L/S	Inner L/S	Outer L/S	Inner L/S	Outer L/S	Inner L/S
1	75µm (~.003")	---	60µm (~.0025")	---	50µm (~.002")	---
2	75µm (~.003")	---	60µm (~.0025")	---	50µm (~.002")	---
4 – 8	75µm (~.003")	60µm (~.0025")	60µm (~.0025")	50µm (~.002")	50µm (~.002")	38µm (~.0015")

Data source: Independent industry capability survey

When the surface area for component interface is restricted, it may justify adopting multilayer or a multilayer sequential build-up (SBU) PCB fabrication to improve power and ground distribution and allow more efficient sub-surface circuit interconnect capability.

Base Material Selection

Circuit board fabricators and circuit board material suppliers have worked together in establishing a series of standards documents to eliminate misunderstandings between manufacturers and purchasers, facilitating interchangeability and end product improvement. Standards allow the fabricator to set up their processes that will meet the quality and reliability criteria defined by the customer company. A standard that focuses on materials for printed circuit board fabrication, for example, is IPC-4101, Specification for Base Materials for Rigid and Multilayer Printed Boards. This document is prepared and maintained by IPC member companies. The working members developing and maintaining these standards are experienced in all segments of the product development: engineers, designers, material suppliers, printed circuit board fabricators, and assembly service providers.

IPC-4101 includes the requirements for both laminates and prepreg base materials used primarily for rigid or multilayer printed circuit boards.

Key properties include:

- Dimensional stability and flexural strength
- Coefficient of thermal expansion (CTE)
- Limits of thermally induced Z-axis expansion
- Glass transition temperature (Tg)
- Thermal conductivity and flammability rating

At the end of IPC-4101 is a series of detailed specification sheets that furnish key requirements for both laminate and prepreg materials. The specification sheets are classified by a specific reinforcement type, resin system, and/or construction. Each variation is assigned a unique specification sheet number and includes copper foil peel strength, resistivity, moisture resistance, moisture absorption potential, and the maximum kV level resulting in dielectric breakdown.

Prepreg sheet materials are furnished when adding additional (buildup) circuit layers onto the partially processed base or core substrate. The prepreg is a thin woven glass fiber

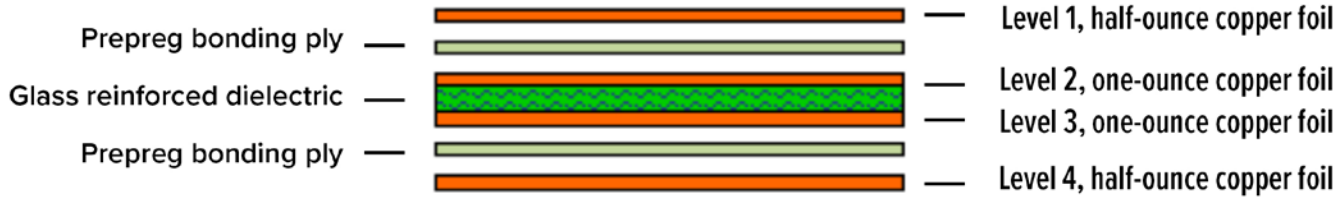


Figure 1: Four-layer printed circuit board stack-up.

cloth impregnated with a resin bonding agent furnished to the circuit board fabricator as a partially cured dielectric sheet (referred to as B-stage or bonding ply) material. In preparation for joining the circuit board layers, the B-stage prepreg material is placed between the rigid laminate materials or as shown in Figure 1, between the copper-clad laminate base and the succeeding copper foil layers. The process for joining the multi-layer circuit uses specialized lamination systems employing both heat and pressure.

FR-4 Glass/Epoxy Laminate ($)

This family of glass-reinforced material developed for printed circuit fabrication has been (and will continue to be) the workhorse of interconnection technology. The materials are widely available, very versatile, and tailored to accommodate different product functions or applications: hand-held, portable electronic products to large multilayer system-level boards. The dielectric is defined as a high-pressure thermoset plastic laminate that exhibits, in a panel form, a robust strength-to-weight ratio and performs well in most environmental conditions.

- Glass transition temp (Tg): 150–200°C
- Surface resistivity: 10^4 MΩ minimum
- Dielectric breakdown: 40kV minimum

These attributes, along with good fabrication characteristics, make it a secure choice for a variety of electrical and mechanical applications, retaining its high mechanical values and electrical insulating qualities in both dry and humid conditions. Although all epoxy/glass laminates have similar physical attributes, the products that adopt these materials often have very different manufacturing focus and performance requirements.

Note: The acronym "FR" stands for flame retardant, denoting that the material comprises woven fiberglass cloth with an epoxy resin binder. The material complies with the Underwriters Laboratory Standard, UL94V-0, defined as glass fiber/epoxy composite with copper foil laminated on one or both sides.

Bismaleimide/Triazine (BT)/ Epoxy Laminate ($$)

BT laminate is one of the preferred materials for products developed to operate in the more physically challenging environments and has proven ideal for semiconductor package substrate applications. The company that developed the material reports that, when compared to standard epoxy resin systems, the blending of bismaleimide/triazine with epoxy provides:

- Enhanced thermal and mechanical stability
- Improved electrical performance
- Furnishes a higher Tg (180°C)
- Lower coefficient of thermal expansion
- Improved electrical insulation in high humidity and temperature.

Polyimide (PI)/Glass Laminate ($$$)

Polyimide-based laminates are comprised of a high-strength and high-temperature polymer material system engineered with an all-polyimide resin chemistry suitable for any electronic package application requiring uncompromised performance. Thermal stability of the polyimide composition and glass fiber reinforcement makes this material particularly attractive for products with stringent high-temperature operating requirements.

- Glass transition temp (Tg): 200°C minimum
- Surface resistivity: 6 x 10^4 MΩ
- Dielectric breakdown: 40kV

Note: The moisture absorption rate for PI materials is relatively high when compared to the FR-4 and B-T composites.

Special Application Laminates

Alternative dielectric formulations have evolved that can address the technical needs of a wide range of special applications. High-frequency laminate products, for example, are better known for cores with better high-frequency properties, such as PTFE (Teflon®) that has a wider range of Dk values than FR-4 material. The PTFE composite is more expensive than fiberglass, but is better suited for high operational frequencies, making the laminate a good choice for RF circuit boards.

- Low electrical signal and dielectric loss
- Excellent thermal management characteristics
- Broad range of Dk (dielectric constant)
- Low out-gassing (ideal for space applications)
- Enables improved impedance control

Comparing the commercial FR-4 to the PTFE (Polytetrafluoroethylene), the material is less likely to experience a dielectric breakdown when operating in extreme environmental conditions.

When selecting base materials for the circuit board, the designer must consider end-product safety. Government agencies, both domestic and international, have banned a number of elements considered a health hazard, for example, plating and soldering alloys that contain lead.

Part two of this series will focus on PCB fabricator-recommended design guidelines for efficient circuit board fabrication processing. DESIGN007

Vern Solberg is an independent technical consultant, specializing in SMT and microelectronics design and manufacturing technology. To read past columns, click here.

Beyond Blueprints: Early Involvement Shapes Superior Fab Outcomes

Feature Article by Lea Maurel
ICAPE GROUP

PCB fabrication is the cornerstone of innovation in electronics, transforming intricate circuit designs into crucial PCBs. As technology advances, the demand for reliable PCBs with ever-increasing circuit density surges and highlights the pivotal role of fabrication in shaping the electronics landscape. In this intricate dance between innovation and execution, a symbiotic relationship emerges between designers and fabricators. This forms the core of success.

Effective communication acts as the bridge between design ideation and manufacturing realization, emphasizing the need for a collaborative approach. The essence lies in early involvement, where fabricators contribute knowledge from the design's nascent stages, ensuring a seamless transition to functional PCBs. Subsequent exploration will delve into harnessing this symbiotic relationship at key stages, reaping tangible benefits in PCB fabrication.

Early Involvement of Fabricators

Collaboration in Floorplanning

In the intricate dance of PCB fabrication, the initial floorplanning stage emerges as a crucial arena where the collaboration between designers and fabricators sets the stage for success. This collaborative approach brings forth many advantages to shape the trajectory of the entire fabrication process.

First, involving fabricators in floorplanning bridges design intent and manufacturability. Fabricators bring practical insights into the materials and processes that will be employed during manufacturing. This collaboration ensures that the floorplan not only aligns with the functional requirements but also optimizes the placement of components for enhanced manufacturability.

One notable advantage is optimizing component placement for both performance and manufacturability. By integrating the expertise of fabricators, designers can strategically position components to minimize trace lengths. This reduction in trace lengths enhances signal integrity and streamlines the routing process during layout. The result is a PCB that meets design specifications in a manner that is inherently easier and more efficient to fabricate.

Benefits

The benefits of collaborative floorplanning extend beyond conceptual advantages to tangible, quantifiable improvements in PCB performance and manufacturability. Reduced trace lengths, for instance, can be quantified in terms of signal integrity improvements. Studies have shown that a collaborative approach in floorplanning can lead to a noteworthy percentage reduction in trace lengths, resulting in a marked enhancement in signal integrity metrics.

Another quantifiable benefit arises from incorporating thermal considerations during floorplanning. By strategically placing heat-generating components and optimizing thermal pathways, designers can achieve better heat dissipation characteristics. This, in turn, contributes to enhanced manufacturing efficiency as it mitigates potential heat-related issues during the assembly process. The quantifiable metrics range from reduced manufacturing time (due to fewer thermal-related defects) to an overall increase in the yield of fabricated PCBs.

Optimizing Material Selection

Early discussions on material choices with fabricators wield a significant impact on the overall success of PCB fabrication. The choice of materials directly influences the performance, reliability, and cost of the final product. In the realm of PCB design, where the selection of materials can be a complex decision, involving fabricators at this stage provides invaluable benefits.

Consider a scenario where informed material selection positively affects both performance and cost. Collaborative material discussions can lead to the identification of materials that not only meet the design specifications but align with the cost constraints of the project. For example, selecting a material with specific thermal properties may not only contribute to the reliability of the PCB but can potentially, in some cases, reduce manufacturing costs by streamlining the fabrication process.

In summary, the advantages of involving fabricators in the early stages of floorplanning translate into quantifiable benefits. From optimizing component placement for improved signal integrity to strategic material selection influencing both performance and cost, this collaborative approach sets the foundation for a more efficient, faster, and ultimately easier transition to PCB fabrication.

DFM Principles

Component Selection and Standardized Footprints

In the intricate tapestry of PCB fabrication, the principles of design for manufacturability (DFM) stand as guiding beacons, illuminating a path toward efficiency and precision. Among these principles, the careful selection of components and the utilization of standardized footprints emerge as pivotal practices, each contributing to a more streamlined and cost-effective manufacturing process.

The importance of selecting easily available components cannot be overstated. In the world of PCB fabrication, component availability directly influences production timelines and costs. By opting for components readily accessible in the market, designers pave the way for smoother procurement processes and reduce the risk of delays due to supply chain disruptions. This strategic choice not only enhances the reliability of the supply chain, it ensures a more cost-effective production cycle.

Furthermore, the advantages of using standardized footprints resonate throughout the assembly process. Standardized footprints, or well-defined patterns for component placement, simplify the assembly line. This practice facilitates an efficient, error-reducing, and ultimately faster assembly process. Components with standardized footprints can be easily sourced, placed, and soldered, contributing to a more streamlined manufacturing workflow.

Documentation and Communication

In the dynamic interplay between design and fabrication, comprehensive documentation and effective communication emerge as pillars of success. The need for detailed design documentation is paramount, serving as a common language that unites designers and fabricators in their collaborative journey. Detailed documentation includes specifications, tolerances, and material requirements, providing fabricators with a clear roadmap for turning design concepts into tangible PCBs.

The significance of effective communication and documentation practices cannot be overstated. Clear communication channels between designers and fabricators foster a collaborative environment, minimizing misunderstandings and ensuring that design intent is accurately translated into the manufacturing process. Documentation serves as a reference point, aiding in the resolution of queries, mitigating potential errors, and ultimately contributing to a more efficient and error-free transition from design to fabrication.

In conclusion, integrating DFM principles, including component selection and standardized footprints, showcases its transformative impact through quantifiable improvements. Case studies demonstrate reduced manufacturing costs, faster assembly times, and fewer errors. Simultaneously, emphasizing comprehensive design documentation and effective communication practices underscores the collaborative nature of the designer-fabricator relationship, paving the way for a seamless transition to PCB fabrication.

Iterative Feedback, Quality Assurance, and Continuous Improvement

Iterative Feedback Loop

In the intricate dance of PCB fabrication, the concept of an iterative feedback loop stands as a dynamic force propelling designers and fabricators toward excellence. This continuous exchange of insights not only accelerates the identification of challenges but fosters a culture of collaboration that is fundamental to achieving superior PCB fabrication outcomes.

Prototyping is a cornerstone of the iterative feedback loop, providing a tangible embodiment of the design for both designers and fabricators. It allows stakeholders to evaluate the real-world manifestation of the design and uncover any unforeseen challenges. For example, in a recent project involving high-frequency circuitry, the prototypes revealed signal integrity issues that were not evident in simulation models. This timely feedback facilitated rapid adjustments to the design, averting potential manufacturing setbacks.

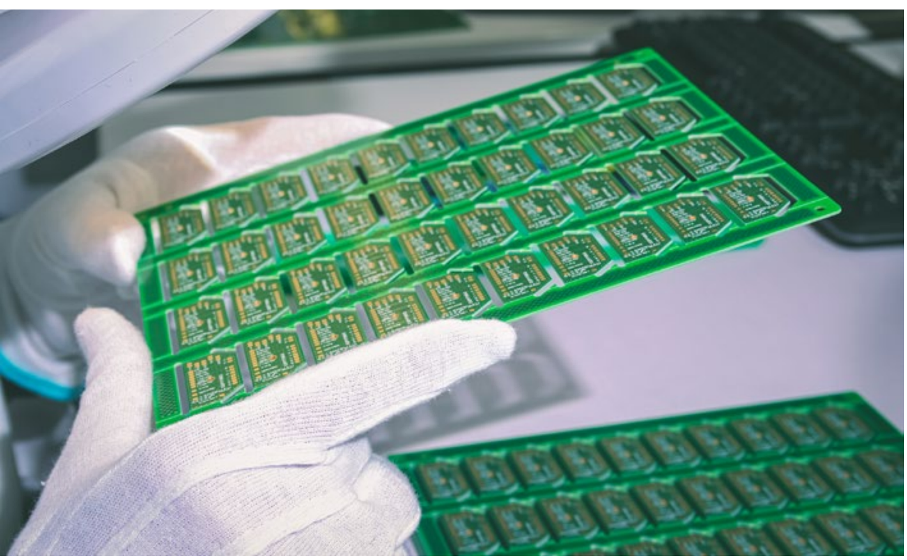
Furthermore, a continuous feedback loop between designers and fabricators enables swift identification and resolution of manufacturing challenges. In a case study involving a complex, multi-layered PCB, the iterative exchange of insights during the fabrication process revealed a minor flaw in the layer stackup. The early identification of this issue allowed for prompt corrective action, preventing downstream delays and ensuring the final product met both design and fabrication specifications.

Quality Assurance Measures

Quality assurance measures are the bedrock upon which the reliability and performance of a fabricated PCB stand. Design verification testing (DVT) and failure mode and effects analysis (FMEA) play pivotal roles in ensuring that final designs not only meet but exceed performance requirements.

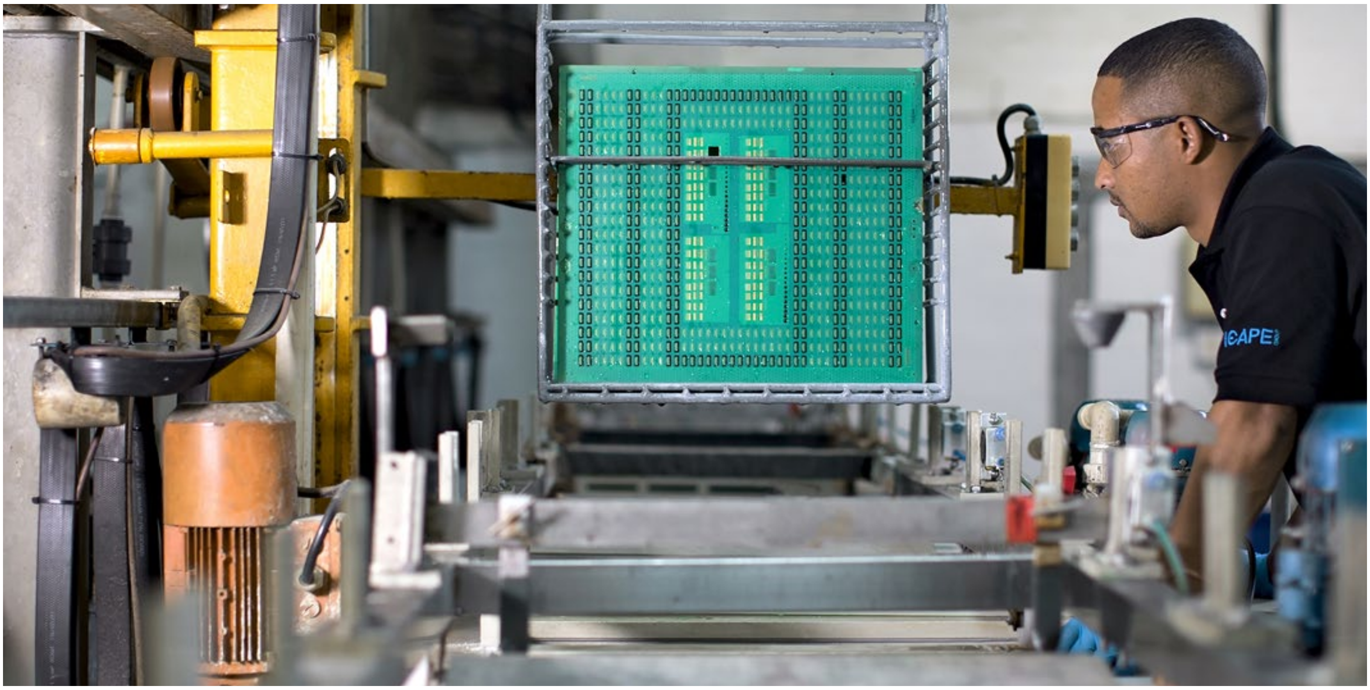
Design verification testing, conducted in collaboration with fabricators, verifies that the PCB functions as intended. This iterative process helps identify and rectify any design-related issues that may impact the manufacturability and performance of the PCB. In a specific project, DVT revealed a minor inconsistency in trace routing that, if left unaddressed, could have led to signal degradation. The collaborative approach to DVT facilitated swift corrective actions, underscoring the importance of early quality assurance measures.

Similarly, FMEA provides a systematic approach to identifying and mitigating potential failure modes in the design. Collaborative FMEA sessions between designers and fabricators unearth potential weak points in the design, enabling preemptive measures to enhance reliability. The quantifiable result is a notable reduction in the occurrence of defects, leading to higher product quality and customer satisfaction.



Continuous Improvement Strategies

The journey of collaboration and innovation extends beyond the confines of a single project. Embracing a commitment to continuous improvement ensures that each



project becomes a steppingstone toward excellence for both designers and fabricators.

Post-project evaluations serve as a critical component of continuous improvement, allowing one to reflect on what worked well and areas that could be enhanced. This reflective process is not about assigning blame but rather about identifying opportunities for growth. In a recent post-project evaluation, a collaborative effort between designers and fabricators identified a bottleneck in the procurement process that, when addressed, significantly improved project timelines.

Knowledge transfer is another cornerstone of continuous improvement, ensuring that lessons learned from one project are seamlessly integrated into future collaborations. By documenting and sharing insights gained during each project, both designers and fabricators contribute to a collective knowledge base that enhances the efficiency and effectiveness of future endeavors.

In conclusion, the iterative feedback loop, quality assurance measures, and continuous improvement strategies collectively form the backbone of a successful designer-fabricator partnership in PCB fabrication. Through collaborative efforts, early identification of challenges, and a commitment to ongoing improvement, designers and fabricators not only ensure the success of individual projects but pave the way for innovation and excellence in future collaborations.

Summary

In PCB fabrication, the vital partnership between designers and fabricators shapes innovation. By emphasizing early collaboration through design, floorplanning, and layout stages, this synergy enhances DFM principles, iterative feedback, and quality assurance. Tangible benefits, including reduced trace lengths and streamlined manufacturing, underscore the united approach. Quality assurance measures like DVT and FMEA ensure products surpass specifications, reducing costs and errors. The resounding conclusion: Early collaboration is indispensable, and fosters a harmonious partnership where creativity aligns with practicality, guiding the intricate dance of PCB fabrication toward a future where innovation knows no bounds. **DESIGN007**

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IPC DESIGN COMPETITION 2024

Third Time's the Charm

Interview by Andy Shaughnessy
I-CONNECT007

As the IPC Design Competition heads into its third year at IPC APEX EXPO, the contest continues to grow. I asked IPC's design instructor Kris Moyer, and Patrick Crawford, manager of design standards, to discuss this year's event, how the competition has evolved, and why PCB designers should sign up now for this competition.


Kris Moyer

Andy Shaughnessy: Tell us about the preparations for the IPC Design Competition at IPC APEX EXPO 2024. Are there multiple heats again this year?

Kris Moyer: Yes, we're running two heats again this year, and it's the same structure as in previous years—a longer, more involved design in the preliminary heat, and a shorter, more layout-centric design in the finals.

Patrick Crawford: Much shorter for the finals heat. You are looking at a four-and-a-half-hour challenge at IPC APEX EXPO vs. having 25 days to complete the preliminary design.

This is the third year of the competition. Contestants said the first year's design was pretty simple, but last year's design was a more complex rigid-flex shaped like a hand. Is this year's design even more complex?

Crawford: We're trying to find the middle ground in complexity between the inaugural event and last year's event, especially for the preliminary heat. As I'm sure you can imagine, it's difficult to optimize for a challenge while considering the diversity of experience among competitors, and we saw this challenge play out last year. The preliminary design was too complicated for a few folks and too easy for others, and while this kind of differential may be inherent to our philosophy of "come one, come all," we certainly want to avoid it if possible. One option is to split the competition into tracks—expert, emerging engineer, hobbyist, etc.—or change up the structure entirely. But for 2024, we just want to make sure that anyone who registers has fun while building their designs.

Moyer: As for the complexity of the finals design, it will be less complicated and easier to complete in-person at IPC APEX EXPO. This is all due to feedback on the time allotted to complete the design last year; none of the designers could finish, even though some of them came pretty close.

There was some discussion about letting contestants use their own EDA tools in 2024 instead of requiring everyone to use Altium. What was the final word on that?

Moyer: Due to the logistics of the competition, we are still going to require Altium Designer for the finals heat.

Crawford: Because we review the finals designs onsite, it is much easier to open the Altium Designer project file to interrogate the design than it would be to have copies of all EDA tools open to review files, or to have the competitors export fabrication files to be opened with a viewer on our end.


Patrick Crawford

Moyer: They can still use whatever tool they want for Heat 1 because, in this case, we are specifically looking to judge a completed design package, including all documentation that would be submitted for front-end review.

Crawford: There is an ongoing discussion for changing this in future years. I understand that this is frustrating for power-users of other tools, but it's a compromise we've had to make given the limited time and person-hours we have available onsite at APEX EXPO.

How many contestants have entered so far, and when is the cut-off date for entering?

Crawford: Unfortunately, not many. In the spirit of transparency, we're down from last year at this point in registration. I think that with APEX EXPO moving to April and with the registration period landing in the middle of the holiday season, things are just a little funky this year. I really hope that we can get some more signups, because this year it will be easier to complete the preliminary design. It won't be as cumbersome as the last two years, but it will still be a lot of fun. I'm looking forward to seeing competitors in Anaheim.

Why should designers enter this competition?

Moyer: As with the last two years, this is all about recognizing and honoring the talents of printed board design engineers who make their work an art. IPC's mission is to help companies build electronics better and help designers design electronics better. We firmly believe that one of the best ways to get better, whether at design, hand-soldering, or any skill, is to compete. This forces the competitors to push their capabilities beyond their current comfort zones.

What advice would you give designers who enter this competition?

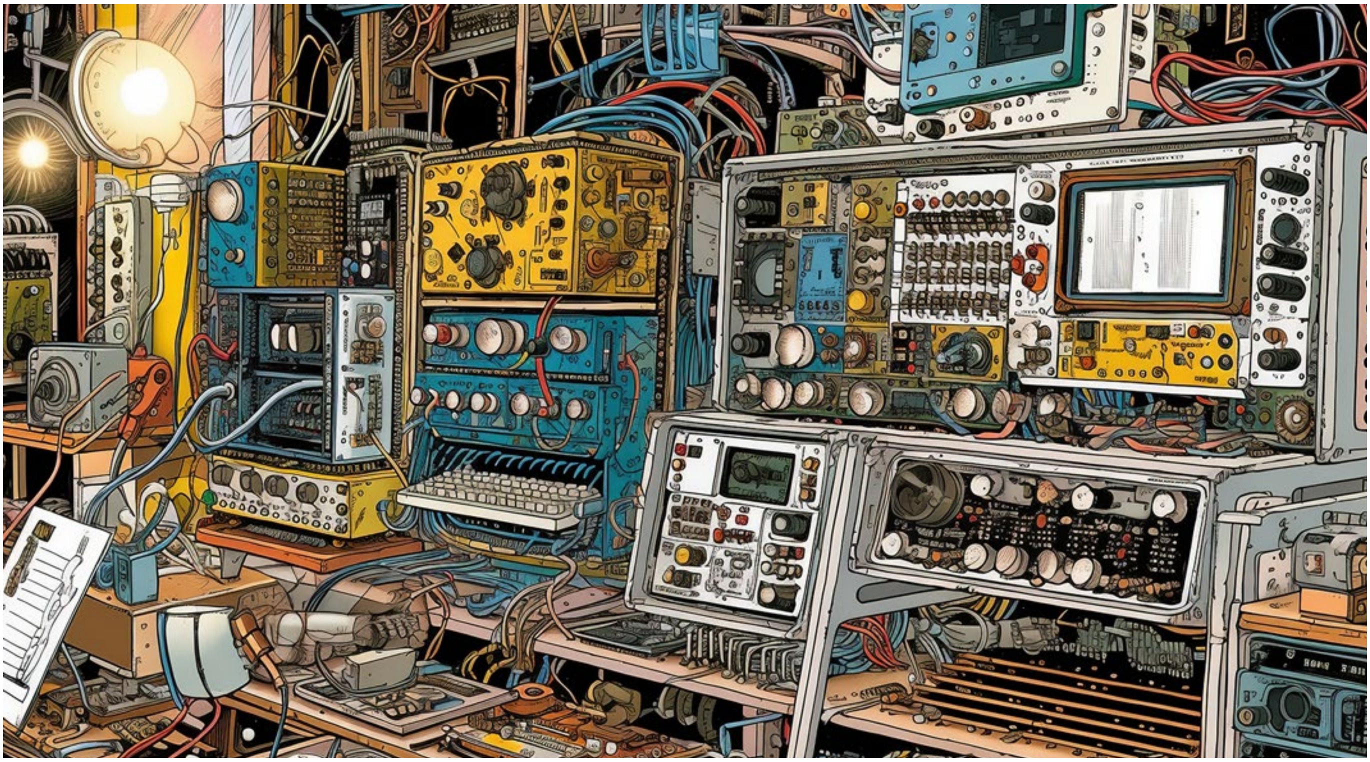
Moyer: Be comfortable with the IPC design standards. That's a must. For both heats, the judges grade designs to the standard.

Crawford: We provide all relevant standards during the preliminary heat, so the competitor has plenty of time to review them. We also grade a tad easier during the finals heat when it comes to adherence to standards, because we don't want to penalize someone with a shakier memory than others, but the competitor can still open them for reference during the finals event.

Moyer: Another piece of advice is to not come into the competition with any preconceived notions about how to design based on your specific company standards. We care about the IPC standards. In that vein, be willing to do something different than what you do every day at work. Finally, look for all possible techniques of optimization in your designs. The judges use IPC standards to judge the designs, but there's also plenty of room in the rubric to award points to those who apply those standards wisely.

Thanks for your time, guys. See you at IPC APEX EXPO.

Moyer: Thank you, Andy. **DESIGN007**



Talking Digital Twin and DFT With Aster

Feature Interview by Barry Matties
I-CONNECT007

Digital twin is a buzzword, but it's really just a way to define what everyone has already been aiming for, says Dean Poplett, technical director at Aster Technologies. But how much does a test company need to put into digital twin? Is it all the equipment or just what needs to be tested? Dean lays out the scenarios Aster manages and how they work with companies to help them achieve their goals.

Barry Matties: What is today's greatest challenge in testing?

Dean Poplett: It's trying to find a new test strategy that helps with the board complexity and the size of the board. For example, you have boundary scan, which is limited by the components that are boundary scannable and limited by the design; ICT, where most of the boards are very limited in size, and we don't have room for test points; and AOI, which is difficult because it's an optical system and tests can be quite subjective. You need to be an expert to understand whether it's doing a good test on that component. It's not definitive.

With our TestWay software, we amalgamate the coverage from each machine and test strategy into an overall coverage. But the limitation is that there are some components we can't test. It would be nice to find the next strategy that takes us further.

Dean Poplett

Digital twin is a term we often hear in the industry. What's your take on it?

Digital twin allows a machine in the real world to predict what a machine will do to the design we have on the table in front of us. If we have it with the entire line, then we can make all the predictions for the real-world scenario before we get there.

Part of the issue, though, is every piece of equipment needs to be digitally benchmarked for performance characteristics and all the data must be ready for a true digital twin, a true manufacturing environment.

Right. Test is slightly easier than assembly, where you have analog-type problems like heat transfer, and tombstoning is caused because of the disproportionate amount of heat and cooling of parts in question. When we are testing, it's reasonably straightforward, and we can predict exactly what a particular option on a machine can achieve. With the circuit and the parallel components around the component we want to test, we know exactly what it will do. With proper circuit analysis, we can predict exactly what a machine can achieve. Obviously, with any analysis, we can predict that, but we might get it wrong one time. Because we have a closed-loop system, our prediction is compared against the actual real cover measurement. Any discrepancy is either because the debug engineer has not done a particularly good job, or our estimator isn't so good. Whenever we get a discrepancy, we can look at the report and say, "Here's your problem, sort it out," or, "It's our problem we will sort it out."

In your software, are you looking at the entire line for the digital twin or are you limited to test?

We pretty much focus on test because most of our customers require it, but we aren't limited. We do have some customers that don't require parametric optimization as their volumes are low enough. They don't want to go to a second source for software to do the job, so we provide assembly and inspection machine analysis and outputs for them. There's no limit to what we can do. It's just that we focus on test because that's what our customers tend to want.

That makes sense, and it ties into design for manufacturing (DFM) and design for test (DFT). When a circuit board designer looks at laying out the assembly, what should they keep in mind for DFT?

Before we start laying out the board, we look at the schematic because that's where it's easier to make any changes. If we can give predictive analysis at that stage, they will save a lot of time by just changing the schematic before the layout starts.

First, we can look at a design, component models, and connectivity, and ensure that this has been done in a way that will not limit test coverage downstream. We have several standard rules that are commonly used, but users also have the ability to verify any issue against their own rule set. Then we can start to look at test coverage estimation and optimization. If we take an example of ICT and boundary scan, we want to test as much of the board as possible but we want to control redundancy. As boundary scan does not usually need test points, we can analyze the coverage of that strategy and remove the necessity for ICT test points on those nets. This allows test points to be placed on the nets the ICT needs to target for optimal combined test.

We go back to the schematic and make the applicable changes, implement the test propositions for the optimized testbed locations, and then go to the layout. This gives optimal coverage but makes the fixture less expensive, too. We've probably saved an iteration or two on the layout as well.

That takes a collaborative effort because a schematic often lines up with the design, or the layout person in that process doesn't come in until later, right?

Right. Traditionally, the tools that have been available to the test engineers have required a layout file, and so the test engineer often gets skipped. They don't do a proper DFT analysis because they don't have time. Once the layout is complete, that's the end of the design, and each iteration holds up release.

If they don't do the DFT, there's a problem. Do we go back and do it twice? Why don't they take the time to really look at DFT? It seems like a critically important operational step.

Yes, it will save quite a bit of money, but it's quite technical. Often, those who make the decisions are non-technical, and those advising them aren't necessarily directly responsible for the DFT. There are management layers, so the information is lost before it gets from the guy who sees it as important to the guy who needs it to be employed.

You mean the person who's in layout? They may have their own process for DFT.

Traditionally, the electronics industry tends to work in booths: You do your bit and then throw it over the wall to the next guy; everyone works in isolation. They do their job to the best of their ability, and they're not really interested in what others are doing. We want the communication between the design and the test engineers to be invisible so they just share information. Some of our tools will allow the development engineer to run the DFT rules that the test engineer has developed without having to send data anywhere. He can just run the tool as it's been set up by the test engineer.

As we look at all the other EDA tools, is this a separate package that would integrate into their design tools?

Yes. Essentially, we already integrate into Altium, and there is a possibility that we integrate into other tools as well. There's no limitation on our side; we can integrate with anybody. It's like Legos: We can plug any module wherever you want it to go.

In your selling process, are you talking to the designers or the OEMs? What's your point of contact?

It depends on where the problem is. If we are looking at DFT and DFM, it may be in the production engineering for DFM. If it's DFT, it would be in the design bureau. Depending on how a company wants to work, it may be pre- or post-layout. We have the test engineering team optimize the test to produce the test data to read back the coverage. So, it might be quality, engineering, or even design. It depends on the customer.

There must be a trigger point for them to stop, or is it just continuous improvement?

If they're interested in improving their process, yields, and their slip rate, they can ask us to do that. But there might be a half-dozen different triggers as to their scenario.

Dean, I appreciate your time and your knowledge. It's great to chat with you.

Thank you. DESIGN007

PCB Design and Manufacturing: Let's Work Together

Tim's Takeaways

Feature Column by Tim Haag, FIRST PAGE SAGE

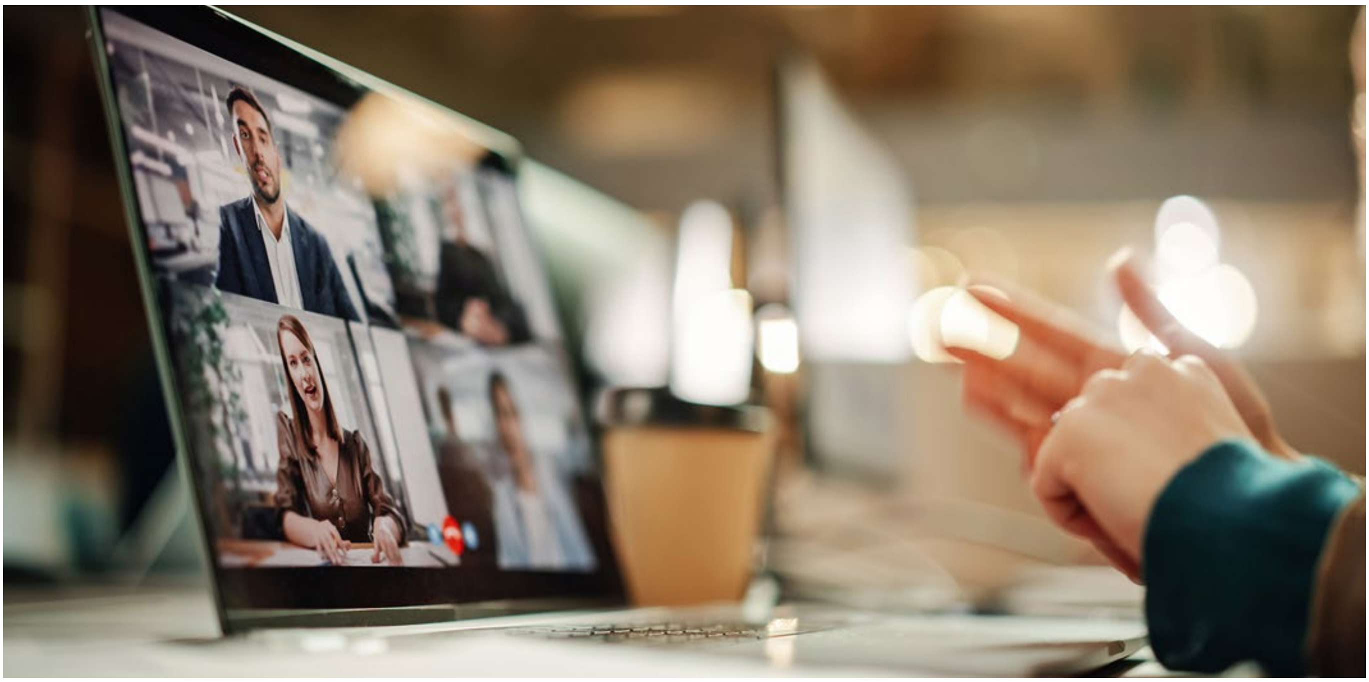
Twas the night before deadline, when all through the house,
Not a creature was stirring, not even an optical mouse;
The components were all placed on the board with care,
In hopes the design review would be gentle and fair.
The traces were routed, with not a single net left,
While power and ground were connected, all expectations were met.
The designers were tired, and ready for a rest,
But hold on everyone, the manufacturer was next in line to test.

Yes, that was embarrassingly cheesy, but I penned this prose to highlight how PCB design and manufacturing has traditionally been treated as two different disciplines when, in reality, we should all be working together.

Let's Work Together

Circuit board design combines electrical, mechanical, and manufacturing engineering. There are many other engineering disciplines involved, such as component and reliability engineering, but the first three are the ones the PCB layout designer will usually spend the most time with. Although electrical and mechanical teams can and usually do have their own dramatic conflicts with each other, they usually end up working everything out in the end.

Manufacturing engineering can be a very different story, especially when those require-




Don't Skip a Beat
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ments come from an outside vendor. Design teams often are more concerned about whether their design is functioning as intended, as opposed to how it gets built. On the other hand, the manufacturer can be more focused on building the design rather than on how it will function once it is built. For the PCB layout engineer, it is essential to realize that neither should be labeled as "the bad guys." Instead, they both have important needs that must be met.

I have spoken with many different companies, and have found that adherence to manufacturing requirements in PCB layout varies quite a bit. On one side are those design groups that don't exercise a lot of caution when it comes to manufacturing requirements. These are often designs produced in lower numbers, and error-free yields aren't their primary concern. The boards are manufactured knowing they will require a lot of manual clean-up to get working units finished.

On the flip side are those companies whose designs are produced in high numbers, and error-free manufacturing is critical to cutting costs. The manufacturing requirements are usually very detailed and process automation is essential to reduce overhead and increase yields. As you would expect, some companies fall between these two extremes. Many of these companies will use different levels of manufacturing requirements depending on the needs of the project, such as prototype vs. regular production builds.

But whether your design team is building prototypes or high-production runs, your success lies in understanding how to work with your manufacturer.

DFM: A Bridge Between Design and Manufacturing

The key to designing circuit boards that can be successfully manufactured with minimal errors is to follow design for manufacturing (DFM) rules. We are all familiar with our CAD system's suite of DFM checking routines, but design for manufacturability is more than just checking off a standard list of rules. It means working with your manufacturer to find out what they need before you hand them the design files. This includes board layer stackup and materials, part selection, and the correct location and spacing of components, traces, and other PCB elements. For the DFM process to truly succeed, consider these three points before you go to layout.

1. Document It

Documenting your company's DFM process so that everyone has a clear understanding of what the objectives are is essential to the long-term success of design for manufacturability. There can be a big difference between how design groups document their standards and procedures, and those with established DFM practices are typically at the top of the list. DFM and other standard operating procedures are usually carefully documented and available to employees electronically or in printed format. In some instances, the design is gated to DFM documentation and won't be released until official reviews are completed and signed off by specific stakeholders. Then there are those groups with very little in the way of official documentation. If they follow DFM practices at all, it is usually in the form of "tribal knowledge" based on previous manufacturing experiences. Do yourself a favor and document your DFM processes and requirements.

2. Enforce It

The next step is to ensure that our DFM is fully documented and ready to be used. This is a great idea, but how can we do it? Here are some ideas to try:

- If you are working at a company where the DFM processes are not well documented, you can start by getting some of these processes recorded. "Is that really my job," you might ask. Well, if you are laying out circuit boards, then the answer is a resounding yes.
- A good place to start is by working with your manufacturing vendors. Contrary to how they are sometimes viewed, they are not the enemy; in fact, they are highly vested in wanting you to be successful. After all, if you are successful, they will be too, and the way they will make you successful is by building your circuit boards correctly, on time, and without errors. Therefore, spend some time with them and find out how you can help them so they can better help you.

- Start capturing some of these standards and get them documented. Even if all you do is create some simple bullet points, it's a good place to begin. You don't have to start out by trying to write a novel; just get the basics down in one place. Once you gather some of these ideas, you will probably find that they will start flowing into what will eventually become a good working document.
- Once your documentation starts to build up, make sure that it is published for all to see and incorporate its use in your job requirements. It is important that designers see quality as an important part of their overall job performance.

3. Automate It

Now that you've started the process of creating your DFM documentation and are enforcing its use by the design team, the next step is to automate. Look for ways to incorporate automated DFM checking into the design process, because there is a big difference out there in how this is being done. Some design teams don't have any DFM checking processes in place and rely solely on their manufacturer to find, report, and even fix DFM errors. Others will perform only a visual check of their designs, while others have built in a very sophisticated automated checking process. Traditionally, automated DFM checking has been handled by the manufacturing vendors with their results reported back to the original designers. Any problems that are found require design changes, and sometimes the board layout has to be completely redone to resolve any bugs found by the manufacturer. Since these same types of DFM checking tools used by manufacturers are available to design teams, engineering teams should put them to work.

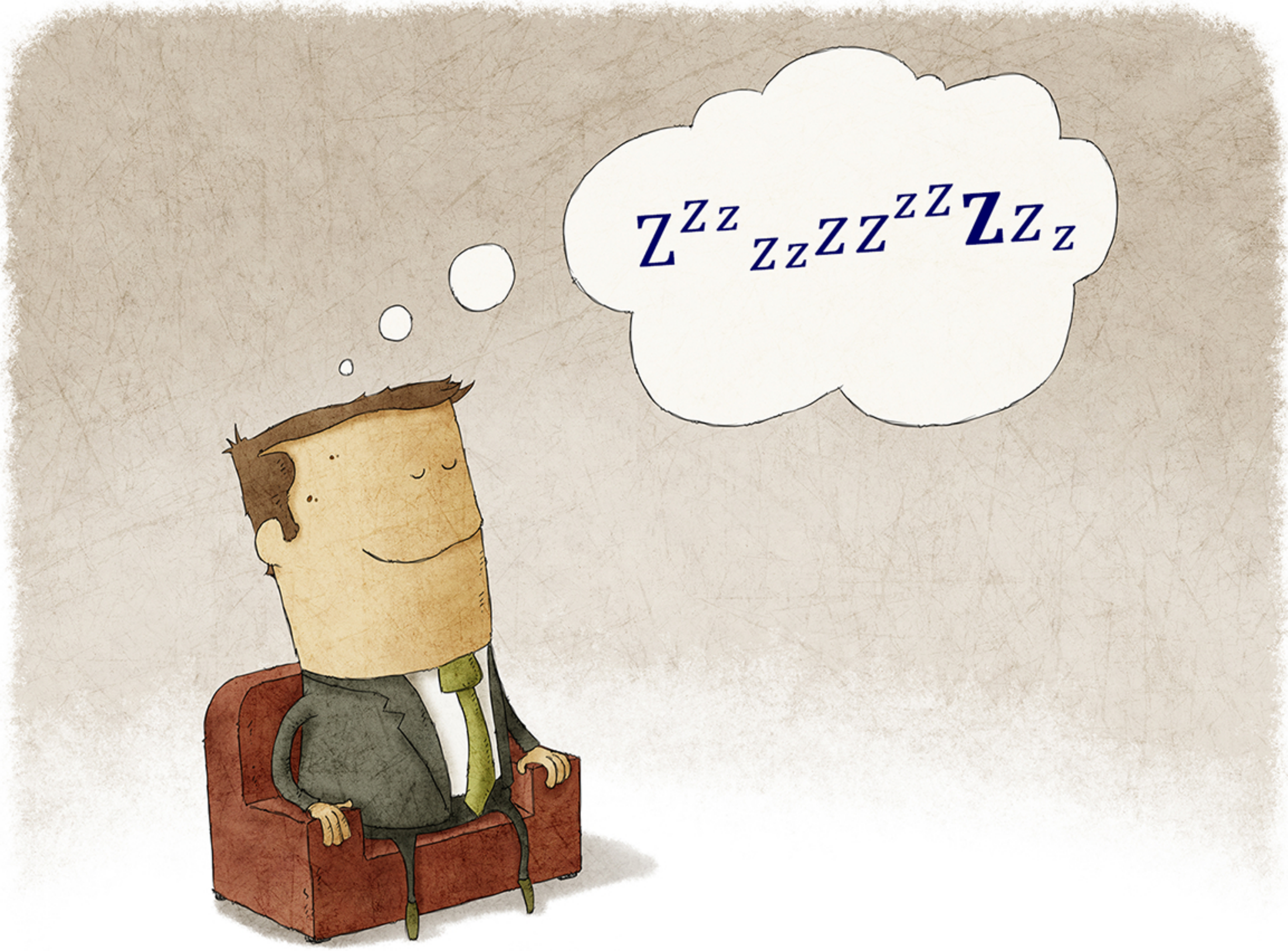
There are a lot of applications that will incorporate DFM checking into the design process, and it may even be that the tools you're using have some new and enhanced features built in that can help. Believe me, full DFM checking by the engineering team before the design goes to manufacturing will save you a lot of time and effort later. But there's still one important step that can potentially save your design team a lot of time and effort: Communication.

How Can We Make It All Work?

One of the best things we can do to help the relationship between design teams and our manufacturing partners is to improve communications. Too often this relationship has been looked at as one of merely throwing the design "over the wall." That may have worked in the past, but it's very outdated considering the amount of information that needs to be exchanged between engineering and manufacturing for a design. Throwing things over the wall is just as likely to end up hitting you squarely in the head and knocking you flat. I know it's tempting to want to dump the completed design in someone else's hands and move on to the next exciting project, but that doesn't work anymore. Our goal as designers should be to see the project through all the way from inception to completion, and that means partnering with our manufacturing vendors to accomplish this task together.

One way to strengthen communication is to encourage participation between designers and manufacturers. Many vendors will happily schedule an onsite visit so you can see exactly what happens during the production of your circuit board. Manufacturers also put a high value on pre-design meetings, design reviews, and in-process questions and check-ins. So, do yourself a favor and spend some time with the people who will build what you design. In the long run it can only help you to design a better product and grow in your career. Until next time, everyone, keep on designing. **DESIGN007**

Tim Haag writes technical, thought-leadership content for First Page Sage on his longtime career as a PCB designer and EDA technologist. To read past columns, click here.



MilAero007 Highlights

RTX to Create Network of 'Energy Webs' for DARPA ▸

Raytheon, an RTX business, has received a $10 million contract from DARPA to design and develop a wireless airborne relay system to deliver energy into contested environments. The Persistent Optical Wireless Energy Relay program, known as POWER, aims to revolutionize energy distribution by leveraging power beaming for near-instantaneous energy transport in a resilient, multi-path network.

New Hampshire's Microelectronics Center Wins $35 Million Through CHIPS Act ▸

The U.S. Department of Commerce and BAE Systems Electronic Systems, a business unit of BAE Systems, have signed a non-binding preliminary memorandum of terms (PMT) to provide approximately $35 million in federal incentives under the CHIPS and Science Act to support the modernization of the company's Microelectronics Center, a mature-node production facility in Nashua, New Hampshire.

Missile Defense Agency, Boeing-Led Industry Team Conduct Early Release Intercept Test ▸

The U.S. Missile Defense Agency and a Boeing-led industry team successfully intercepted an intermediate-range ballistic missile in space during the latest test of the Ground-based Midcourse Defense, or GMD, system. The test validated GMD's Capability Increment 6B configuration, which gives the Missile Defense Operators more time, space, and flexibility to intercept ballistic missile threats to the U.S. homeland.

Nokia to Acquire Fenix Group, Strengthening Wireless Offering in the Defense Segment ▸

Nokia has signed an agreement to acquire Fenix Group, a privately held company that specializes in tactical 3rd Generation Partnership Project (3GPP) communications solutions for the defense communities. Fenix systems are designed to provide high-speed, low latency data connections to many devices and users simultaneously, making them ideal for supporting a wide range of military applications.

Boom Supersonic Selects Honeywell Anthem Integrated Flight Deck for Overture Aircraft ▸

Boom Supersonic, the company building the world's fastest airliner, has selected the Honeywell Anthem integrated flight deck for its Overture aircraft. As part of the agreement between the two companies, Honeywell's next-generation flight deck and its modular avionics platform will be incorporated into Overture.

Future Leaders in Aerospace Prepares the Next Generation for Research Careers ▸

MIT's Department of Aeronautics and Astronautics (AeroAstro) recently hosted the 2023 Future Leaders in Aerospace Symposium, inviting women and underrepresented minorities in aerospace fields to campus for a two-day program. The symposium was open to applications from recent graduates and students within one to two years of earning their PhD, helping early-career academics to launch and navigate an academic career in aerospace engineering.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The Effect on SI and PI Board Performance

Quiet Power

Feature Column by Istvan Novak, SAMTEC

In signal and power integrity (SI and PI), we would ultimately like to see a reasonable agreement between the predicted or simulated and the measured performance of our circuits. Real-world measurements will always contain errors and usually show a distorted replica of the true behavior of the device under test (DUT). Real measurements always show more than just the behavior of the DUT. Even if we don't consider random noise and random errors, in the measured data we have contributions from instrument, cable, and probe errors (just to name a few) that our calibration could not completely remove.

Simulations work differently: They always show less—an incomplete picture of the DUT—simply because there is no way for us to include every detail in our models practically. Not to mention the details that we may not even know about. In simulations, our first question is how to select and set up the models and how to adjust the simulation tool settings so that we get the correct and expected results. But simulations will include only those details that we set up and specify in our simulation model.

This is true for relatively well-known parameters, such as the dielectric constant and loss tangent of laminates, and for other parameters that we tend to describe with a range of fitted models, such as surface roughness. Dimensional tolerances fall into this category. They can be considered in simulations, for instance, by doing statistical margining of the dimensions. However, in high-speed interconnects there are so many geometry details that determine the channel performance, that simulating a meaningful number of combinations becomes daunting. One interesting case is related to backdrilling the unwanted via stub on high-speed channels. If the backdrilled hole is not concentric to the via barrel that we want to remove, there is a chance that a sliver of the barrel remains (Figure 1).

Figure 1a is a properly backdrilled via. In Figure 1b, there is a visible misregistration of the backdrilled hole, leaving part of the original via barrel in place. The residual via barrel behaves similarly to a full via barrel; it creates a dip in the signal transmission. The frequency of the

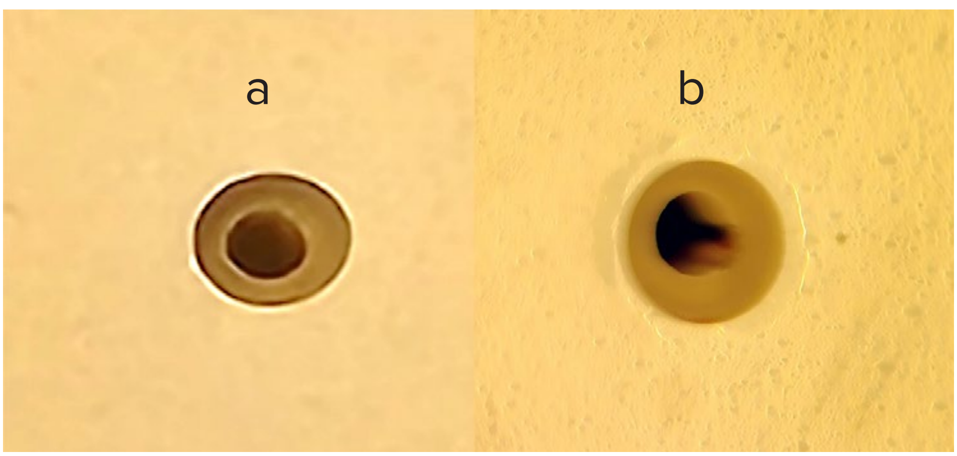

Figure 1: Photos of "good" and "bad" backdrilling.


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dip is inversely proportional to the length of residual barrel, and the depth and bandwidth of the dip depend on its shape. Usually, a narrower residual sliver means a narrower dip on the frequency plot.

Though this is clearly a manufacturing defect, it does happen occasionally because optical inspection of a high-aspect-ratio small hole is challenging. The length, width, and shape of any remaining barrel are highly statistical in such cases. Correlation can only be successful if we first find the defect and get the dimensions of the remaining barrel by further analysis.

The next example (Figure 2) is not the result of manufacturing defect; it can happen in any high-speed board. The case study[1] described the impact of registration tolerances on connectorized differential pairs. Coaxial connectors today tend to be much bigger than our typical trace width in high-density high-speed boards, requiring us to start with uncoupled traces until we can bring the two traces closer to form a differential pair. This inevitably means that the immediate vicinity of the connector launch—though they may be mirror images of each other—will not be identical.

The close-up photo of the launch via shows a case where the manufacturing tolerance pushed the via barrel sideways, further away from the exiting trace. We can then expect (as it was verified) that the via barrel in the other launch will get closer to the exiting trace. This minute difference is enough to create the highlighted difference in the TDR response. For such cases, the suggested solution of the cited reference is to exit differential launches with short parallel trace sections before the traces take a turn.

The third illustration, which is related to assembly, is reproduced[2] and is shown in Figure 3. Many of our complex packages today use a ball grid array (BGA) connection to the printed circuit board. These tiny solder balls are usually placed on a regular grid with a center-to-center spacing called the pitch. For big chips, 0.8 mm and 1.0 mm pitches may

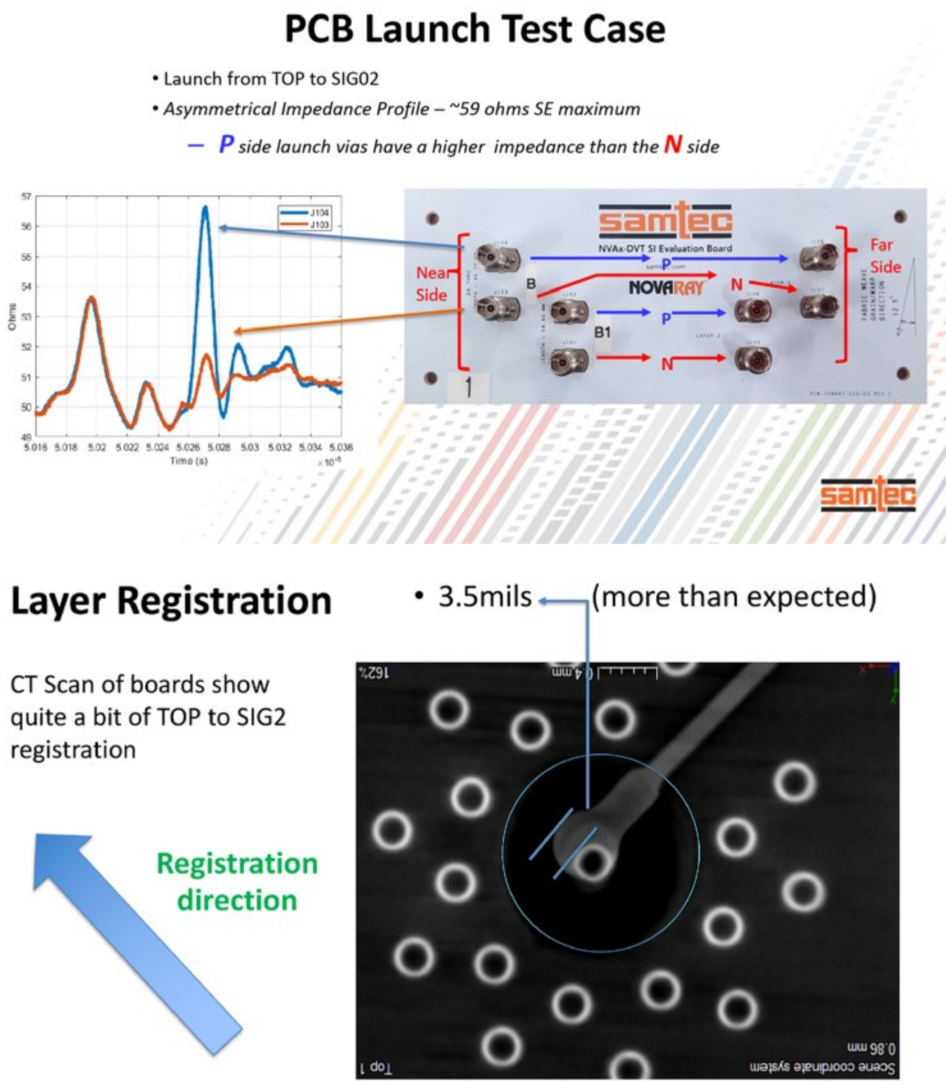


Figure 2: Effect of misregistration on differential escape (reproduced[1]).

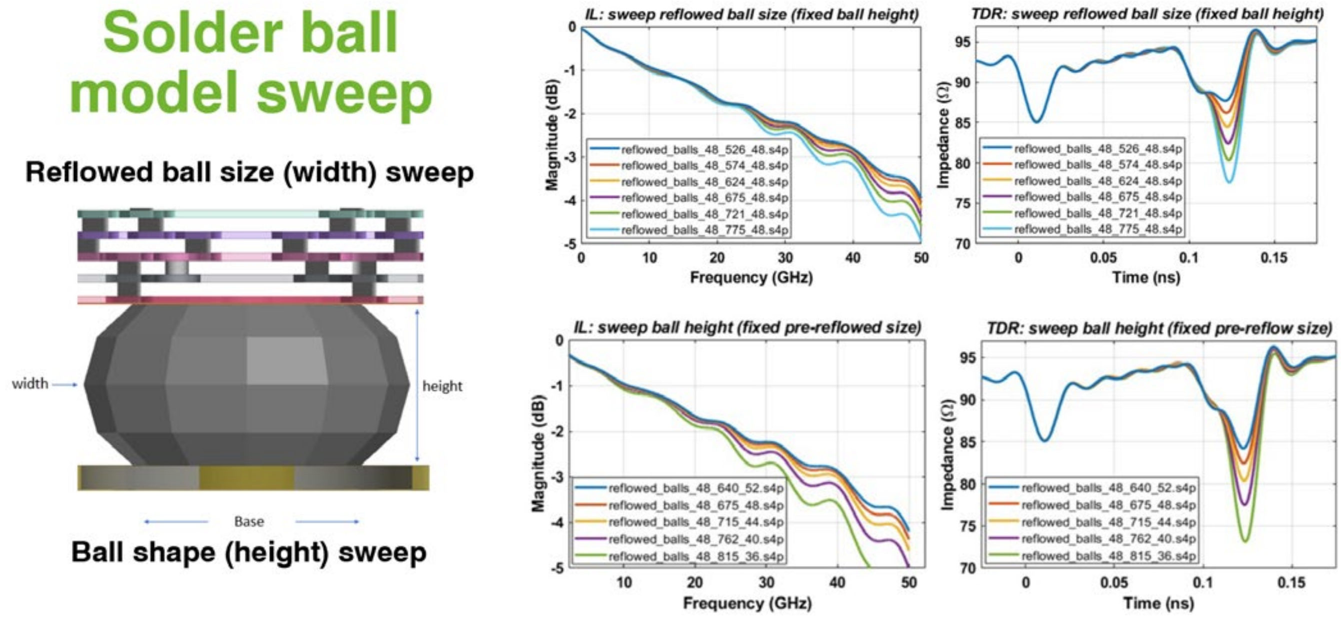


Figure 3: Effect of solder ball height on insertion loss and TDR profile (reproduced[2]).

be common. For smaller packages and higher speeds, smaller pitches are available. When we route differential pairs through a package, it is a good idea to place the balls connecting the two legs of the differential pair on adjacent grid points and surround them with enough return (ground) vias.

Return vias help to keep the impedance better defined through the transition between the board and package and provide isolation to and from nearby signal and power connections. During the solder reflow process, depending on many factors, the size and shape of the solder balls will end up being slightly different. These solder balls, no matter how tiny they look, still tend to be bigger than the connecting via barrels and traces. Therefore, seemingly small absolute variations in geometry numbers may result in very noticeable impedance, insertion loss, and crosstalk performance differences. Reproduced[2], Figure 3 shows the simulated performance as a function of solder ball dimensions.

Our final illustrations are related to power distribution. As opposed to the early days of electronic circuits, when carrying the power and ground connections around a board was done with wires or fat traces, to feed power-hungry chips consuming tens and hundreds of amperes today, we use power planes in our boards. When we define our stackup, the number and thickness (weight) of our power and ground layers, it is very useful to know a little bit about the processes of how printed circuit boards are fabricated.

To determine the current-carrying capability of a power-plane shape, we need to know the thickness and conductivity of the copper. Instead of thickness and conductivity, in the trade of copper foils, people use weight (you may hear about one-ounce or two-ounce copper) and method of production (electrodeposited or rolled/annealed copper). The recent "Mind Your Units" article[3] is a reminder that units matter, and the units used for PCB fabrication and trade may be counter-intuitive.

How the PCB copper is patterned during fabrication will also influence the current-carrying capability. During wet etching, the sidewalls of traces and plane shapes will become tilted. On a single large plane shape, this may matter very little, but when we have large

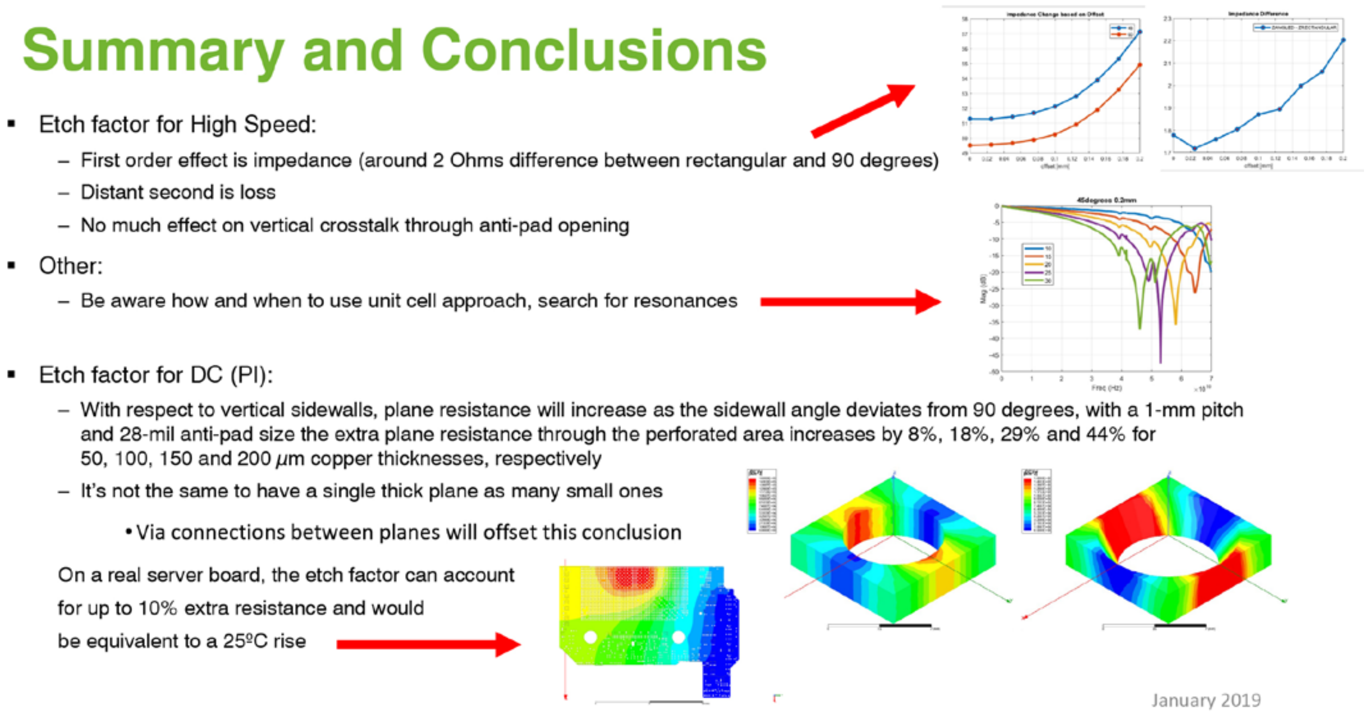


Figure 4: Effect of etch factor on DC resistance and loss (reproduced[4]).

chips in a dense printed circuit board, we end up with a lot of perforation due to the many antipads around vias that do not connect to the particular plane. This becomes obvious under the cores of big chips, where alternating power and ground through-vias perforate the planes. If we do not consider the slanted sidewalls, we may end up with a too optimistic design. The illustration in Figure 4 is reproduced[4]. It shows the simulated voltage drop on the power plane of a high-current CPU rail, assuming vertical sidewalls and the more typical 60-degree sidewalls. The etch factor alone results in a 10% increase of end-to-end resistance, on top of the impact of the perforation itself.

Summary

We need to be aware of the basics of PCB fabrication and assembly because they have an impact on the high-speed, power integrity, and thermal performance of our boards. **DESIGN007**

References

1. "Increasing Broadband Interconnect Characterization," EDICON 2018.
2. "A Case Study in the Development of 112 Gbps-PAM4 Silicon and Connector Test Platform," DesignCon 2021.
3. "Mind Your Units," Printed Circuit Design and Fab, Circuit Assembly, December 2023, p. 56.
4. "Etch Factor Impact on SI & PI," DesignCon 2019.

Istvan Novak is the principal signal and power integrity engineer at Samtec with over 30 years of experience in high-speed digital, RF, and analog circuit and system design. He is a Life Fellow of the IEEE, author of two books on power integrity, and an instructor of signal and power integrity courses. He also provides a website that focuses on SI and PI techniques. To read past columns, click here.

Laura Martin

Save Your Design by Understanding Fab Processes

Feature Interview by Andy Shaughnessy
I-CONNECT007

At PCB Carolina, I met with Laura Martin, director of applications engineering for Summit Interconnect. Laura has been at Summit for about a year, moving into the role from a similar position at Insulectro. She has now become Summit's go-to design for manufacturing (DFM) expert, and she's working to move DFM further up in the design cycle, eliminating unpleasant surprises at CAM.

Many DFM issues stem from designers not understanding all the steps in the manufacturing process. I asked Laura to share her thoughts on this situation, and she had several pointers for designers. As she notes here, many fab variables can put your board on hold, so it's best to be prepared.

Andy Shaughnessy: What are some of the most important things a designer should know about fab?

Laura Martin: One of the most common DFM findings is the via or plated through-hole pad size is designed too small to meet the specified annular ring requirements. I don't think it's well understood how to calculate the correct pad size, and IPC documents don't include some of the manufacturing caveats. We did a webinar on this topic recently, and one of the things we covered is how the type of final finish impacts the drill diameter. We compensate the drills differently for HASL and ENIG finishes. We also consider the aspect ratio of the board, and the total thickness or thickness of each sub being drilled.

If a copper plating thickness beyond IPC requirements is specified, that additional plating can impact the drill diameter we choose. So, it's not as easy as using the IPC formula to calculate the minimum pad size. Unless you know what the fabricator will choose for a drill diameter, then you might be off on your pad size calculation, which is why partnering with a fabricator when you're beginning your design is very important. The last thing you want to do is complete your entire layout, release it, send it to get fabricated, and suddenly the fabricator says, "You have to change the pad size." That can have a major impact on your layout, and you may have to allow exceptions to your annular ring requirements if you can't update your design.

Another common DFM finding is copper spacing. Most people know how to design for half-ounce, one-ounce, or two-ounce copper on print-and-etch layers, but internal and external plated layers are not as simple. Plating and fabrication processes can vary when there are multiple hole structures like buried vias, microvias, plated through-holes, or epoxy-filled holes. These features can impact the minimum spacing needed on the plated layers. Oftentimes, internal and external plated layer design requirements are not straightforward because they depend on the way the board will be fabricated. Is it getting planarized? Is it getting button-plated? How much copper will end up on each plated layer after processing? Not having enough spacing for fabrication can result in electrical shorts and low yield, so collaborating with the fabricator from the get-go is crucial. Frontloading this communication can prevent major hiccups down the line.

Another common DFM finding is copper spacing.

That's interesting. Even if the designers are following IPC specs, it's still possible to get things wrong if you don't work with your fabricator, because you may not be aware of their capabilities or limitations.

Exactly. Boards are becoming so complex that you have to work with the fabricator now. On a simple single lamination, with only plated through-holes, the fabrication process is pretty straightforward. But when you start getting into multiple lamination cycles, internal plated layers, and multiple-hole structures, it becomes more complex to fabricate.

Fabricators joke about how designers get all the matched impedance stuff right, but they'll put a connector too close to an edge or a component in the bend zone of flex. It seems like these little board-level errors put many jobs on hold.

Yes, there are many things that can put a board on hold. That's why having DFM up front is becoming so important. Many customers just expect it because they know that will catch most of the issues before they go into fabrication. So, we're trying to rise to that occasion and offer multiple solutions. Some customers just want a quick DFM, and that's good enough for them. Other customers want an in-depth review. By offering multiple solutions, we can provide that extra service.

Laura, I saw you last year at PCB Carolina, and since then you've moved into a new job at a new company. Tell me about your past year.

Shortly after last year's show I transitioned to Summit Interconnect as director of applications engineering. It's been an exciting journey as I assumed the responsibility of leading a department focusing on recruiting and training field application engineers. Our mission is to excel in technical support and customer service. Over the past year, I've enjoyed the process of establishing a department, introducing new processes, and innovating the way we approach DFM for our customers.

Traditionally, DFM has been a somewhat ambiguous concept in the industry. Designers often toss their designs over the wall and request a DFM without a clear understanding of what it entails. Many perceive it as a tooling department activity, involving running scripts, planning the job, and identifying issues in a technical query. While this is valuable, it consumes front-end engineering resources and may result in prolonged back-and-forth exchanges with the customer on design updates.

To address this, my team intervenes at the initial stages of the design process, even before it reaches the CAM department. One innovative solution we offer is called "preliminary DFM." This involves a semi-automated review where we thoroughly examine all design requirements. The ensuing report allows us to provide valuable insights, such as assuring designers that their design is manufacturable or identifying potential design rule violations. In cases where adjustments are needed, such as increasing pad sizes to meet annular ring specifications, or addressing challenges in etching small spaces on specific copper weights, we can intervene proactively.

This approach ensures that potential issues are tackled before the design is released or sent into manufacturing, preventing the common cycle of revisions and updates. Designers benefit from a personalized, one-on-one interaction with our team, leveraging our expertise in design for manufacturing and our in-depth knowledge of each of our shops' capabilities. Essentially, we aim to provide customized solutions that address a variety of needs.

Essentially, we aim to provide customized solutions that address a variety of needs.

With preliminary DFM, you're getting designers and fabricators to communicate, which isn't always the case. What are customers saying about this?

It's been received very well by customers. They appreciate the quick and insightful assessment of their designs, giving them confidence before committing to a full tooling DFM. It's a win-win situation. We avoid using up our front-end engineering resources on designs that might need extensive revisions, and designers get a more efficient, one-on-one interaction that addresses their specific design.

At last year's PCB Carolina, you were teaching a class on fabrication for designers.

Yes, that was my PCB 101 class. It delved into the basics of board fabrication, all the way from raw material to laminating, drilling and plating, and final finishes.

Are you an electrical engineer?

My academic background is in industrial engineering with a focus on manufacturing. It turned out to be a perfect fit for my journey. I started as a technician at an OEM, learning hands-on board building without a degree. After transitioning into front-end engineering, I pursued my engineering degree part-time. By the time I graduated, I had already gained a deep understanding of DFM and board fabrication. It was a seamless integration of knowledge and experience.

What are your plans for 2024?

The past year has been a whirlwind, and there's so much opportunity at Summit. Our focus on automation, customer obsession, and making the design-to-manufacturing handoff seamless are driving positive changes. I'm excited about the future and the chance to continue serving our customers in the best possible way. I feel like I'm just getting started, and there's so much more to accomplish in this dynamic and enjoyable industry.

It is a great industry. Thanks for speaking with me, Laura.

Thank you, Andy. DESIGN007

New Designer's (Partial) Guide to Fabrication

The Pulse

Feature Column by Martyn Gaudion, POLAR INSTRUMENTS

PCB designers fresh to the industry may think that once the schematic is loaded into CAD and routed out into XY data, the finished PCB is an "exact" copy of their XY data. That's not an unreasonable assumption for basic designs. Here, I'll outline some of a designer's considerations related to signal integrity as designs become more complex.

A False Assumption?

It may appear to the casual observer that PCB fabrication is "just" like PCB assembly. Even in casual language, when industry outsiders discuss making printed circuit boards, nine times out of 10, they imagine the assembly process rather than the PCB fabrication process. It's then a casual segue to consider that just as components are attached to a PCB with solder—but apart from that are unchanged from their raw form—the PCB itself is just that: a bonding of components unchanged by the manufacturing process. I've met many PCB designers and some EEs who slip into this assumption, especially that they can create a stackup "exactly" from the base material datasheet.

It's not a bad assumption on low layer count and simple low-speed boards, but as layer count and stack complexity increase in a design, it becomes increasingly necessary to know which layers are core or prepreg, which ones will press, and which layers the copper traces will press into. Experienced designers

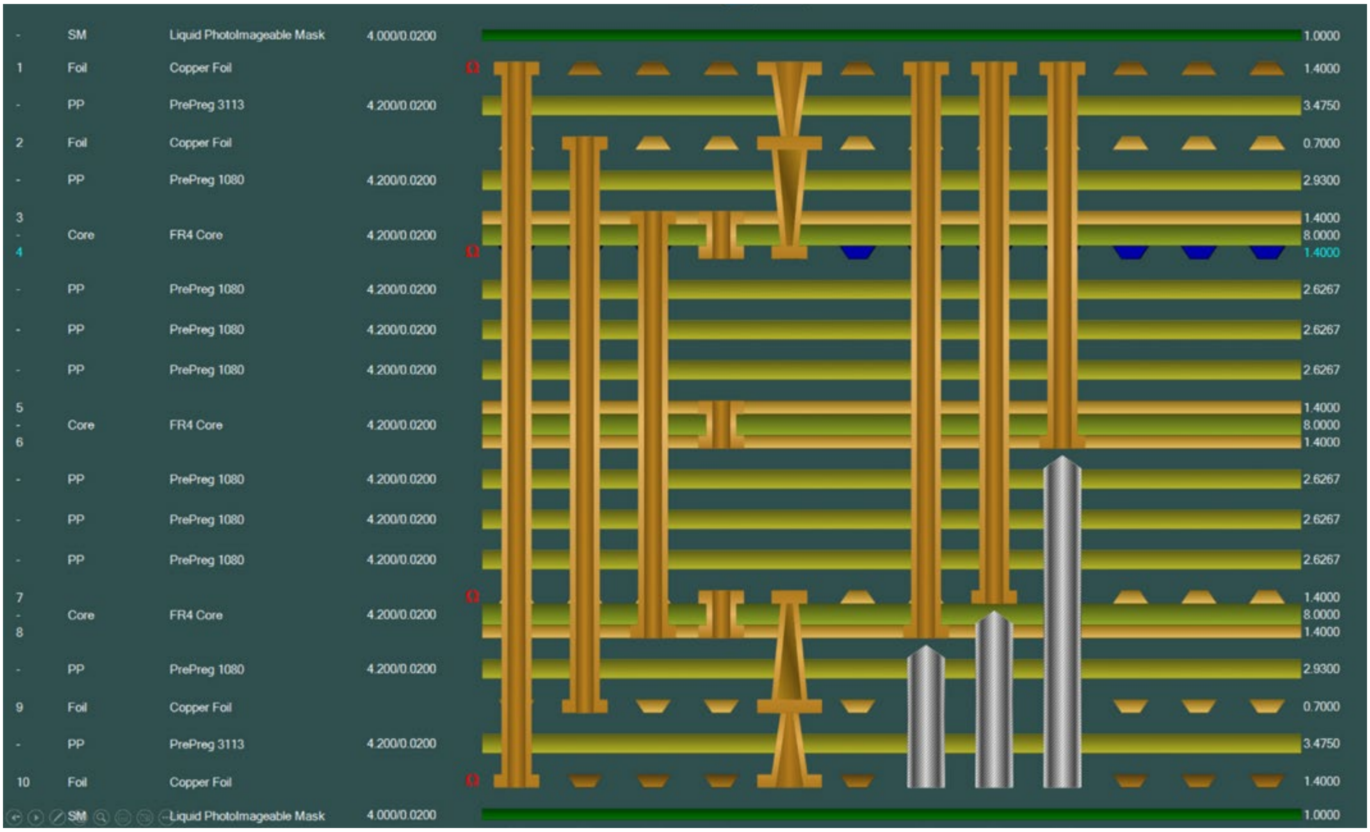


Figure 1: Schematic view of a stackup.

know that dimensions across core materials are quite predictable and the datasheet information is good to rely on. But suddenly, "it depends" when a foil is laminated onto prepreg, or two cores are laminated with prepreg with the Z-axis dimensions.

Datasheets and Interpretations

When you look at a stack schematic as in Figure 1, the labels showing core, prepreg, and the foils are separate from the prepreg materials. But to the uninitiated, it is not so clear what is pressing into what and which dimensions are fixed.

The schematic view of a stackup is a very clear illustration of the content of the stack, but it is not to scale, and more importantly, it does not show graphically where the traces impress into the prepreg, nor visually show the plated thickness on drilled or double-plated thickness on sequentially laminated traces where needed.

Figure 2 shows the schematic overview of the stack alongside a proportionally scaled view so you can see just how much the pressed stack varies from the schematic stack.

I have intentionally overlaid the proportional stack on the right of the schematic stack to show how the copper presses into the prepregs in contrast to the copper on the core side where its Z-dimension across the core is fixed. This illustration shows that new designers often wish to get accurate data from the material datasheet. The fact that PCBs are laid-up cores, followed by prepregs, cores, prepregs, and then foils means that the isolation distance between the copper on a core and the next core will depend on the amount the copper traces impress into the prepreg that flows during the heat and pressure of the press cycle. Stackup tools can make a good prediction of this, given the copper density of the tracking layers, but there will always be a degree of variation from fabricator to fabricator, depending on their press equipment and settings. This doesn't make the information on isolation dis-

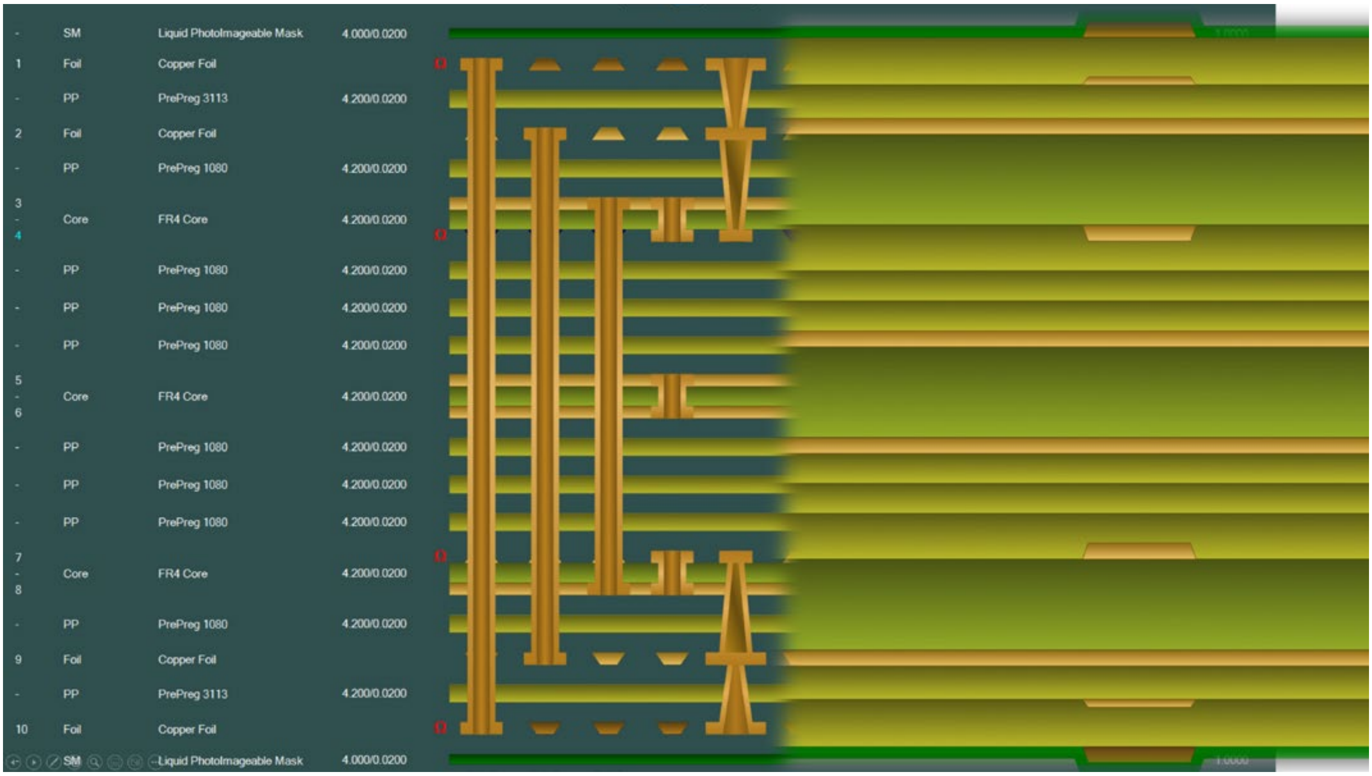


Figure 2: Side-by-side schematic and proportional view of the same stackup.

tance invalid, it's just that the designer needs more than a datasheet to make the height prediction. As always, if the designer has a good relationship with the fabricator (or a specialist broker), then good predictions and models can be made. Longer supply chains, though, can make this a challenge.

The isolation distance marked in Figure 3 shows the Z distance from the surface of a trace facing downwards from a core. It is pressed into the top of the three prepreg layers below. The stackup tool, in this case, is fed with the copper coverage percentage on each layer to assist in predicting how far the copper presses into the prepreg.

A good sanity check with this kind of calculation is to think of the limit situation. With 100% copper coverage (such as a ground plane), there will be no penetration into the prepreg. The same is true for the other limit situation: With zero percent copper coverage, again there is no penetration into the prepreg. The maximum situation is at 50% copper coverage where the resin in the prepreg will flow into all the gaps between the traces.

I've written this from the perspective of PCB thickness and isolation distances, but there are many other areas where it is very valuable for PCB designers to have an insight into the PCB fabrication process. A visit to a PCB fabricator is an enlightening and educational experience. From time to time, industry bodies like EIPC arrange such plant tours, and one such tour is taking place in southern Germany later this month. Visit eipc.org for more information. If you miss this one, be sure to keep your eyes open for another one or call your local PCB supplier and ask for a visit.

Conclusion

PCB fabrication is quite different from PCB assembly. In assembly, the parts are joined electrically and mechanically by soldering, but the components (including the PCB) travel through the process essentially unchanged. In PCB fabrication, copper is etched and plated,

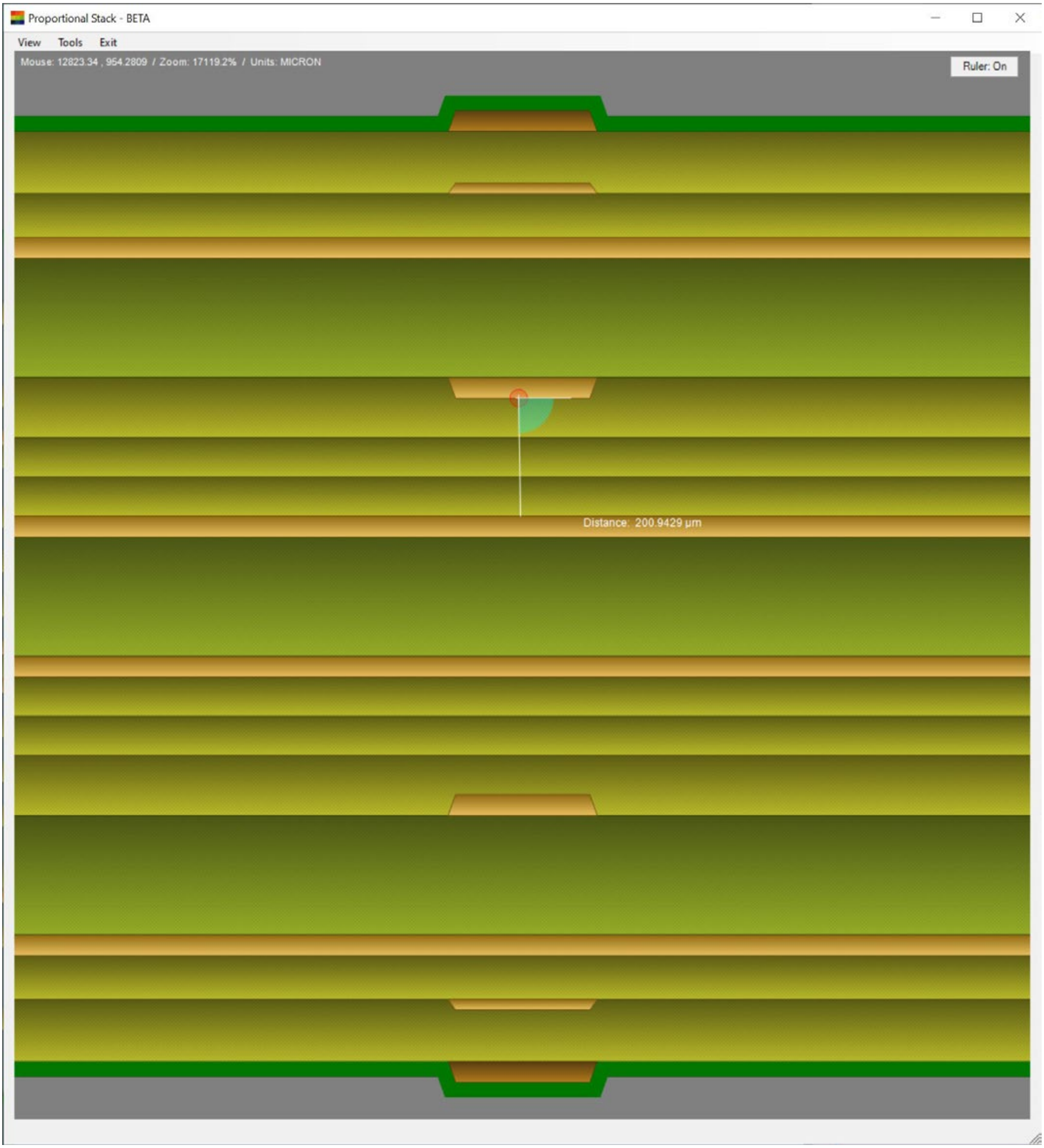


Figure 3: Proportional view expanded showing an isolation distance.

sometimes multiple times in sequential-lamination boards, and the prepregs change state as the resin heats and flows to a degree in the curing process. For that reason, a designer needs more than a raw material datasheet to understand how the PCB being fabricated will change in the process. DESIGN007

Martyn Gaudion is managing director of Polar Instruments Ltd. To read past columns, click here. Martyn is the author of *The Printed Circuit Designer's Guide to... Secrets of High-Speed PCBs*, Parts 1 and 2.

Flex007 Highlights

All Flex Solutions Installs New Inner Layer Factory ▶

All Flex Solutions has purchased and installed a new inner layer factory in their Rigid Flex Center of Excellence located in Minneapolis. This continues their investments in plants and technology to support customers' needs for capability, speed and increased yield.

Ventec Strengthens VT-901 / VT-90H Polyimide Supply Chain ▶

Ventec has further enhanced global supply chain resiliency for its global customer base. The new prepreg treater has enabled Ventec to ramp up capability and capacity at its Taiwan facility. As a first step, Ventec is now able to supply the full range of its VT-901 and VT-90H polyimide laminates and prepregs at high volumes, in addition to adding production capability to supply no-flow/low-flow prepregs for rigid-flex applications from this facility.

Eltek Placed Purchase Orders for $4.5 Million ▶

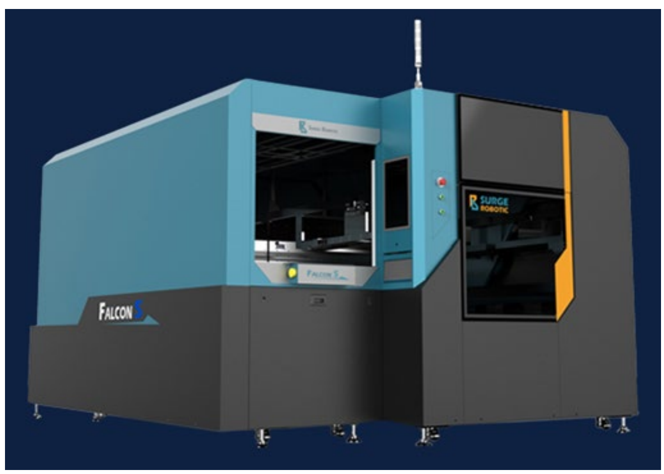
Eltek Ltd. announced the placement of purchase orders totaling $4.5 million for state-of-the-art machines, software, and a comprehensive service contract, with most deliveries scheduled for the first quarter of 2024, in connection with its planned expansion of its production capabilities.

Flexible Printed Circuits: A Design Primer ▶

Flexible circuits consist of conductive strips in a sandwich of insulating or dielectric material. They resist moisture and contamination and are insulated from external shorts, with holes or contact surfaces for interconnection.

Real Time with... productronica 2023: Ventec Now Also an Equipment Supplier ▶

Mark Goodwin announces that Ventec is now in the equipment business, as it were, now offering equipment under representation as well as equipment Ventec is now building. The equipment line matches up well with Ventec's core. Some equipment includes: Legend/solder paste, via fill, press plates, and more. These new offerings just demonstrate how Ventec continues to be a value-add supplier.



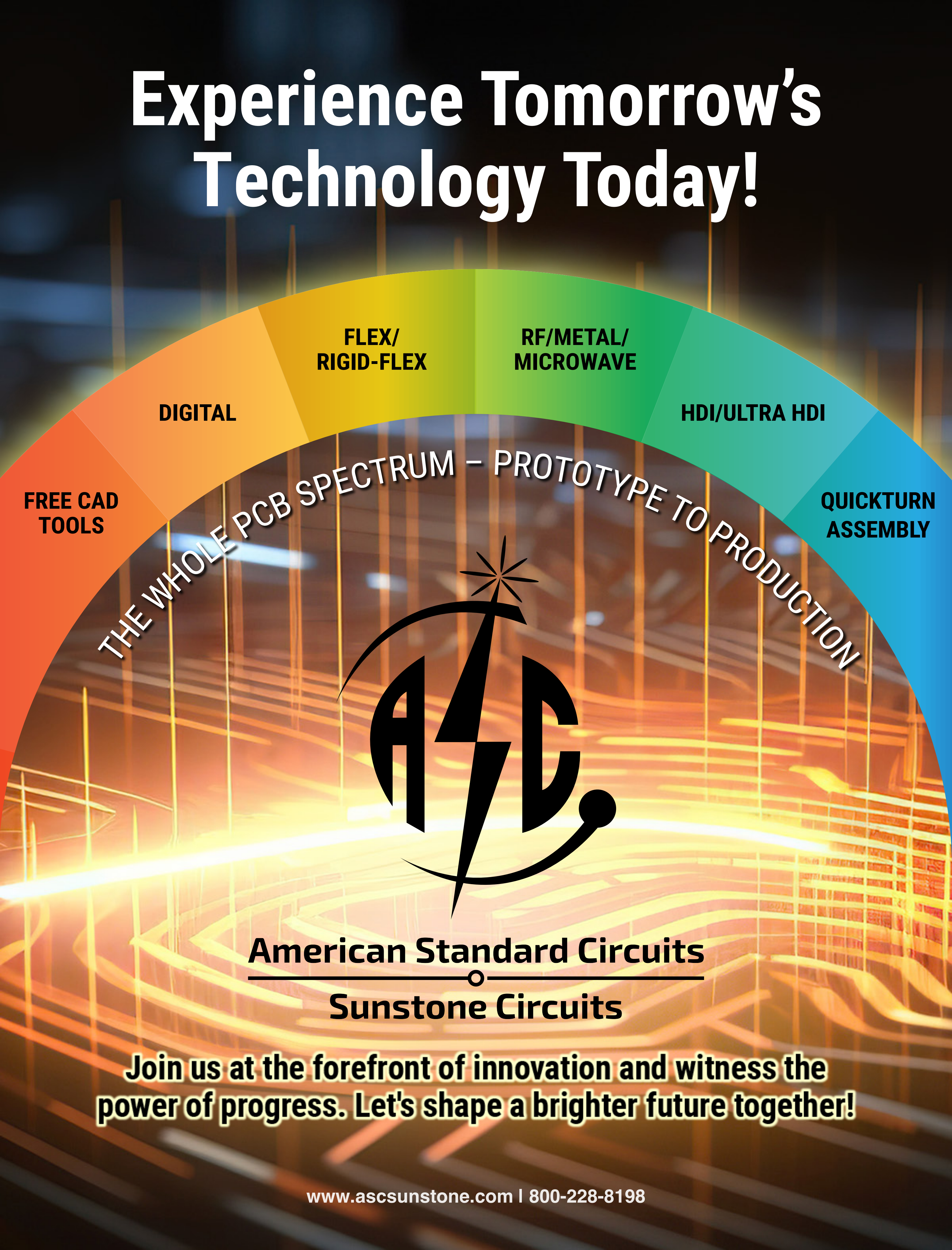
What Designers Should Know About Test

Feature Interview by Andy Shaughnessy
I-CONNECT007

Bert Horner, president of The Test Connection, Inc. (TTCI) in Hunt Valley, Maryland, has been helping PCB designers address design-for-test challenges, as well as the need to consider DFT early in the design cycle. I asked him to discuss some of the DFT issues that PCB designers need to be more aware of, and what designers can do to help PCB manufacturers avoid test problems farther down the line. As Bert says, many DFT snafus could be avoided if designers had a better understanding of the actual testing process.

Andy Shaughnessy: Bert, what are some things that designers need to know about designing for test?

Bert Horner: Of course, test is an integral part of the manufacturing process. Often, designers will design a board that works, but it may only work in a lab or a non-production environment. With DFT, there are really only a couple of key things that you'll need to consider. One is the controllability of parts; you want to be able to disable, control tri-state, and do certain things to have controllability of the card as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you're testing areas of the circuitry. You look around at the different control ports, and if you want to utilize things like boundary scan, make sure the five key pins have some kind of access, whether it's going through a header or a bed of nails, where you can access that point to utilize the boundary scan capabilities on the board. Then you'll have that controllability in utilizing test tools.

Also, be sure to have access to allow for enough power and ground points on the board so you have a balance and you don't have ground bounce. If you're looking at ICT, flying probe, or anything with a bed of nails, you want physical access so you don't have to have the big 0.032" points. Different probing technologies allow you to utilize smaller center-to-center spacings. You can use a through-hole device as a test point on a net; just utilize an unmasked via and call it a test via. Normally on a bed of nails, you don't want to go below 0.018" to .020" in diameter; you want to stay in 0.039", 0.050", 0.075", or 0.100" center-to-center spacing.

When you look at testability, controllability, having enough power and ground points on the board, and then the physical access, you realize that DFT could be setting up your test strategy. I know I will be looking at these bypass caps with AOI, and AOI or testing will be looking at this, so I don't need to have test points all over that part of that circuitry. If you're in RF, or even just high-speed digital, you might say, "I can't have test points hanging off that because there are a whole bunch of RCLs hanging off that location." Well, what can we test, and how do we test that high-speed portion of that board through a black box when not everything is high speed?

Then you can say, "I'll test the board using boundary scan," and if you have these things chained together, you know you're not dropping test points on the CCA. Designers should understand a good amount of the test strategy and how we run a test service. A lot of times, designers are not looking at that, and it's not really their fault. They're not building the board, or testing it in a production environment. You have to make the test stable, reliable, and robust enough that you can handle multiple boards if you are doing production over 100 or 1,000 pieces.

There are also limitations with flying probe DFT...

How does test change with production volumes?

If you're getting into tens of thousands of pieces, then you need bigger test targets, and you have to allow for panelization. The panel layout is something that a lot of people don't think about, and that's not always the function of the designer. That's the function of the manufacturer. Designers should be thinking about not only how manufacturers will build the board, but also how they're going to test the board. When all the boards on your panel are not facing the same direction, you will create a lot more challenges than solutions. You have to have some controllability on that.

You're really buying the panel, right?

Exactly. If you're a designer with an OEM looking at contract houses, you should know going into it what their test methodology is and not just throw it over the wall. Because if a contract manufacturer has an old Z1800, that will use a different test strategy than somebody who has a new Keysight 3070. If you have more and newer tools, you have more capabilities.

There are also limitations with flying probe DFT, where you will be probing on a joint. You need to know how you'll access these points and what your probing angle is. If you're coming straight down on a test target that's eight degrees, that will be handled a lot differently than coming down at zero degrees. The OEMs and the designers need to know what and how things can be tested, as well as the controllability and access on the board. But the manufacturer, contract house, or test development group must understand how that's panelized in the panel layout.

Other than talking to you, where can designers learn more about test and DFT?

At TTCI, we have our own guidelines for in-circuit and flying probe tests. I know XJTAG, Keysight Technologies, Goepel, and JTAG Technologies have DFT guidelines for boundary scan and tools. So, if you understand the test methodology that you're utilizing, there are documents available. But it's a challenge to have a standard uniform test guideline. There are so many different test methodologies.

If it's odd-shaped or highly populated, that can make it even tougher.

Right. You get some of these boards where you have a part of the circuit with a lot of devices next to each other. When it's very highly populated, it's hard to put in test points. But understand that you can access things through connectors. If someone is putting vias on the board and you can identify one per net, you can identify a potential test point. There are methods for getting around some of the odd-shaped stuff. DFT is very multifaceted.

Good stuff. Thank you, Bert. It's been a pleasure.

Thanks, Andy. **DESIGN007**

Chung-Ang University Scientist Develops New Antiferromagnetic Superconducting Spin Valves

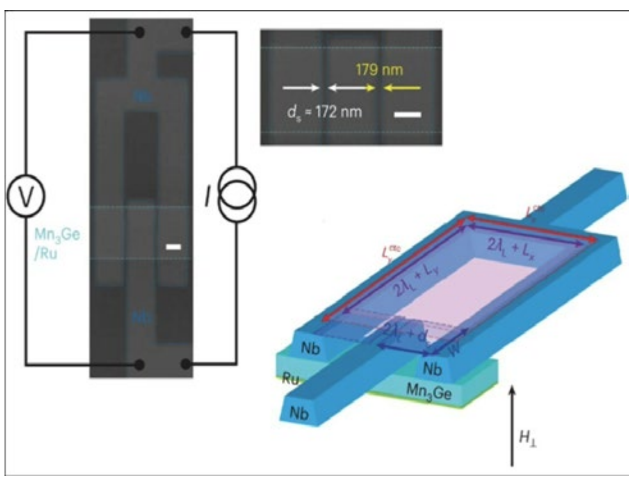
Superconductors are materials that offer no resistance to electrical current flowing through them. Combining their study with spintronics, which deals with the intrinsic spin of electrons and their use in electronics, has paved the way for the new field of superconducting spintronics. Developing intricate logic and memory circuits that utilize this unique behavior demands answers to two critical questions: how to efficiently generate spin-triplet Cooper pairs and how to precisely control their behavior.

In response to these challenges, researchers have engineered spin-triplet superconducting valves capable of switching superconducting currents on and off as per the need. These valves require only a modest external magnetic field to actively manipulate the behavior of spin-triplet Cooper pairs. However, they are fabricated from ferromagnetic Josephson junctions (JJs) consisting of a thin layer of the non-superconducting material sandwiched between superconductors. They require complex and delicate engineering to prevent interference from stray magnetic fields.

To make the fabrication of spin-triplet superconducting valves easier, a team of researchers led by Assistant Professor Kun-Rok Jeon from the Department of Physics at Chung-Ang University, Korea, has now developed an antiferromagnetic analogue of the spin-triplet supercurrent spin valves. While ferromagnetic materials are magnetically attracted, antiferromagnetic materials effectively cancel out magnetic fields, displaying no magnetic attraction.

Dr. Jeon highlights the broader implications of their work. "This study can advance the field of superconducting spintronics and potentially lead to a new generation of green supercomputers with much less operation energy compared with that of today's semiconductor technology."

(Source: Chung-Ang University)



Five Best Practices for Designing Flex and Rigid-flex PCBs

Connect the Dots

by **Matt Stevenson**, SUNSTONE CIRCUITS

Flex and rigid-flex PCBs represent exciting technology for designers. Suddenly, boards no longer need to exist along one plane—or along a flat plane at all. Designs can now conform to specific shapes or be bent during use, and this opens new possibilities for applications with space constraints or flexibility requirements.

Built using materials that can bend, a flex PCB is usually constructed with materials like polyimide and polyester film. These PCBs have many properties that designers might find useful beyond their flexibility. They have improved resistance to both vibration and movement. They are also significantly thinner and lighter than traditional rigid PCBs.

Flex PCBs do have some drawbacks, however. They can be more expensive to manufacture, and extra care needs to be taken for large or heavy components that may not be able to handle the flex. When these drawbacks seem problematic, rigid-flex PCBs are probably the best way to go.

Rigid-flex PCBs combine traditional rigid PCBs with flexible connectors. This approach offers better durability and mechanical stability compared to flex PCBs. While designs may lose some of the versatility of flex PCBs, combining traditional rigid PCBs and flexible elements brings the best of both approaches.

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Five Best Practices for Designing Flex and Rigid-flex Circuits

Of course, adapting to these new materials requires learning about their capabilities and restrictions, as well as learning a new set of design rules and best practices. Here are five best practices to get you started on your first flex or rigid-flex PCB design.

Before exploring these best practices, consider whether your PCB will be used in a static flex application—that is, it just needs to flex once during installation—or if it will be in a dynamic flex application. This important distinction can impact your design decisions.

1. Use curved paths for your flex traces.

Sharp angles can cause weak points in your traces across flex PCB segments. They tend to concentrate mechanical stress along the angles, so if you use curved paths for flex points, you will avoid cracking and weakening connections. This is particularly important in dynamic flex applications, where traces and conductors are subjected to repeated bending.

Figure 1: The example shows a cover-coated pad area in a Type 1 (single-sided) application. [1]

2. Use fillets to connect your traces to pads.

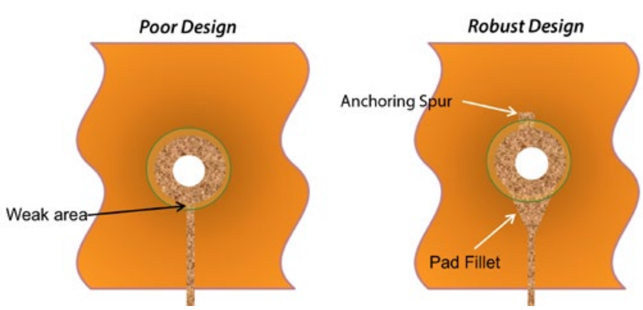

Figure 2: The example shows a cover-coated pad area in a Type 2 (double-sided) application.

A widened fillet can help reduce stress at connection points between traces and pads, greatly increasing the robustness of your design. Teardrop and rounded trace designs can reduce stress concentration points and prevent potential cracking or peeling around connections.

3. Make allowances for the coverlayer.

Unlike rigid PCBs, flex PCBs require an additional coverlayer to protect circuits and maintain flexibility. It is important that the coverlayer leaves room for various features of the PCB and for the interaction between the coverlayer and the flex board.

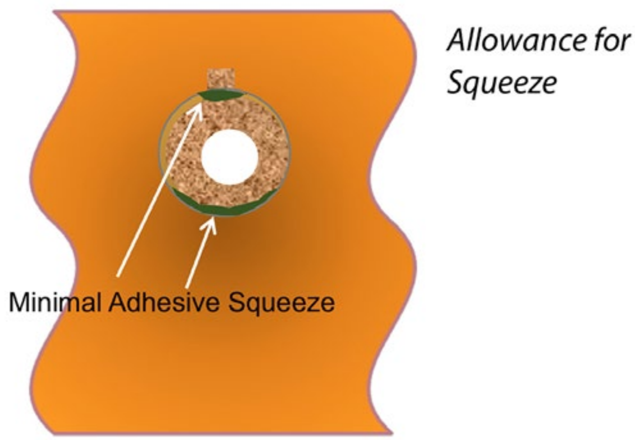

Figure 3: A coverlayer pad area in a Type 1, 2, or 3 application.

First, the coverlayer needs to be drilled to create access to the pad for soldering. However, it is important that the adhesive isn't squeezed out onto the pads. To accommodate for this, coverlayer drill holes need to be 0.005–0.010" larger than the land area.

In addition, this same allowance needs to be made for clearance holes in the coverlayer around through-holes in the flex PCB.

4. Layout considerations to be made for conductors and traces in dynamic flex areas.

Conductors need to be evenly staggered across areas of the board that will see regular flexing. If the circuit is repeatedly flexed perpendicular to the conductors, stress will occur

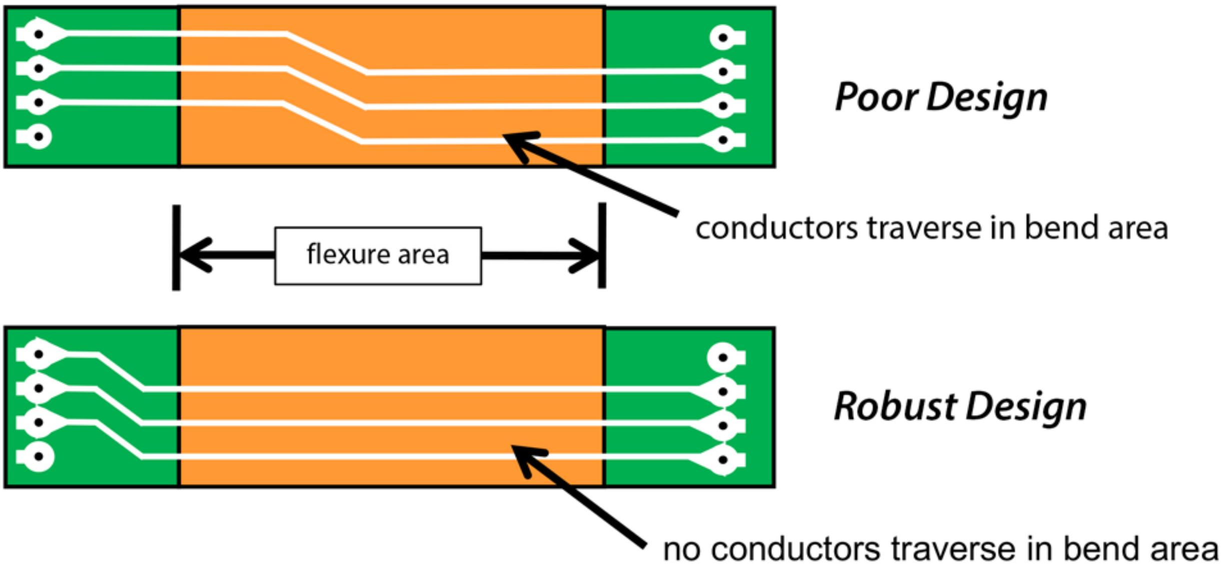

Figure 4: Note that the robust design is absolutely critical in flexing applications.

in the same location. This will cause any isolated conductors to crack prematurely.

However, when conductors are routed and staggered evenly, an isolated stress condition cannot develop. This ensures that no premature failure will occur.

In addition, be careful to avoid traversing conductors in the bend area. This can cause additional mechanical stress and can lead to cracking and failing traces.

5. Plan adequately for strain relief fillets.

Strain relief fillets are intended to prevent conductors from cracking during installation and are an important part of rigid-flex PCBs. Usually made from a two-part, epoxy-based

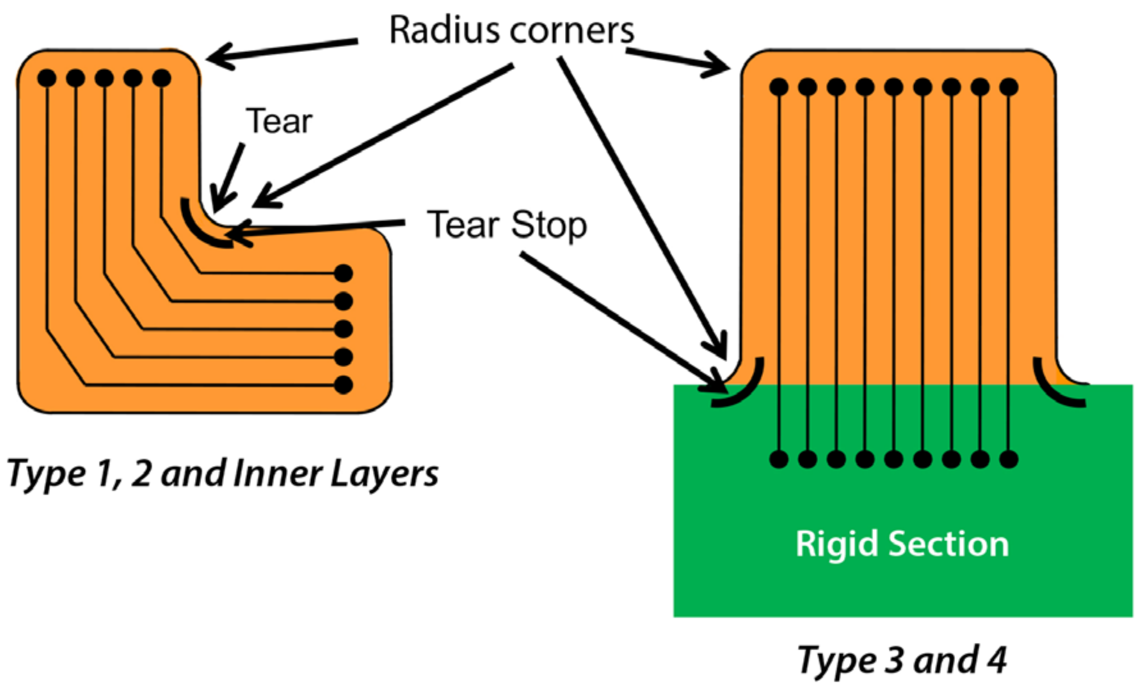

Figure 5: The purpose of the fillet is to prevent conductors from being cracked when the flex circuit is flexed during installation.

material, its main purpose is to prevent flex circuits from being bent at the transition point between flex and rigid PCBs. However, this material can also protect flex PCB portions from being damaged by "prepreg squeeze-out," which can create sharp edges along the sides of rigid PCB components.

Best Practices Make for Smooth Manufacturing

Flex and rigid-flex PCBs have opened a world of possibilities for designers. Their ability to conform to various shapes, along with a reduction in weight and size, has revolutionized the electronics industry. Designers now have the freedom to imagine and create products that were once limited by the constraints of rigid boards.

However, as with any new design component, we must remember the importance of following best practices when designing flex and rigid-flex PCBs. Attention to these details helps ensure optimal performance and reliability. Collaboration with experienced PCB manufacturers is also important for a smooth and reliable production experience.

Flex and rigid-flex PCBs are ready for designers to embrace. It is an exciting time when imagination and vision can be put to work to shape the future of electronics. **DESIGN007**

References

1. The images used in this column are from the American Standard Circuits book *"The Companion Guide to... Flex and Rigid-Flex Fundamentals, Tips for Designing Flexible Circuit Products,"* I-Connect007, 2023.

Matt Stevenson is vice president at Sunstone Circuits, a division of American Standard Circuits. To read past columns, click here.

Download *The Printed Circuit Designer's Guide to... Designing for Reality* by Matt Stevenson. You can view other titles in the I007eBooks library here.

PCB Market to Grow by $19.05 Billion from 2022 to 2027

The printed circuit board (PCB) market is set to grow by US$19.05 billion from 2022 to 2027. The market is estimated to be progressing at a CAGR of 5.05% during the forecast period. The report offers an up-to-date analysis regarding the current global market scenario, the latest trends and drivers, and the overall market environment.

Rising industry automation is an emerging trend shaping the market. As a result, several industries are forced to adapt to automation to sustain the competition in the market. But due to the increasing adoption, optimum power consumption can be a significant challenge. Hence, PCBs are increasingly adopted across industries to ensure efficient power consumption within the minimal size of the application. One of the main functionalities of PCBs includes withstanding peak temperatures and voltages. Hence, such factors are expected to drive market growth during the forecast period.

The market is driven by the rising adoption of smartphones. Factors such as the availability of low-cost smartphones and growing global Internet penetration are expected to fuel the adoption of smartphones globally. Furthermore, developing economies like India and China are becoming significant emerging markets for smartphones due to the rising disposable income of people and growing population.

(Source: PRNewswire)

What Matters When Designing Next-generation Products

Flexible Thinking

Feature Column by Joe Fjelstad, VERDANT ELECTRONICS

Since at least the 1970s, there has been a somewhat fungible mantra in electronics product development that has included two or more of the following descriptive adjectives: smaller, faster, lighter, better, and cheaper (often coupled with more rugged and reliable). Getting all of them simultaneously was not always possible, but if you paid enough, you could probably achieve it. However, it generally required the purchaser to give in to some commonly held "rules of the road" set down by the manufacturing community. When navigating the design process, what happens when the manufacturers want you to follow a road that does not take you where you want to go, or when standard practices are too constraining?

You can certainly decide to leave the path to gain benefits, but you should be aware of the risks and dangers that lie on the road less traveled. Robert Frost's timeless poem about that road left the reader with the impression that the results of choice were good—or not if you couldn't see the full length of the road ahead. With that in mind (and current knowledge), let's try to create a roadmap of sorts to see what might be done to make sure we reach our desired destination in a constantly changing design and manufacturing environment. Full


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disclosure: This will not serve to map the myriad concerns facing electronic product designers, nor will it detail where all the problems lie. Still, I hope to provide some guidance on important issues facing PCB designers.

First, all PCB designs are typically custom and unique; they are one-of-a-kind products. Unfortunately, they are also considered commodities, making them a "custom commodity" (an oxymoron). That said, the designer can try to comply with the needs of a commodity, which is to attempt to keep the dimensions orthogonal, if possible.

I trust we have all seen odd-shaped PCBs: round, polygonal, and mixtures of the two. Recognize that these boards are produced on rectangular panels and that missing material winds up in the trash. It was paid for, thus the admonishment. Still, it is not uncommon that the board must be designed for a specific product, such as missiles, which are (for ballistic reasons) invariably round. Thus, round circuit boards are designed to fit.

In general, when an odd-shaped board is inescapable, it will be necessary to design it for manufacture using a rectangular piece of laminate of a standard size, which is what the industry is tooled to do. This is true for both PCB manufacture and assembly. Thus the designer's odd-shaped design will not be manifest until it is freed from the assembled panel on which it was manufactured.

While on the general topic, it is highly advisable that designers invite themselves (or get invited) to visit their PCB provider before locking down their designs. We all read compelling stories about "bleeding edge" high-layer-count PCBs with line and space features of less than 75 µm, but is your vendor capable of such? This brings to mind other concerns relative to circuit performance, including one that has been increasingly important for the past few decades: controlled impedance and signal integrity. Dealing with these companion concerns requires the use of newer software tools that are designed to help address the challenges involving multiple material and feature design factors, including precision line dimensions, laminate dielectric properties makeup, and thickness. Even the "tooth" of the copper foil used can impact results.

Heat generation and its management are also of concern. There has been a tendency to pack more components into smaller spaces.

Heat generation and its management are also of concern. There has been a tendency to pack more components into smaller spaces. This impacts the signal integrity concerns as well as the thermal density of the assembly. Increasing thermal density has become a higher-order concern for product developers. Thus, heat mitigation has steadily risen in importance because of a known inverse relationship between heat excursions and an electronic product's reliability. Failure modes include solder joint reliability, plated through-hole integrity, and silicon chips' longevity. Again, modeling and analysis tools specific to thermal characterization should be desirably included in the design tool software suite.

I'm sure most of you are aware of the continuing evolution of wireless products that are now an indispensable part of our daily lives. With increasing expansion of the electromagnetic spectrum for wireless use, designers must be attentive to the susceptibility of their products to electromagnetic interference (EMI) and its potential to emit electromagnetic radiation that could impact products that surround it.

It's increasingly important to learn how best to mitigate or eliminate these concerns, and the designer must learn the best grounding practices as well as how to employ the best shielding techniques and incorporate EMI filters. In general, they need to follow established electromagnetic compatibility (EMC) guidelines.

My last item on this much-abbreviated list is meeting regulatory compliance requirements, which can determine whether your product can make it to the market. This means that the designer (or someone on the product design team) must stay informed about regulatory standards, perform pre-compliance testing, or, alternatively, involve regulatory experts and consultants early in the design process to ensure all aspects of the relevant laws and regulations are followed.

In summary, it is crucial to approach nonstandard PCB designs systematically, with a careful mindset, and considering all relevant electromechanical and thermal concerns as well as those that are regulatory, to ensure a successful product build. Close collaboration between PCB designers and experienced manufacturers is frequently the key to circumventing problems. **DESIGN007**

Resources

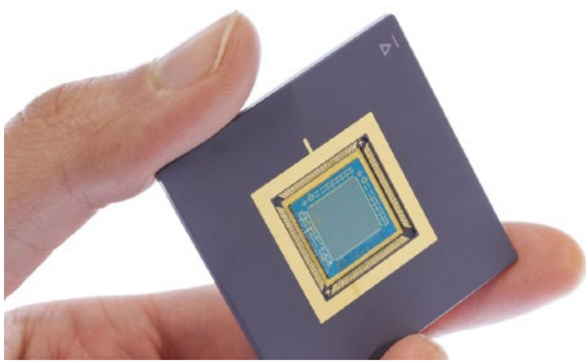
1. For more on the subject, read *"Flexible Thinking: DFM or Design With Manufacturing?"*

Joe Fjelstad is founder and CEO of Verdant Electronics and an international authority and innovator in the field of electronic interconnection and packaging technologies with more than 185 patents issued or pending. To read past columns or contact Fjelstad, click here. Download your free copy of Fjelstad's book *Flexible Circuit Technology, 4th Edition,* and watch his in-depth workshop series "Flexible Circuit Technology."

Redefining Energy Efficiency in Data Processing

As information and communication technologies (ICT) process data, they convert electricity into heat. Already today, the global ICT ecosystem's CO_2 footprint rivals that of aviation. It turns out, however, that a big part of the energy consumed by computer processors doesn't go into performing calculations. Instead, the bulk of the energy used to process data is spent shuttling bytes between the memory to the processor.

According to Andras Kis, who led the study, the main culprit behind the inefficiency of today's CPUs is the universally adopted von Neumann architecture. Specifically, the physical separation of the components used to perform calculations and to store data. Because of this separation, processors need to retrieve data from the memory to perform calculations, which involves moving electrical charges, charging and discharging capacitors, and transmitting currents along lines, all of which dissipate energy.



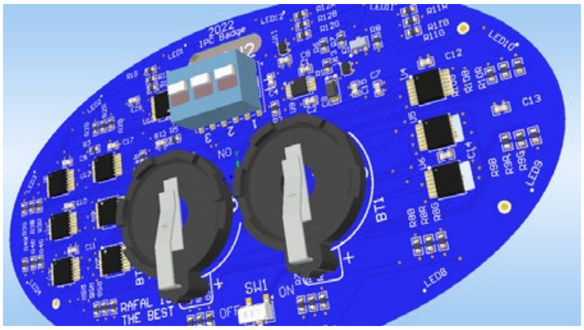
The choice of material—MoS_2—played a vital role in the development of their in-memory processor. For one, MoS_2 is a semiconductor, a requirement for the development of transistors. Unlike silicon, the most widely used semiconductor in today's computer processors, MoS_2 forms a stable monolayer, just three atoms thick, that only interacts weakly with its surroundings. Its thinness offers the potential to produce extremely compact devices.

Aside from its purely scientific value, Kis sees this result as a testament to the importance of close scientific collaboration between Switzerland and the EU, in particular in the context of the European Chips Act, which aims to bolster Europe's competitiveness and resilience in semiconductor technologies and applications.

(Source: EPFL)

TOP TEN

EDITOR'S PICKS



Register Now for the IPC Design Competition 2024

Every year, thousands of printed board design engineers spend countless hours completing and perfecting their designs. IPC is inviting these designers to put their skills to the test and compete to become the IPC Design Champion of 2024.

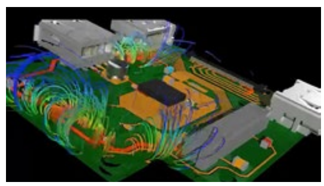
Engineering Their Future at PCB Carolina

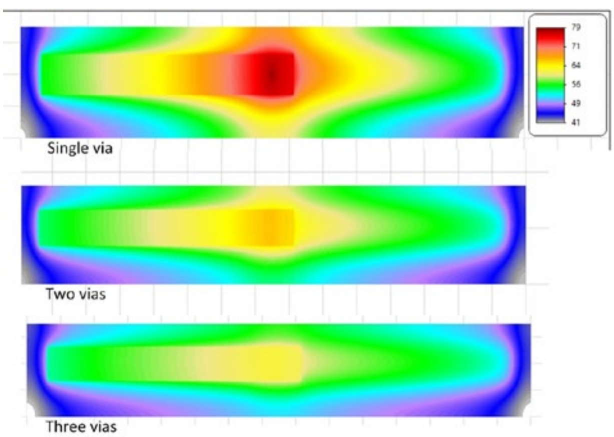
Cayden Longwell

At the PCB Carolina show in Raleigh, North Carolina, I had the opportunity to speak to several engineering students. I sat down for an interview with Cayden Longwell, a member of the class of '27 in the Electrical and Computer Engineering department at NC State. Even as a freshman, Cayden already has a basic roadmap for his career in electronics. Check it out.

Beyond Design: Return Path Optimization

Ground impedance is at the root of virtually all signal and power integrity problems; low ground impedance is mandatory for both. This is readily achieved with a continuous ground reference plane but becomes increasingly difficult with the addition of more and more plane layers on a multilayer PCB. A ground plane serves well as a signal return, provided the ground is continuous under the signal path.





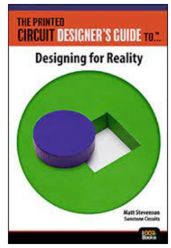
Your Thermal Designs Are Inefficient

Most designers rely on the trace widths suggested in IPC-2152, the "bible" for calculating high-current trace widths. IPC-2152 is the best, most thoroughly researched study of trace currents and temperatures available. But it does have some weaknesses. One weakness is that it (by necessity) studies 6-inch-long traces in isolation. But traces are not all 6 inches long nor in isolation.

Elementary, Mr. Watson: Consider Physics When Designing Non-traditional Geometries

One of the significant impacts of innovation on PCB shapes is the move away from conventional rectangular and square boards toward more customized and irregular shapes. These unconventional shapes cater to the specific requirements of diverse applications, such as wearables, IoT devices, automotive electronics, and more.

Book Excerpt: *'The Printed Circuit Designer's Guide to... Designing for Reality,'* Chapter 2



Once a CAD tool is chosen and the basics understood, the thought process should then shift toward the manufacturing of the PCB, before applying electrons to the screen. Let's get the "bad news" out of the way first. Perfection is an unattainable goal. Don't expect manufacturing to be perfect. There will always be variations from optimum at every step of every manufacturing process.

Unconventional Geometry Design Techniques

We asked design instructors Kris Moyer and Kelly Dack to discuss the challenges related to designing odd-shaped PCBs, as well as some solutions for designing today's boards that are anything but rectangles. What's the craziest-shaped board you've ever worked with?

EDA Tools and Unconventional Geometries—Designing Embedded Components

We asked Stephen Chavez, senior product marketing manager with Siemens, to discuss the company's approach to designing embedded components. He also explains how designers can take advantage of today's ECAD tools, which feature greater integration with the MCAD tool environment.

UHDI Fundamentals: Talking UHDI with John Johnson, Part 2

American Standard Circuits is an early adopter of Averatek's A-SAP process for its ultra-high density interconnect (UHDI) products. I had the opportunity to sit down with industry veteran John Johnson to discuss this. John previously worked at Averatek and is now vice president of business development at American Standard Circuits where he oversees quality. We will be discussing and sharing photos, slides, and materials with permission from both ASC and Averatek.

Target Condition: Designing Unconventional Geometries

I've worked on some LED light board designs with very complex geometry, particularly in my days designing boards for the gaming industry. Hitting the "auto-dimension" button on a design with so many arc origins and spline features would surely yield catastrophic documentation.

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- Excellent oral and written communication skills
- Business-to-business sales experience a plus
- Good working knowledge of Microsoft Office Suite and common smart phone apps
- Valid driver's license
- 75-80% regional travel required

To apply, please submit a COVER LETTER and RESUME to: Fernando Rueda, Americas Manager

fernando_rueda@kyzen.com

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Career Opportunities

Career Opportunities

INSULECTRO

Are You Our Next Superstar?!

Insulectro, the largest national distributor of printed circuit board materials, is looking to add superstars to our dynamic technical and sales teams. We are always looking for good talent to enhance our service level to our customers and drive our purpose to enable our customers to build better boards faster. Our nationwide network provides many opportunities for a rewarding career within our company.

We are looking for talent with solid background in the PCB or PE industry and proven sales experience with a drive and attitude that match our company culture. This is a great opportunity to join an industry leader in the PCB and PE world and work with a terrific team driven to be vital in the design and manufacture of future circuits.

apply now

MivaTek Global

Field Service Technician

MivaTek Global is focused on providing a quality customer service experience to our current and future customers in the printed circuit board and microelectronic industries. We are looking for bright and talented people who share that mindset and are energized by hard work who are looking to be part of our continued growth.

Do you enjoy diagnosing machines and processes to determine how to solve our customers' challenges? Your 5 years working with direct imaging machinery, capital equipment, or PCBs will be leveraged as you support our customers in the field and from your home office. Each day is different, you may be:

- Installing a direct imaging machine
- Diagnosing customer issues from both your home office and customer site
- Upgrading a used machine
- Performing preventive maintenance
- Providing virtual and on-site training
- Updating documentation

Do you have 3 years' experience working with direct imaging or capital equipment? Enjoy travel? Want to make a difference to our customers? Send your resume to N.Hogan@MivaTek.Global for consideration.

More About Us

MivaTek Global is a distributor of Miva Technologies' imaging systems. We currently have 55 installations in the Americas and have machine installations in China, Singapore, Korea, and India.

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Career Opportunities

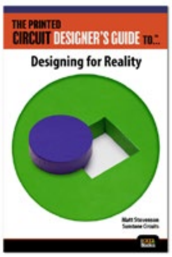
Educational Resources

Manufacturing Driven Design

by Max Clark, Siemens

This book introduces a new process workflow for optimizing your design called Manufacturing Driven Design (MDD) and is a distinct evolution from DFM. When defining Manufacturing Driven Design, it is important to recognize that this is, foremost, an element of the design stage. Manufacturing certainly plays a critical role in this process change, and manufacturers do certainly benefit from the improved process, but it is design teams that ultimately own their overall product workflow; they are the ones who need to drive this shift. Design teams are already invested in the success of their product; they just need to be empowered to control all the factors that go into this success. Get empowered now!

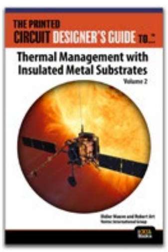
I-007eBooks The Printed Circuit Designer's Guide to...



Designing for Reality

by Matt Stevenson, Sunstone Circuits

Based on the wisdom of 50 years of PCB manufacturing at Sunstone Circuits, this book is a must-have reference for designers seeking to understand the PCB manufacturing process as it relates to their design. Designing for manufacturability requires understanding the production process fundamentals and factors within the process. Read it now!



Thermal Management with Insulated Metal Substrates, Vol. 2

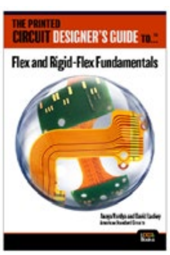
by Didier Mauve and Robert Art, Ventec International Group

This book covers the latest developments in the field of thermal management, particularly in insulated metal substrates, using state-of-the-art products as examples and focusing on specific solutions and enhanced properties of IMS. Add this essential book to your library.

High Performance Materials

by Michael Gay, Isola

This book provides the reader with a clearer picture of what to know when selecting which material is most desirable for their upcoming products and a solid base for making material selection decisions. Get your copy now!



Flex and Rigid-Flex Fundamentals

by Anaya Vardya and David Lackey, American Standard Circuits

Flexible circuits are rapidly becoming a preferred interconnection technology for electronic products. By their intrinsic nature, FPCBs require a good deal more understanding and planning than their rigid PCB counterparts to be assured of first-pass success.

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