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JANUARY 2014

RELIABILITY

Addressing Flux Corrosion & Reliability Concerns Early

Renee Michalkiewicz—page 20

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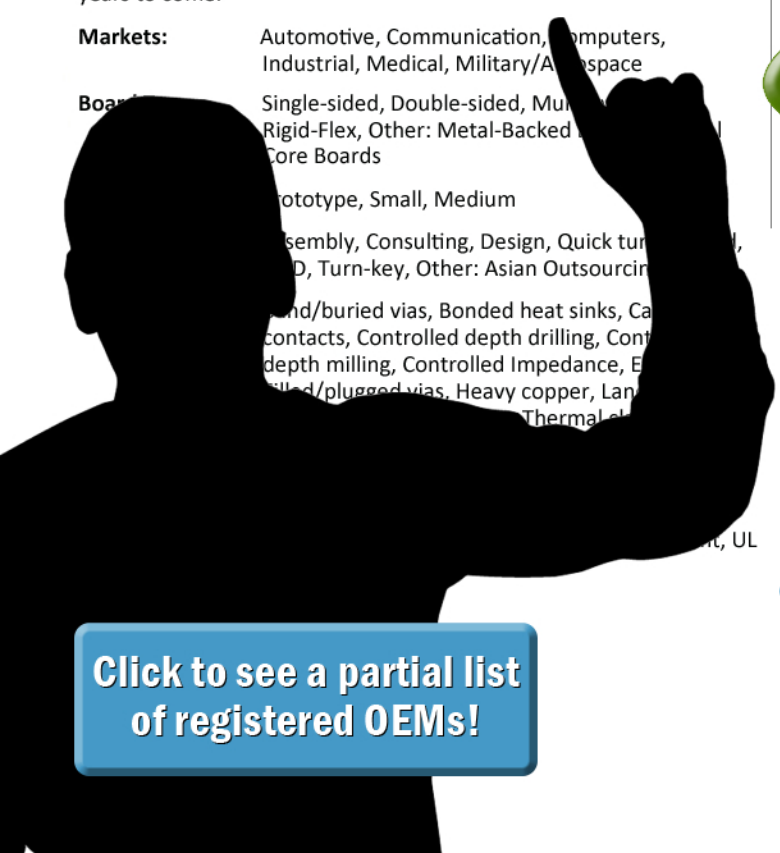

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January 2014 Featured Content

RELIABILITY

How can the reliability of an electronic assembly be assured? How does cleaning affect an electronic assembly's reliability? Is design a factor? This month, our contributors and columnists address these issues and many more. *SMT Magazine* wishes you a Happy New Year!

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JANUARY 2014
VOLUME 29
NUMBER 1
www.smtmagazine.com

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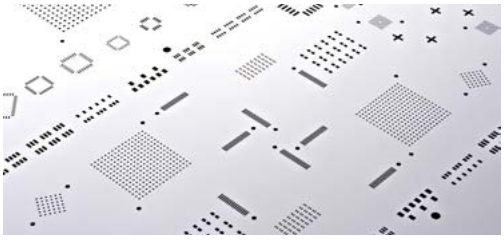
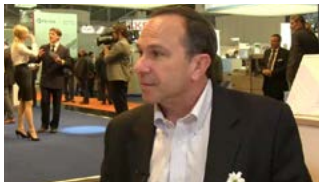




THE WAY I SEE IT

Printed Electronics Update

by Ray Rasmussen
PUBLISHER, I-CONNECT007

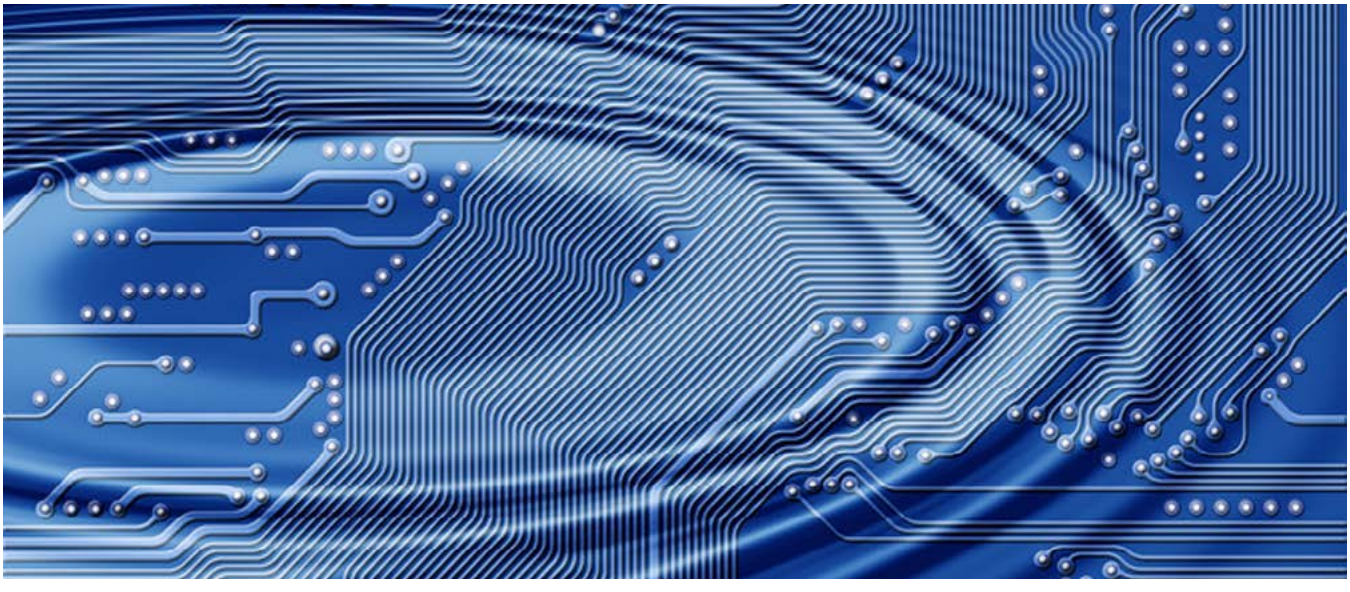
At IDtechEx this year in Santa Clara, California, I heard something for the first time: Several presenters said that they had replaced their PCBs with printed electronics. One of them was Multek (Flextronics).

When people talk about PE opportunities, they almost always focus on new markets and how PE is an enabling technology that allows electronics to be added to just about any product out there. In fact, there are some who suggest that it's possible to connect over a trillion products through the use of PE technologies, when they talk about The Internet of Things. It's really astounding.

Flextronics/Multek gave an interesting presentation about their efforts in PE. They're moving quite quickly into materials, thanks to their acquisition of Sheldahl and their flex materials. And as I mentioned, they are already replacing PCBs with PE circuits.

PE for EMS

A few years ago, I invited Matt Timm, CEO of Soligie, to keynote an IPC conference on printed electronics that I was emceeing. Soligie is a PE contract manufacturer: EMS for the PE industry. I had invited him to talk about the current status and prospects for the future. Timm spent a lot of time talking about the hype curve and how the industry was starting to come down the backside of the curve, which was the more realistic state of the industry. Still exciting, but the reality was that PE technologies were going to take longer than the pundits had been espousing. He was in the trenches and had a good perspective on things. Something he said to me offline, which I found quite interesting, was that his biggest concern with our industry was the giant EMS providers like Flextronics who, when they figured out the opportunity, would eat his lunch. Well, I think they're starting to do just that. It's still a specialty market for them but it's going to grow really fast. They already have the customers. Now, they just need to match the PE product with the right customer and application. The customers want it. On the EMS side, the opportunities are almost endless. They do everything needed for PE in-house, on their own, wherever the customer is located. They can mix and match conventional technologies with emerging PE options when and where needed. They're in a great position to dominate this market in fairly short order.



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PRINTED ELECTRONICS UPDATE *continues*

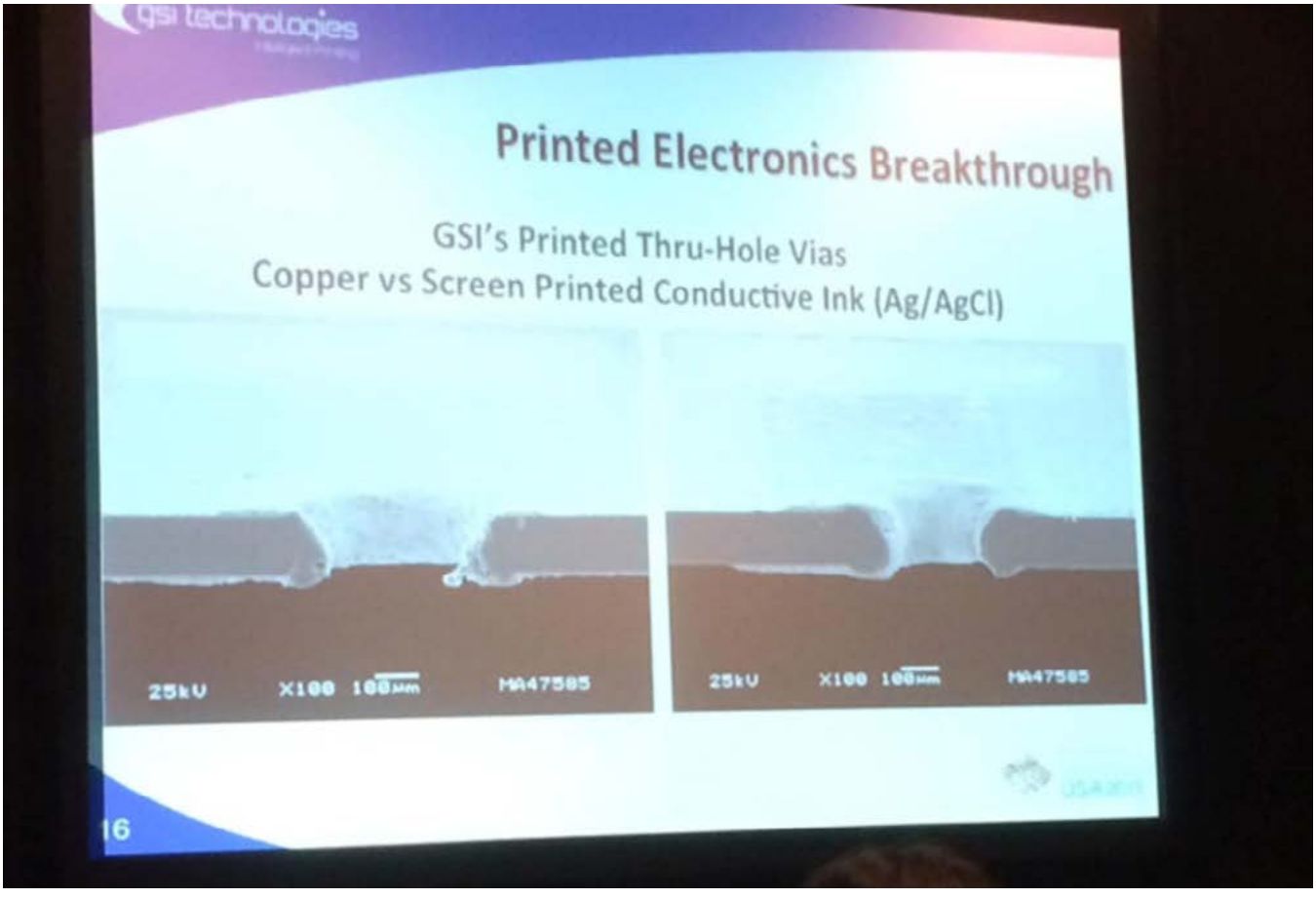

Figure 1: A slide from GSI's presentation on printed electronics.

PE for PCB

I ran into John Andresakis from Oak-Mitsui who, like me, has a keen interest in printed electronics. As we discussed some of the technologies and presentations we saw at the show, I suggested that we need an annual technical benchmark to show the progress of the PE materials and capabilities as they relate to PCB technology. It would be important for the industry to know how rapidly the PE capabilities are advancing. Certainly, the most obvious target for PE is the flex circuit industry. Flex PCB suppliers are already selling their latest materials at PE shows. Lots of companies are selling materials into this market. Conductive inks are everywhere and they're getting better and better every year. It won't be long before they perform like copper; then, watch out!

Figure 1 is a slide from GSI Technologies touting their "printed thru-hole vias." GSI was a printing company that has made the jump into printed electronics.

In a presentation from PragmatIC, the CEO caught my attention. Basically, he said that the closer they get to free (referring to the cost of their product, which is printed memory), the larger the market gets. I've heard these kinds of statements before, but the way he put it made a lot of sense to me. At a higher price point, the market is limited. The higher you go, the smaller the market. If you go high enough, you reach the costs of traditional electronics, which is the market we're all very familiar with. I get all this. It's logical and makes sense. Very few of our manufacturers are looking for ways to reduce the cost of their boards for their customers. Typically, we fight every price change and try to not leave any money on the table. The problem with that thinking is that it closes the door on a ton of potential that the PE

guys have grabbed hold of. That's the way they think.

Driving down cost as quickly as possible to expand the market makes a lot of sense to them. You could say that the Chinese, and in particular, Foxconn have also grabbed that concept by building boards and assemblies in an environment that allows them to dramatically reduce costs; this has opened up a much larger market for electronics than would have otherwise existed. Now, most of the world can afford electronic products, which were mainly sold in developed countries. As a result, all boats rise. More electronic gadgets require more electronic infrastructure, which creates more jobs which then provides more income and more buying power, etc. Now, PE takes this cost reduction to a whole new level. In just a few years everyone, everywhere, will have access to most of the technologies out there and printed electronics will make that happen.

As I mentioned last month, in a recent assembly industry technology survey, printed electronics was the topic of greatest interest. Although not surprising to me, it does indicate that our industries are finally waking up. And as I said earlier, the EMS companies are in a prime position to leverage the capabilities of PE technologies for their customers. My biggest concern is with the PCB fabricators. There is both a great opportunity and an ultimate endgame for many. I'm not sure why there aren't many more fabricators walking a show like IDtechEx. I only saw a few (Sunstone, Viasystems, Multek). Maybe I'm way off base, but I don't think so. **SMT**

Ray Rasmussen is the publisher and chief editor for I-Connect007 Publications. He has worked in the industry since 1978 and is the former publisher and chief editor of *CircuiTree Magazine.* To read past columns, or to contact Rasmussen, click here.

Video Interview

Hamed El-Abd Offers His 2014 Forecast

by Real Time with... HKPCA

Hamed El-Abd, President of WKK reflects on the past year and gives his forecast for 2014. Hamed reports the increase in world-class Chinese capital equipment manufacturers that are exhibiting at this year's HKPCA & IPC show.

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SMT PERSPECTIVES & PROSPECTS

New Year Outlook: What Can We Expect in 2014?

by Dr. Jennie S. Hwang
CEO, H-TECHNOLOGIES GROUP

Once again, it is the time to look at the year ahead. This is a relished tradition as I am on the spot to think critically about the next 12 months and then have the opportunity to cross-check the predictions 12 months later. My 2013 outlook was, by and large, on or very close to target (Year-in-Review, December 2013). In this piece, I will take a long view on market thrusts in the anticipated global economic landscape, as well as technological trends in selected areas deemed important and relevant to the industry, which are tailored to the target readers of this magazine. Each of these areas will be highlighted, but more detailed discussions will be addressed in my future publications and speeches.

Global Economic Outlook

Overall, the U.S. economy in 2013 was not too hot and not too cold, rendering the Federal Reserve's inaction in rolling back the stimulus program in bond buying. In 2014, the first and second largest economies, respectively, U.S. and China, are expected to show improved outlooks over 2013, while the third largest economy, Japan, launches bold new fiscal policies and economic stimuli. With Japan holding the highest debt levels in the world (at 230% of GDP), Abenomics needs to show real progress; it will be a tricky maneuver. China and Japan both happen to have recently installed new leadership, which will exert new influences and economic policies.

Across the Atlantic Ocean, progress has been made. The signposts indicate that the financial crisis is ending in the Eurozone. Countries such as Italy and Spain are exiting recession. However, the ECB is pondering the challenge and impact of the worryingly low inflation rate. The U.K. sees recovery gaining pace. The Bank of England believes the U.K. economy is recovering so quickly that it will likely consider raising interest rates in 2014[1].

However, a sound economy exists only if there is political and social stability. To that end, the standoff between China and Japan over territorial disputes could skew the global economies if it escalates to a dangerous stage. Such an escalation is unlikely, but not impossible. Eschewing any adverse complications calls for one of the most sensitive and intricate ex-

NEW YEAR OUTLOOK: WHAT CAN WE EXPECT IN 2014? *continues*

ecutions of the U.S. diplomacy and the foreign policies. Navigating between the two disputing countries takes more than the assessment of the current parameters and environments. It also needs both retrospective and prospective understanding of the two countries in relevant economic, political and cultural terms, which are profoundly complex. Brinkmanship would not be an effective tactic. A gingerly and delicate treatment is in order.

The year 2014 appears to be an extension of another relatively low interest rate economy even with a modest interest rate increase, which is good for borrowing money to conduct business and corporate-finance activities. The 2013 U.S interest rate of 0.25% was at a historical low, far below the average (6%, with the all-time high of 20% in the 1980s), and the Eurozone was at 0.25%, also a record low, and U.K was at 0.50%.

In corporate America, a rising tide (stimulus and low interest rate) has raised all boats in the stock market. But many premier companies are taking a hard look at their business strategy and focusing on enhancing operating margin and profitability. It is an arduous and critical thinking process, but it has to be done in order to be competitive. This process includes where and how the cash-rich multinational corporations (collectively holding more than $1 trillion in cash) are going to invest—overseas or domestic; dividend increase or share buyback; operation expansion or mergers and acquisitions. The strategic outcome will impact the job market and the U.S. economy, as will government policies and tax reforms. At the date of this writing, December 1, 2013, the U.S. fiscal policy's holding pattern poses uncertainty and risks to the 2014 economy, and thus to corporate actions.

Judging from the Chinese government's decision not to pump funds into the economy and its implementation of new reform policies, the commodity prices, tightly linked with the supply and demand dynamics, are expected to stay flat or decline further. Another good sign is that U.S. manufacturing activity is in upward trajectory[2].

Going into 2014, the U.S. unemployment rate should see moderate improvement, hovering around 7%, but reaching the 6.5% milestone is perhaps a stretch, unless the new Fed Chair's emphasis on employment out of the central bank's dual mandate—maximum employment and stable prices—exerts "miracle" muscle on reducing unemployment. And the Eurozone continues to struggle with a double-digit high unemployment rate.

> ***"With increased underlying strength, the U.S. economy is expected to grow at a faster pace than 2013, barring political debacle in Washington."***

2014 is also the year that the U.S. Federal Reserve looks for clarity on growth in order to taper bond buying. In my view, the Fed should and perhaps would pare back the stimulus in the spring (if not in December 2013), at least moderately. With increased underlying strength, the U.S. economy is expected to grow at a faster pace than 2013, barring political debacle in Washington. There is a good chance that the U.S. GDP may recover to 3% or better.

Overall, for the first year since 2008, you don't have to be an optimist to see the glass as half full. And China's economy (as does its politics) continues to be a factor!

China Factor

China is gaining traction in global trade. The country has just hit another milestone as the use of the yuan (renminbi) in trade finance overtook the euro and the yen, although the yuan is still far behind U.S. dollar. This is not to say that China's banking and financial systems are well established. However, this milestone indicates that foreign (non-Chinese) companies are getting more comfortable trading in Yuan, in addition to garnering some pricing advantages.

It is crucial for China's new leadership to implement structural reforms in 2014. Within the context of "planned reform," the timing

happens to be good from the standpoint of the state of the world economy. With all three of its largest trading partners in a slow growth mode, China has more a reason to gear up its consumption-oriented economy to spur long-term growth, sustainability and social stability. Its government increasingly recognizes the market role in economy in order to move to a sustainable path that is to depend more on domestic demand and less on exports and government spending. The country has just formed the National Development and Reform Commission to design and coordinate its reform. The new leading group's duties, apart from economic reforms, are to plan and carry out reform on modernizing China's "governance system" and "governance capability." The core issue of the reform is "to better handle the relationship between government and the market"[3].

With the formidable task in hand, the country's stability is the new leaders' number one "wants and needs." Consequently, the official growth target is not expected to be higher than 7%. However, take note that, in practice, China has always exceeded its target in recent years.

China's twelfth Five-Year Plan is the national master blueprint to achieve medium-term economic and social objectives. The country must stay on its course to develop seven strategic priority industries: new energy (e.g., nuclear, solar, wind); energy conservation and environmental protection (e.g., energy reduction target); biotechnology (e.g., drugs, medical devices); new materials (e.g., high-end semiconductors, rare earth); new IT (e.g., broadband network); high-end equipment manufacturing (e.g., aerospace, telecom equipment); clean energy vehicles.

China plans to provide financial and tax support to these industries over the next decade in hopes of making these sectors account for around 8% of China's GDP by 2015 and 15% by 2020. The broad-based goals to be achieved are: sustainable growth; moving up to the value chain; reducing disparities; scientific innovation with R&D spending increase to 2.2% of GDP; environmental protection; energy efficiency; and domestic consumption.

To foreign companies, these goals bear a plethora of business implications. I see specific opportunities in individual areas and industry sectors.

For Chinese companies, iconic branding is a dream come true. Many have gained understanding on what it takes to globalize through the thoroughly planned strategy executed relentlessly over sustainable years—Samsung and Singapore Airlines are two admirable models. As more indigenous companies aspire to be a global brand, more global competition in all industry sectors is in the works.

Electronics Industry: Hardware

Five words cover the essence of electronics hardware: smart, mobility, connectivity, wearability and innovation.

Technology never holds still. Technology advances will prop further mobility and connectivity in 2014. The growth and volume of electronics hardware will be driven by mobile devices, and high reliability and high performance electronics will propel new materials innovation.

In semiconductor sector, Intel, the top captive semiconductor manufacturer since its inception, made an astounding announcement that the company will open up its fab factories to outside business, serving as foundries as well. The company will compete head-on with other giants, such as Samsung and Taiwan Semiconductor Manufacturing Company (TSMC). Its unprecedented strategy of giving up its long-standing captive status will change the dynamic of foundries business among the top players, and may spill over to the industry.

"In semiconductor sector, Intel, the top captive semiconductor manufacturer since its inception, made an astounding announcement that the company will open up its fab factories to outside business, serving as foundries as well."

NEW YEAR OUTLOOK: WHAT CAN WE EXPECT IN 2014? *continues*

In manufacturing technology, 28 nm node has demonstrated high yield and low-cost manufacturing. Samsung and TSMC reportedly will use the 20 nm node technology to manufacture Apple chips in 2014. Additionally, the manufacturing prowess in 14 nm node will be unveiled by Intel. As the 20 nm is being established, 2014 is also the year to lay the ground work for developing 10 nm capability on 450 mm wafers.

Building chips on 450 mm wafers in volume production is moving forward by both OEMs and foundry manufacturers. Establishing 450 mm wafers are a major technological move, so is to further shrink transistors below 20 nm. These plans and commitments will lead to further advances in the chip industry to deliver increased functionalities and reduced cost in electronic and optoelectronic products that serve a broad spectrum of industries. In the wafer fab equipment market, a year-over-year growth rate of more than 30% brings 2014 to the projected spending of $39.5 billion.

In optoelectronics, new materials for LEDs, such as gallium nitride-on-silicon, is expected to see market penetration in 2014.

As ICs move to 20 nm and below, a continuing effort to make the next levels of connections to reach the end-use products calls for new designs and new materials in the second level IC packages and the third level connection in PCBs. In 2014, major new thrusts are not in sight for the second and third levels of inter-connections, yet activities are abundant that offer gradual technological advances, including optical inter-connections, embedded devices and printed electronics. The development in high density packages, including 3D packages, system-in-package and BTC packages will continue. Overcoming the design and manufacturing hurdles, the packages with 0.3 mm pitch BGA architecture will be entering into the mainstream.

To maximize the yield and reduce cost, PCBs' thermal stability, under the high manufacturing temperature imposed by the assembly process, continues to be the most critical performance parameter. Although a PCB possessing a higher glass transition temperature (T_g) is readily available, T_g, per se, does not represent the PCB's heat tolerance ability. Other properties, such as mechanical properties, thermal decomposition temperature, thermal expansion over a temperature range, out of plane and in-plane thermal expansion and moisture absorption all contribute to the overall performance (i.e., internal structure integrity).

Electronic Hardware Manufacturing

Going forward, the three business models in electronics hardware manufacturing, OEM (original equipment manufacturer), ODM (original design manufacturer), and EMS (electronics manufacturing services) will shift and the demarcation among them will be blurring. The challenge to companies will be crafting a clear vision and formulating a strategy based on not only the core value but also the deep understanding of the market and its trajectory.

Nonetheless, the bottom-line objectives in executing the business remain the same: to produce high quality reliable products at a competitive cost, in a competitive timeline while generating target operating margin and profits at any justified locale in the world. Specifically, attention goes to the following areas:

- Strategic alignment with core competency in niche areas
- Moving up in operating margin through niche products and services
- Time-to-market from design to end-use customers
- Manufacturing flexibility from design to production flow to supply chain agility
- Supply chain infrastructure and execution
- Inventory management and optimization
- Physical proximity to customers
- Partnership with customers
- Partnership with individually justified external services (e.g., outsource)
- Innovative capability
- Ability to foresee emerging technologies
- Tie-in with advanced manufacturing

In the context of competitiveness in the global marketplace, advanced manufacturing will gain further momentum in 2014. As one example, to slash production lead times and to advance a product's characteristics, additive manufacturing (3D printing) has opened up

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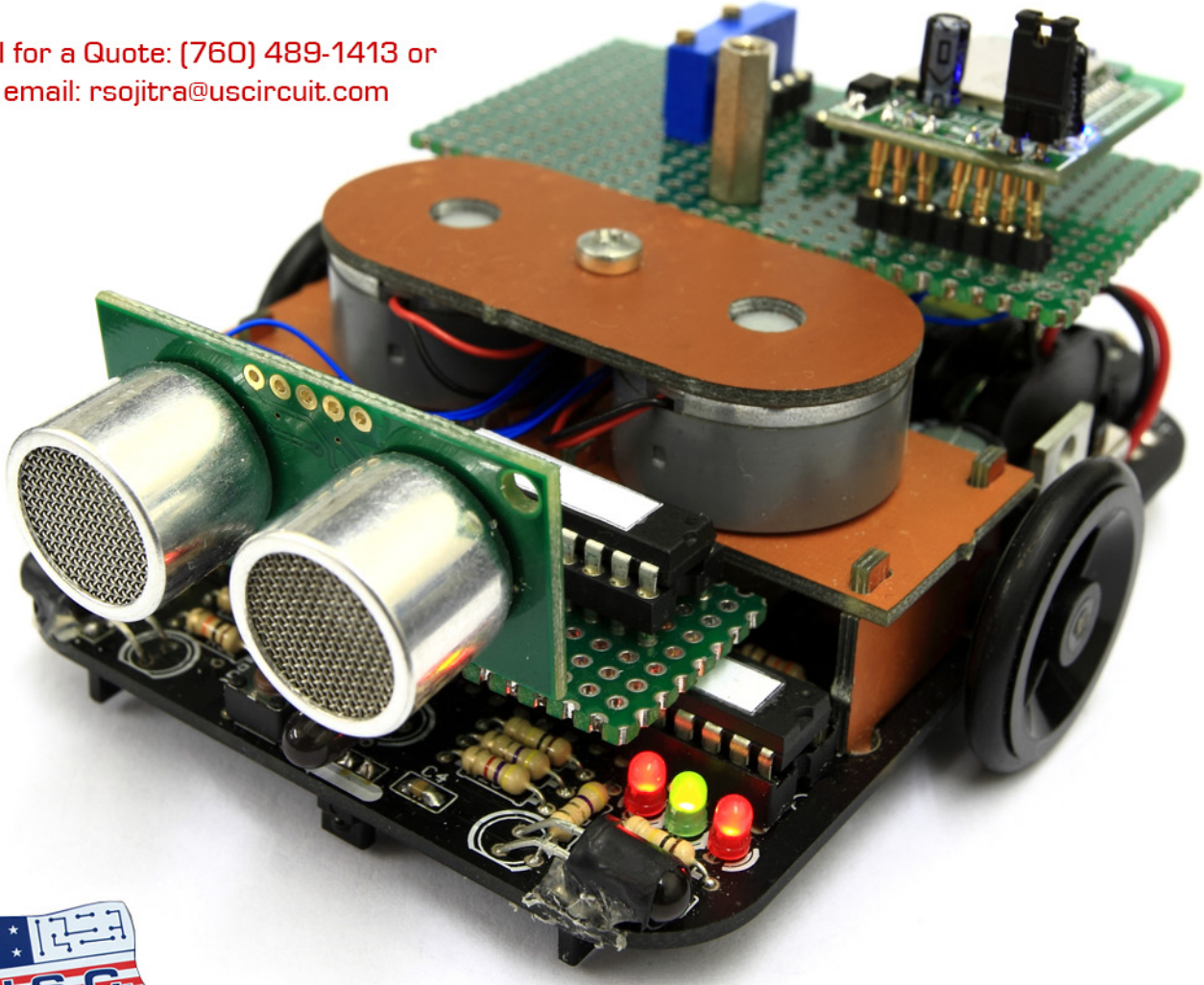

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NEW YEAR OUTLOOK: WHAT CAN WE EXPECT IN 2014? *continues*

new space. I define advanced manufacturing as "manufacturing capability and leadership capacity to sustain, grow and excel in the global landscape to meet both anticipated and unpredictable challenges by leveraging technologies and a well-positioned business model." This is a separate topic to be discussed in future columns.

I cannot emphasize enough that inventory management is imperative to the success of manufacturing operations, and its optimization is paramount to the healthy balance sheet and cash flow. Companies must keep track and control of both days of inventory as well as the actual dollar value of inventory. Doing well in this area mitigates the mishap of production outpacing demand as well as eschews cash flow trap.

When assessing the viability of out-sourcing, regardless of on-shore or off-shore, the cost is not a sole variable in the equation; rather, the cost of ownership drives the business model.

Solar Photovoltaic Market and Technology

The painstaking rebalancing, consolidation and shakeout are ending.

All signposts indicate that 2014 is looking brighter throughout the solar industry and the "healthy" companies who have served the solar sector during the boom and bust times will win big and the sustainers will be handsomely rewarded. Companies that have a solid strategy and have thus survived the last two-year "massacre" have raised their shipment guidance. Overall, 2014 will be a rebounding year, with the explanation below.

In 2014, the global end-use market will be growing or stabilizing—U.S., China and the rest of Asia-Pacific will grow and Europe will be stabilizing. Japan's lucrative feed-in tariff scheme will accelerate its solar deployment. Solar global GW installation will hit 45–55 GW level.

In the U.S., more than 9.4 GW of cumulative solar electric capacity was installed in 2013. The Federal Energy Regulatory Commission (FERC) stated that solar is one of the fastest-growing sources of new energy in the United States. To spur new solar deployment nationwide, FERC issued a new order that allows solar projects that meet certain requirements to qualify for a "fast track" interconnection process, thus eliminating the need for costly and time-consuming studies. This new development will help reduce interconnection bottlenecks.

> ***"In 2014, the global end-use market will be growing or stabilizing—U.S., China and the rest of Asia-Pacific will grow and Europe will be stabilizing."***

China's Bureau of Energy proposed to increase solar power installations from the previous target of 10 GW to 12 GW in 2014. The prevalent view is that reaching 15 GW is likely. This time around, on top of the elevated installation target to help the industry, Beijing is accelerating its build-up of solar power plants, which will undoubtedly help solar panel sector. This action is expected to rectify any residual imbalance that wrecked the industry for the last two years in an extraordinary way. Obviously, this action is good for "healthy" pure-solar-players who survived the two-year downturn, such as Canadian Solar, Trina, Yingli, and First Solar, but not the "unhealthy" companies, who are goners.

In photovoltaic cell technology, while thick film and thin film are co-existing in the marketplace, the quantum dot technology is burgeoning in the laboratory prototype, which is poised to leapfrog the existing technologies. In the marketplace, thin film has lost market share during last two years due to the market turmoil and lack of scale. Going forward, the advanced thin technology coincides well with the future growth of mobile devices.

In terms of regional market, there will be a market re-distribution geographically. The solar PV market is shifting from Europe to Asia Pacific. However, not to ignore Europe; it remains overall a vast pool of end demand for solar energy, accounting for nearly a third of global demand at 10–12 GW in 2014. Europe will be stable in 2014 and will remain a key region for business.

For suppliers in materials, components and devices in the supply chain of the solar industry, the healthy companies with a solid business model will also be rewarded substantially. In the solar space, when taking all factors into consideration, the industry remains rewarding, perhaps one of a few that have reachable, handsome growth prospects in the visible future. After going through the growing pains, the industry is expected to get stronger.

Environment-Friendly Lead-free Electronics and Regulatory-Compliant Manufacturing

The industry's technology and manufacturing are expected to move ahead with incremental improvements.

On conflict mineral disclosure requirements, 2014 will be the first filing year to comply with the Securities and Exchange Commission (SEC) rule. The rule requires supply chain due diligence and specialized reporting by companies that manufacture or are contracted to manufacture products that contain certain minerals originating from the Democratic Republic of the Congo and adjoining countries. Conflict mineral disclosure requirements include specific elements—tungsten, tantalum, tin, gold and their derivatives. Make a note that the category of derivatives is a tricky area.

In 2014, more electronics sectors including medical devices will join the world of lead-free electronics to comply with RoHS. Additionally, RoHS will be deployed to more countries.

Introduction of new or modified lead-free solder alloy materials will continue through sound scientific (metallurgical) execution in an effort to improve the performance and reliability and to alleviate production and reliability issues of tin-copper and tin-copper-silver systems. On reliability, high-quality work has been conducted and abundant data generated. One challenging effort is not to make a conclusion when a conclusion is not ready to be made. Publications that deviate from this principle are not in short supply. Going forward, it is hoped that this necessary principle would be followed so that reliability means reliability.

Overall, environmentally friendly electronics is becoming a given. Corporations' environmental stewardship for global sustainability, driven by regulations or other causes, continues to be one of important corporate business policies in 2014. **SMT**

References

1. Financial Times
2. Institute of Supply Management
3. China Daily
4. SEMI World Fab Forecast report

Upcoming Appearances

Dr. Hwang will present a lecture on "Preventing Manufacturing Defects and Product Failures" at IPC APEX EXPO 2014, on March 24 in Las Vegas.

Dr. Hwang, an international businesswoman and speaker, and business and technology advisor, is a pioneer and long-standing contributor to SMT manufacturing since its inception, as well as to lead-free electronics implementation. Among her many awards and honors, she is inducted to the WIT International Hall of Fame, elected to the National Academy of Engineering, and named an R&D-Stars-to-Watch. Having held senior executive positions with Lockheed Martin Corp., Sherwin Williams Co., SCM Corp, and IEM Corp., she is currently CEO of H-Technologies Group, providing business, technology and manufacturing solutions. She has served on the U.S. Commerce Department's Export Council, Chairman of Assessment Panel on DoD Army Research Laboratory, various national panels/committees, and the board of Fortune 500 NYSE companies and civic and university boards. She is the author of 400+ publications and several textbooks, and an international speaker and author on trade, business, education, and social issues. Her formal education includes four academic degrees as well as the Harvard Business School Executive Program and Columbia University Corporate Governance Program. For further info, go to: www.JennieHwang.com. To read past columns, click here.

Addressing Flux Corrosion and Reliability Concerns Early

by Renee Michalkiewicz
TRACE LABORATORIES

SUMMARY: The old saying "An ounce of prevention is worth a pound of cure" is very true when it comes to the assembly process and avoiding field-failure returns.

Flux corrosion is just one of the reasons an assembly might be rejected by the end customer, or worse yet, be returned from the field nonoperational. Fortunately, there are steps that can be taken to minimize the risk of corrosion, even before the first component is placed.

Understanding how flux corrosion is assessed per industry standards is an important first step in selecting the correct flux-containing products for the assembly process. Additionally, understanding the different types of flux corrosion is useful in determining the best way to minimize the flux's corrosive effects, which can be assessed using actual process chemistry on dummy circuits through testing that is termed "assembly process validation testing." And what better way to avoid field failures than to learn from others' mistakes? The following three case studies will provide steps for assembly process improvement.

There are two types of corrosion associated with fluxes, chemical and electrolytic. By definition, chemical corrosion is a process in which a solid, especially a metal, is eaten away and changed by a chemical action. Electrolytic corrosion, on the other hand, is an electrochemical process in which one metal corrodes preferentially to another when both metals are in electrical contact in the presence of an electrolyte.

Flux corrosion on electronic assemblies was assessed in the 1950s. Unfortunately, it is a failure mechanism still

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observed today. Initially, flux materials were qualified for use on military products per MIL-F-14256 [1]. These were the days of the RMA (rosin, mildly activated) and RA (rosin, activated) fluxes. The first IPC specification, IPC-SF-818 [2], came along in 1988, followed by a standard that was accepted by multiple organizations. Given the joint effort, it was renumbered IPC J-STD-004 [3] (J-STD = joint standard).

Since the 1950s, the corrosive properties of fluxes have been assessed and materials have been qualified. Low solids no-clean fluxes have been added to the mix, but these are not without processing concerns. The weak organic acids typically found in many no-clean fluxes can cause corrosion if they are not fully activated through thermal exposure. The most common issues are related to an inadequate reflow profile or excessive application of flux so that all of the potentially harmful flux residues are not completely volatilized. The remaining acid could easily attack copper barrels or traces and eventually lead to an open circuit on the assembly.

On the other hand, electromigration will often occur when you have an unactivated no-clean flux residue or a water-soluble flux residue that was not completely removed. These are somewhat tough to isolate because they often lead to intermittent short circuits, as dendrites tend to form and burn off once the current flowing through the dendrite becomes too great.

IPC J-STD-004 is a current document used to classify fluxes, and any flux containing solder—solder paste, cored wire, etc. There are four tests in 004 that assess how corrosive a flux or flux residue is: copper mirror, corrosion, surface insulation resistance (SIR) and electrochemical migration (ECM). These four tests are used to establish whether the flux will be categorized as an L (low activity), an M (moderate activity), or an H (high activity). For reference, many of the L fluxes are no-cleans, while many of the H fluxes require cleaning following the soldering process. The 004 document is intended to qualify the flux material not the soldering process.

In the copper mirror test, the flux is assessed in the as-received condition. It is not reflowed before or during the test. The flux is applied to glass slides that have been coated with 50 nm of copper. The slides are placed in a chamber at 23°C/50%RH for 24 hours. Following the exposure, a visual exam is performed to assess the amount of breakthrough. You can see by the photos that the amount of breakthrough determines whether the flux is an L, an M, or an H. The final classification for the flux is determined by the highest activity level for all tests, so the flux may give an L result for one test and an M for another—in this case it would be classified as an M.

The corrosion test is different than the copper mirror test. In this test, the flux is tested af-

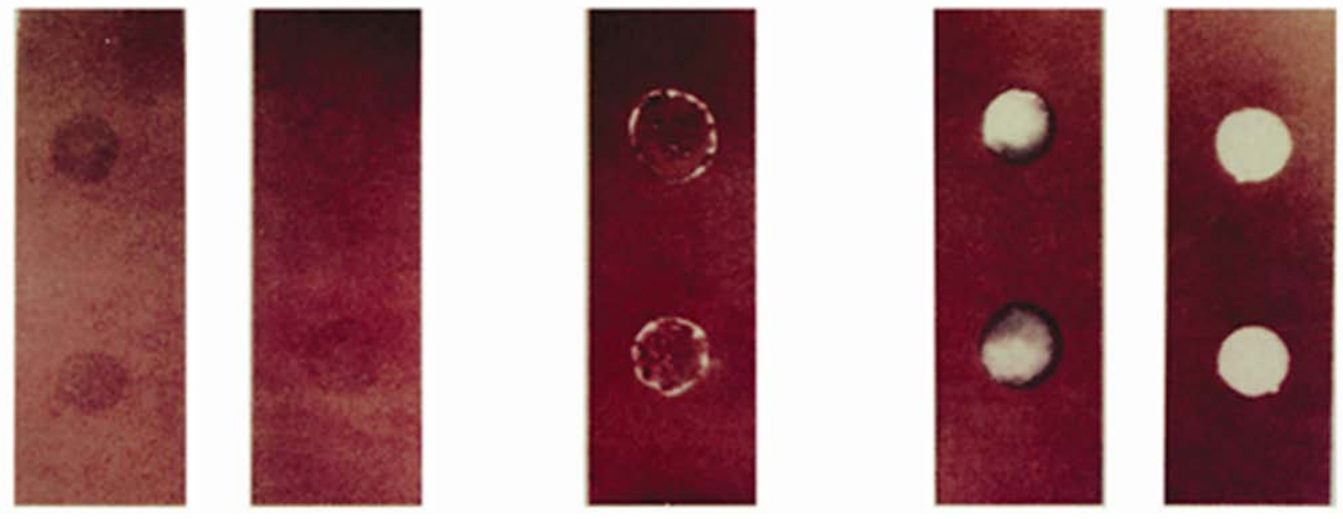

Figure 1: Copper mirror test. L = no breakthrough, M = less than 50% breakthrough, H = greater than 50% breakthrough.

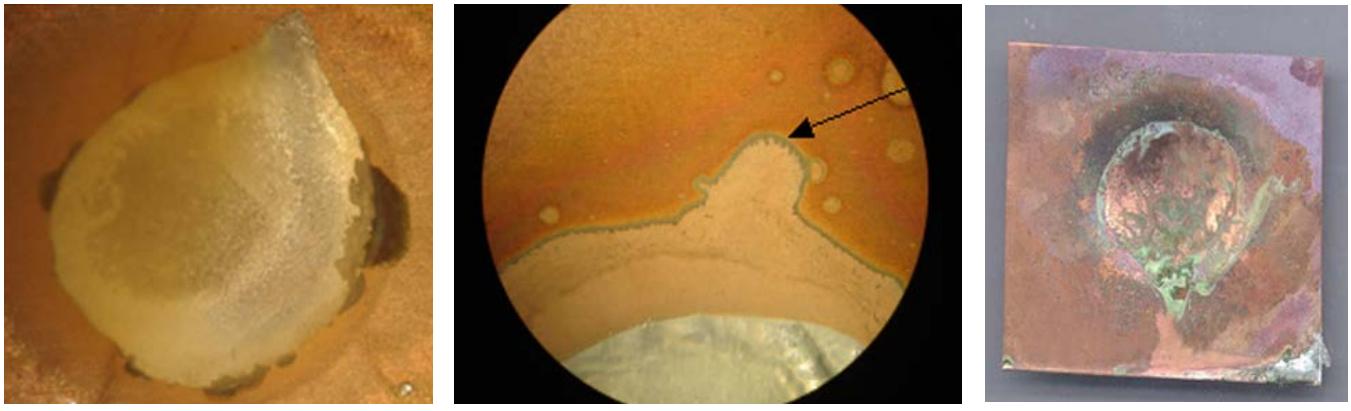

Figure 2: Corrosion test showing (l–r) no corrosion, minor corrosion and major corrosion.

ter reflow. A small amount of flux and solder is run through the appropriate reflow profile on a copper panel. The copper panel is then conditioned for ten days at 50°C/95%RH. Following exposure, the panels are removed and visually examined. The "no corrosion" on the left would indicate an L rating. The "minor corrosion" in the center would yield an M rating and the "major corrosion," where a green/blue copper salt has formed, would be an H; here, the copper is being corroded by the flux.

The next two tests assess the flux's propensity to develop leakage current across two isolated traces. This leakage current is often caused by the formation of dendrites or electrochemical migration. Again, these J-STD-004 SIR and ECM tests were developed to test the flux itself, not an assembly process. For the SIR test, the flux is reflowed on the test board. The samples are biased and exposed to 40°C/90% RH for seven days. During that time, insulation resistance (IR) measurements are taken every 20 minutes. The reason for the frequent monitoring of the IR is that dendrites tend to form and then burn off because they cannot carry the current that builds up across this fragile "circuit," as shown in this real time video.

The 20-minute measurement interval is intended to catch the drop in IR when there is a bridge between the conductors. Fluxes that fail to meet the 1 x 10E + 08 ohm requirement must be cleaned. Additionally, following the test, a visual exam is performed. Evidence of corrosion of the conductors is also considered to "not meet" the specification and the flux would have to be cleaned. There is a lot of product develop-

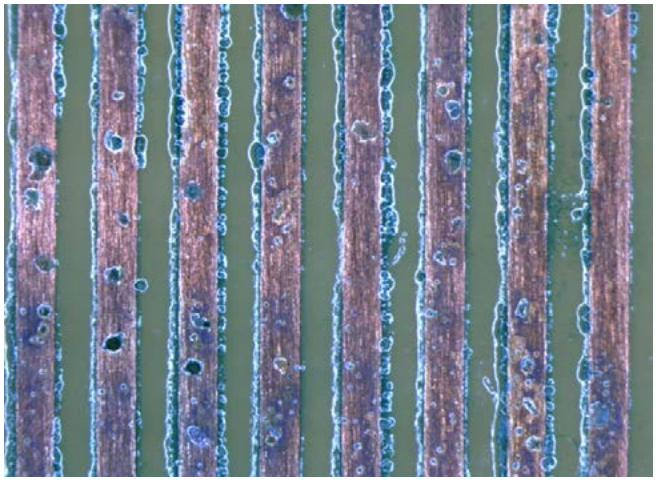

Figure 3: Flux corrosion of copper conductors.

Figure 4: Dendritic growth.

ment that flux manufacturers must perform to develop a product that will effectively clean the metals to be soldered, make a good quality solder joints and leave no corrosive residues.

The electrochemical migration test was copied from the Telcordia GR-78-CORE [4] specification. For manufacturers who are required to have their materials qualified to J-STD-004, as well, the GR-78 wanted one qualification procedure to cover both J-STD-004 and the Telcordia document. This method has not been modified to include frequent monitoring of the IR because the Telcordia document does not include this. Again, for this test, the flux is tested in the reflowed state. The boards are run at 65°/85% RH for 21 days and the IR measurement at 96 hours is compared to the 500-hour measurement. A greater than 1 decade drop in IR would constitute a failure.

Again, dendrites and corrosion are reasons for failure.

There is one additional test, the Bono test, which has been run for a number of years but is not currently part of the J-STD-004 specification. The Bono test is based on a test developed by Dr. David Bono and recently modified by Dr. Laura Turbini [5]. For the most recent study, weak organic acid (WOA) solutions including abietic, succinic, glutaric, adipic and malic acids were used to assess the best environment for assessing flux corrosion. This experiment did not use full flux chemistry, just the acid itself. The study found a 60°C/93% RH environment for 10 days was most effective in detecting differences in the WOA's corrosivity. The J-STD-004 committee is currently considering the research being done on this method for possible inclusion in the specification. This test is a similar temperature/humidity/bias (T/H/B) test, but the amount of corrosion and the IR are measured quantitatively. The test is showing promise for being more sensitive in assessing flux corrosion.

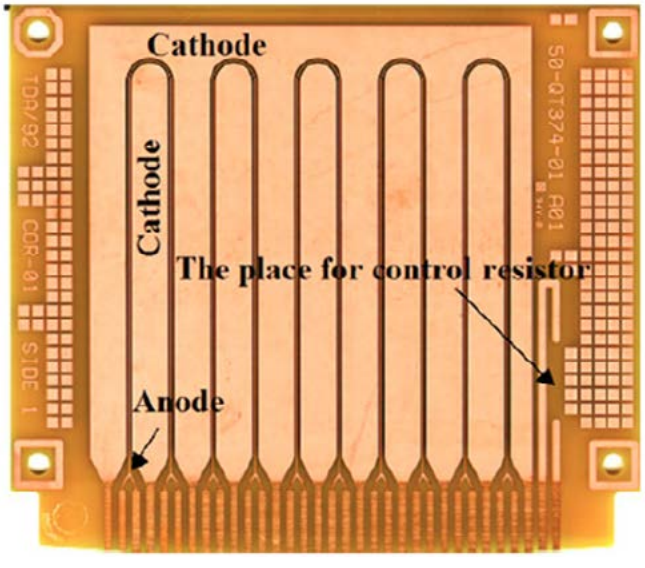

Figure 5: Modified Bono test pattern.

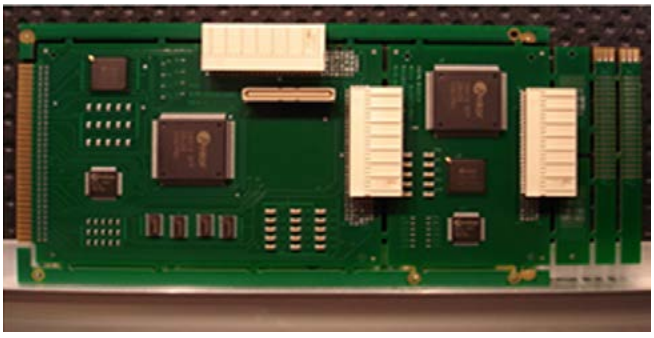

Figure 6: IPC-B-52 assembly.

Once the fluxes have been selected, it is important to confirm that all of the assembly process chemistries work well together and that there will not be any unexpected reactions. IPC-9202 [6] and IPC-9203 [7] are resource documents for this assessment. Often, a perfectly benign flux, when placed in the company of other chemistries, can cause some unexpected reactions. The IPC-B-52 board pictured below is a good tool to assess process chemistries. Test boards and dummy components may be purchased commercially or the boards may be built by the actual board supplier to assess this step, as well. It is important to use dummy components as active circuits would not allow for IR to be measured beneath the components. This board is a good tool to assess a change in assembly line chemistry. The old and the new chemistry may be run side-by-side to compare leakage current development and corrosion characteristics.

Case Studies

Case #1: An automotive audio supplier began experiencing intermittent failures in their radios. Intermittent failures can be difficult to

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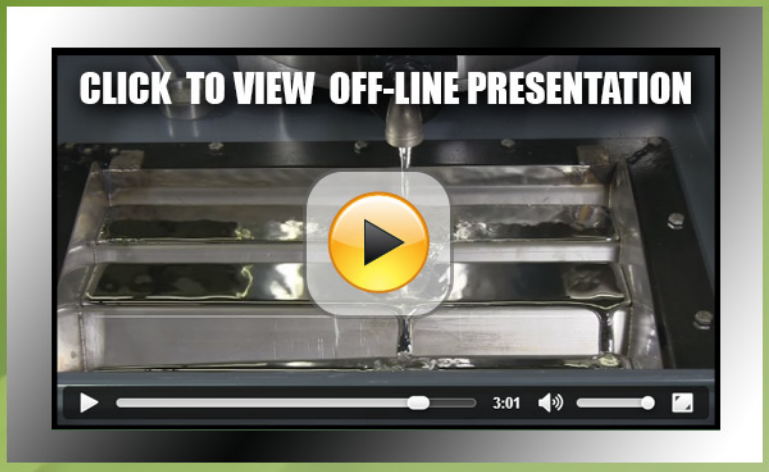

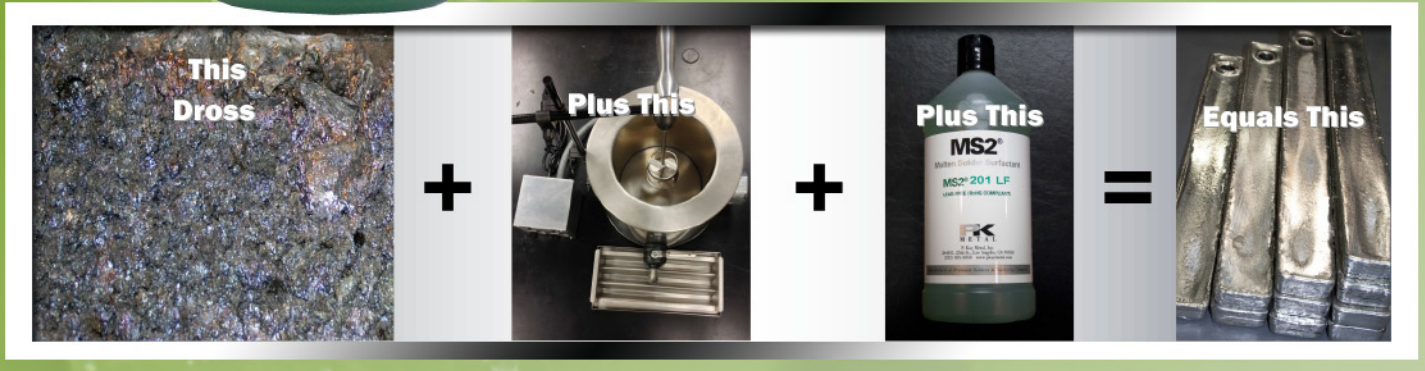

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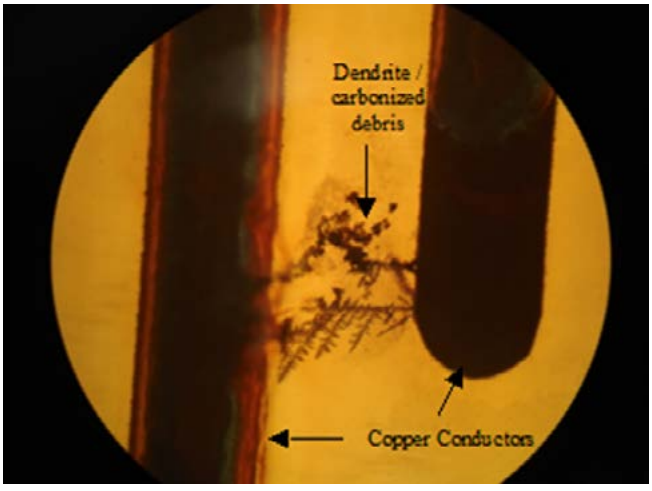

Figure 7: Carbonized debris.

detect, but evidence of carbonized debris was observed (Figure 7). This debris is what remains when the dendrite sees too much current and then disintegrates.

When assessing what went wrong in the assembly process, data sheets and qualification data were reviewed for all chemicals involved. The flux supplier was asked for recent evidence of lot conformance testing and qualification data. It was discovered that the material had not undergone a full qualification in 15 years. Running an ion chromatography test on the flux confirmed that the activity level of the flux had changed, most likely due to a change in one of the raw materials.

For users of fluxes, it is important to select fluxes that are qualified per J-STD-004 or another industry standard. After selecting the soldering materials for the assembly process, it is important to ask to see the dated qualification and conformance reports. Do not rely on technical datasheets as this information can be years old. Per 004, flux manufacturers must be able to provide this data to their customers. This is most often an issue (product not tested for a very long time and out of control) in product failure analysis when the contract manufacturer (CM) or original equipment manufacturer (OEM) is using a flux supplier who does to participate in IPC or other technical conferences.

IPC has recognized this as a common issue and has begun a program called Product Validation Services. Randy Cherry, the director of this program, is trying to help eliminate these issues by performing supplier audits and by testing products to show conformance to IPC documents. The first group of products to be qualified was fluxes. This will hopefully lead to a qualified products list (QPL) similar to that used by the military industry that will be readily available to the industry for selection of approved products.

Case #2: The second case study involves a security company that began receiving field failure returns of their camera system. The issue was isolated to a particular BGA. You can see excessive flux residue around the suspect component.

The test engineer X-rayed the BGA to look for potential failure causes and was able to capture images of the dendritic growth projecting from the solder balls. Additionally, once the BGA was removed, there was clear evidence of excessive flux residue and dendritic growth bridging electrically isolated conductors.

These photos show the dendrites beneath the excessive flux residue with the component removed. Fourier transform infrared (FTIR) spectroscopy was run on the flux residue for comparison to reflowed flux residues of all fluxes used in the assembly process. There was a close match to a particular tacky rework flux. When reviewing the flux datasheet the following state-

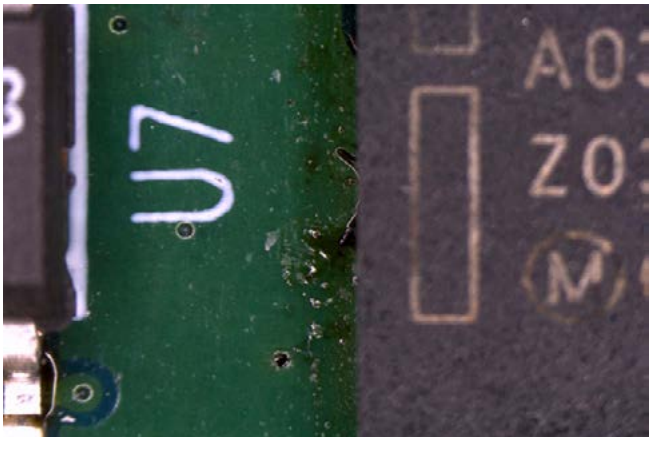

Figure 8: Excessive flux residue observed surrounding BGA.

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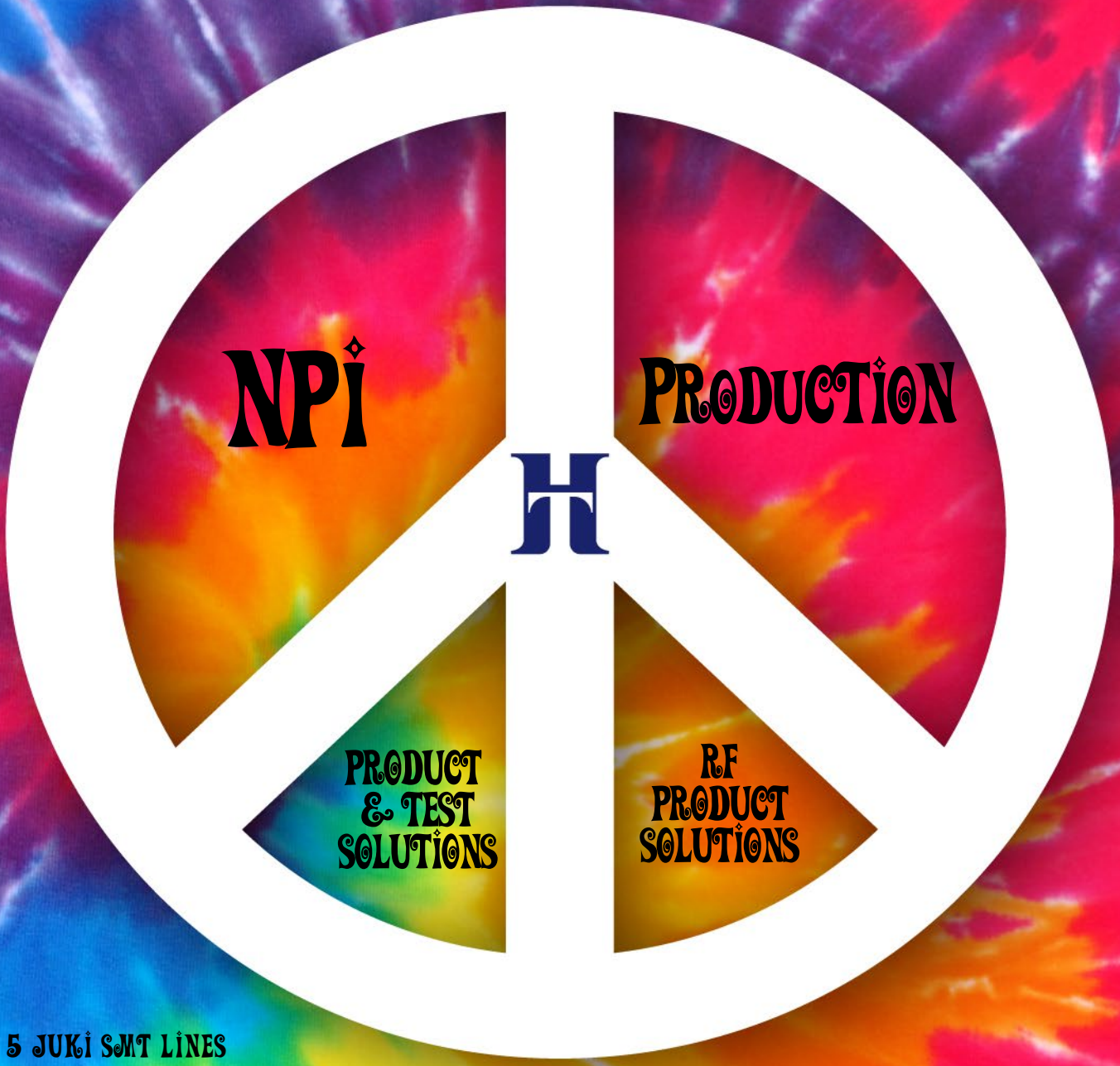

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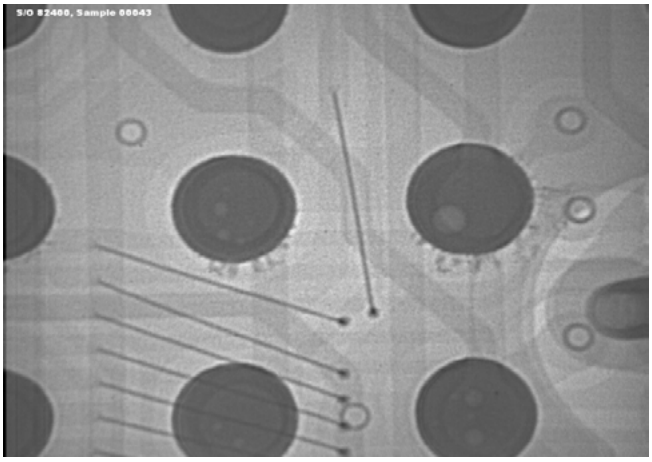

Figure 9: X-ray image showing dendritic growth beneath BGA.

ment was found: "Meets IPC ANSI-J-STD-006 requirements for ORL0, Water Soluble." There is a problem with this statement. J-STD-006 is the standard for the solder metal, not the flux activity level. This should be a red flag that the manufacturer may not have a complete understanding of the IPC classification system. When ion chromatography was run on the flux, it was found to be an L1 level containing halides.

Again, these are very straightforward examples of what pitfalls need to be avoided when developing the assembly process steps. Any hand soldering step—in this case rework—must be tightly controlled to make sure all flux is fully activated. Request and review actual flux data

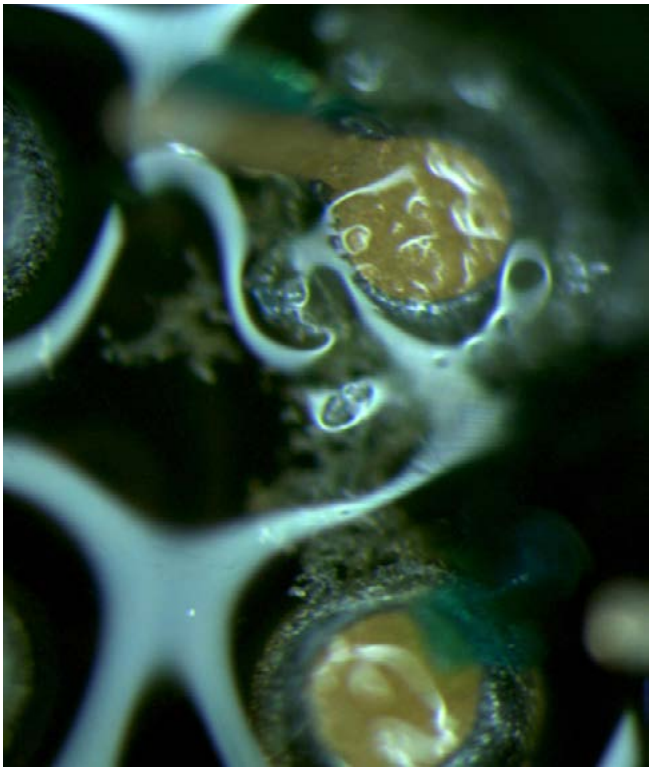

Figure 10: Excessive flux residue and dendritic growth visible once BGA component was removed.

and be on the lookout for red flags. Consider performing process validation studies before the product is in a field failure return situation. Weigh your risks and potential damage to your reputation if product is recalled.

Summary of Recommendations

Use reputable flux suppliers	Rework flux must see full heat to be fully activated
Periodically request the most recent qualification and lot screening test results	Look for "red flags" on product datasheets that could suggest the flux supplier does not have understanding of product specifications
Be sure to have controls on all stages of the soldering process	Do not tent via on one side of board
Verify assembly process through process validation studies	Make sure vias are completely tented; no soldermask voids
Control process steps that are not part of the normal process (i.e., rework)	

Table 1.

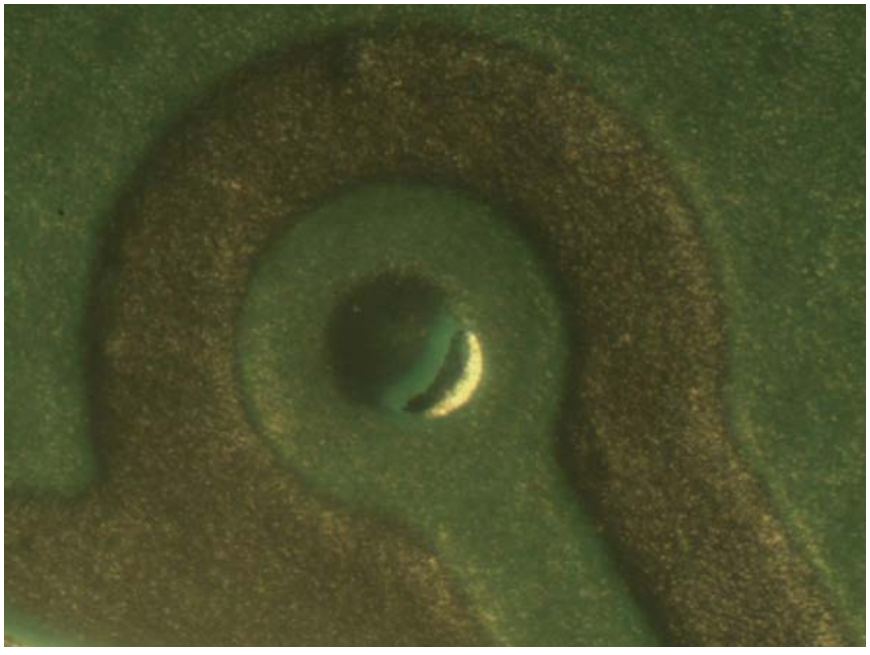

Photo 11: Soldermask void in tented via.

Photo 12: Blind via with missing copper plating.

Case #3: Entrapped assembly chemicals are an issue that can arise within small vias or within vias that are tented on one side of the board. Soldermask voiding and misregistration can also allow assembly chemicals to enter a via and become trapped. A board going through an additional reflow step can give the chemicals time to dissolve the copper in the hole which can lead to an open circuit. Manufacturers appear to be more aware of this failure mode, so it is not found as often as it was few years ago.

Table 1 contains a summary of steps that may be taken to improve assembly reliability as it relates to controlling flux corrosion. **SMT**

References

1. MIL-F-14256, Flux, Soldering, Liquid, Paste Flux, Solder Paste and Solder-Paste Flux, (For Electronic/Electrical Use) General Specification for (1956).

2. IPC-SF-818, General Requirement for Electronic Soldering Fluxes (1991).

3. IPC J-STD-004B, Requirements for Soldering Fluxes (2008).

4. Telcordia GR78-CORE, Generic Requirements for the Physical Design and Manufacture of Telecommunications Products and Equipment (2007).

5. Zhou, et al. Characterizing Corrosion Effects of Weak Organic Acids Using a Modified Bono Test (2013).

6. IPC-9202, Material and Process Characterization / Qualification (2011).

7. IPC-9203, Users Guide to IPC-9202 and the IPC-B-52 Standard Test Vehicle (2012).

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Grain Refinement for Improved Lead-Free Solder Joint Reliability

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Previously published in the 2013 IPC APEX EXPO Conference Proceedings

Abstract

The very small solder joints that now account for an increasing proportion of the connections on which modern electronics depend, are typically made up of only a few grains, sometimes only a single grain. This combined with the high degree of anisotropy in the mechanical properties of the body-centred tetragonal beta-tin crystal is a significant factor in determining the response of the joint to the strain to which it is subject in service, with consequent implications for reliability. The superior reliability in joints with multiple small grains of random orientation suggests that it would be advantageous if the solder alloy could be made to solidify with that fine grain structure. In the study reported in this paper, the effect of trace additions of selected elements on the grain structure of pure tin and lead-free solder alloys was observed. The elemental additions were chosen on the basis of previous research as well as an analysis of relevant binary phase diagrams.

Solidification theory suggests that an objective of the addition should be to promote the rapid development of a constitutionally undercooled zone ahead of the advancing solid/liquid interface since this is known to favour the repeated nucleation required to achieve a fine grain structure. The results contribute to the growing body of knowledge on the development of microstructure in lead-free solder alloys.

Introduction

Most of the significant differences between the commonly used lead-free solders, those based on additions of copper and/or silver to tin, and the eutectic tin-lead solder that they are replacing can be related to the microstructure. The microstructure of the tin-lead eutectic is made up of interleaved layers of a lead-rich tin metallic phase and a tin-rich lead metallic phase while that of the lead-free solders

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is essentially a pure tin matrix in which are dispersed particles of one or both of the intermetallics Cu_6Sn_5 and Ag_3Sn.

While the equilibrium phase diagrams for the lead-free solders with 3–4% silver and 0.5–1% copper predict a microstructure dominated by eutectics with a fine dispersion of the intermetallics, the conditions during solidification in production soldering processes are usually very far from thermodynamic equilibrium. The situation is further complicated by interactions with substrates with much of the Cu_6Sn_5 ending up at the interface. The consequence is that the microstructure is predominantly tin with a dispersion of intermetallics that often have a morphology more typical of a primary phase than that formed by the coupled growth of a eutectic.

A further factor with implications for joint reliability is that there are typically very few individual tin grains in a solder joint. In the very small joints to the area array packages that account for an increasing proportion of the connections in modern electronic assemblies there are typically only two or three grains and sometimes only one. The reliability consequences of having so few grains are particularly severe in tin because of the extreme anisotropy of its physical properties. Given that anisotropy the time to failure for a particular joint under the conditions to which it is exposed when it is subjected to thermal cycling can be very dependent on the orientation of those few grains[1].

While grain boundaries can themselves contribute to failure the reduction in the anisotropy of a solder joint by increasing the number of randomly oriented grains would be an advantage and the observation has been made that joints with a finer effective grain size last longer in thermal cycling than otherwise expected[2].

Given the continuing need to increase the reliability of solder joints an avenue that warrants exploration is reducing the grain size of the tin matrix.

Factors that Affect Grain Size

It has been found to be difficult to reduce the grain size of as-solidified tin because tin has been found to be particularly difficult to nucleate[3]. For a grain to form from the molten alloy the first requirement is a solid particle to which tin atoms from the liquid can attach in the ordered arrangement of the body-centred tetragonal crystal of the beta allotrope that is the stable form of tin at temperatures above 13.2°C. The grain size of the solder joint is inversely related to the number of nuclei activated in each joint during solidification. In pursuing this possible avenue of solder joint reliability improvement, therefore, the challenge is increasing the number of active nuclei in each joint.

Two methods of increasing the number of active nuclei are to:

- Introduce foreign particles that can act as nuclei for tin (heterogenous nucleation)
- Create conditions during solidification that favour homogeneous nucleation

Attempts at tin grain refinement with heterogenous nuclei have not been successful in significantly increasing the number of grains in s solder joint[3] and in the study reported in this paper the focus has been on the promotion of homogeneous nucleation. Homogeneous nucleation occurs when atoms from the liquid organise into a particle of the crystal lattice large enough to provide a stable base to which other atoms can attach. Measures that promote homogeneous nucleation also have the effect of increasing the likelihood that any heterogenous nuclei that are present will be activated.

Because of the need to create a new high energy solid/liquid interface homogenous nucleation requires the driving force of a large free energy reduction so that it does not occur at the equilibrium melting point. Cooling has to continue to temperatures below the melting point before there is sufficient free energy available to initiate nucleation. This is the phenomenon known as undercooling. As molten tin cools the plot of temperature versus time (Figure 1) initially follows Newton's Law of Cooling. Because of the difficulty of nucleation the cooling continues past the theoretical melting point until a temperature is reached at which there is sufficient driving force (Gibbs free energy) to create the high energy solid/liquid interface required for a stable nuclei to

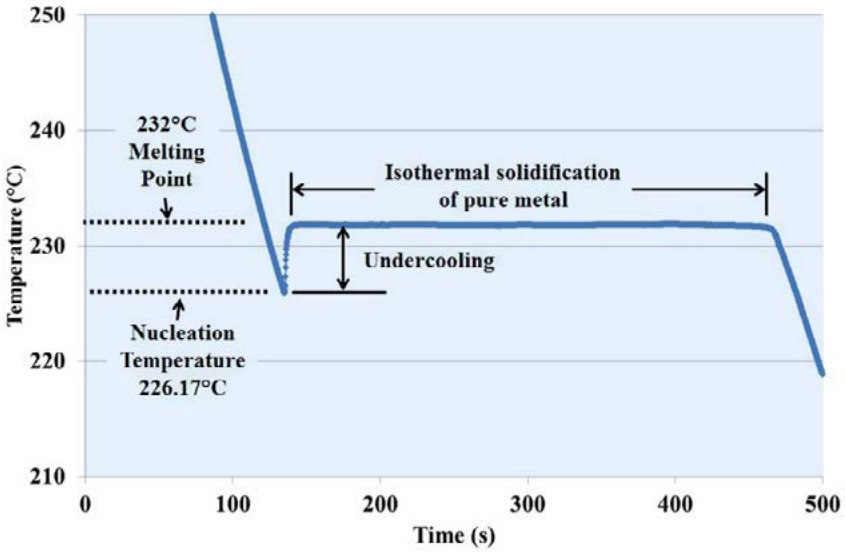

Figure 1: Cooling curve for pure tin showing the undercooling required to trigger nucleation of solid.

form. In Figure 1 the undercooling is only six degrees but undercooling as large as 187°C has been measured in extremely high purity tin[4].

Once solid tin has been nucleated and growth begins the latent heat released by the solidifying tin results in the temperature climbing to the equilibrium freezing temperature (the melting point) and in a pure metal or eutectic solidification proceeds at that temperature until all liquid has solidified, after which Newton cooling continues.

It has been demonstrated that tin dendrites grow very quickly once solidification has commenced[1] so that particularly in a small joint there is little time for further nuclei to activate. For this reason nucleation of more grains should be favoured by slowing down solidification.

The rate of solidification can be reduced by lowering the melting point of the liquid at the interface. The liquid then has to cool further before solidification can proceed. The resulting delay provides additional time and the extra cooling additional driving force for the activation of other nuclei. Such a reduction in the melting point of the liquid at the interface can be achieved by adding to the tin an element that lowers the melting point of tin and that has relatively low solubility in solid tin. As the solid tin interface advances the concentration of the rejected additive in the liquid adjoining the interface is increased and its freezing temperature reduced. This is the effect known as constitutional undercooling.

The greater the reduction in the melting point per unit of additive the more effective the additive should be in promoting constitutional undercooling. And the lower the solubility of the addition in solid tin the faster its concentration will build up. These two factors therefore provide a basis for selecting candidate grain refining additives.

The effect can be quantified by the use of what is known as the growth restriction factor (GRF), which is a measure of the extent to which the advance of the solid interface into the adjoining liquid under the influence of a temperature gradient is limited by the increase in solute concentration in the area adjacent to the interface. This in turn is determined by the rate at which the solute atoms diffuse through the region of liquid ahead of the interface, Q, which is defined[5] as

$$Q = mc_o(k-1)$$

where m is the gradient of the liquidus at the composition of the alloy and k is the partition coefficient defined as

$$k = c_s - c_o$$

where c_o is the concentration of the additive in the liquid and cs is the concentration of the additive in the solid that forms from that liquid. These features are indicated on the schematic eutectic phase diagram in Figure 2.

It has been proposed that when the constitutional undercooling is small this equation could be used to predict the grain size. When the constitutional undercooling is large a plot of grain size again Q makes it possible to determine whether the additive is functioning as a nucleant of a promoter of constitutional

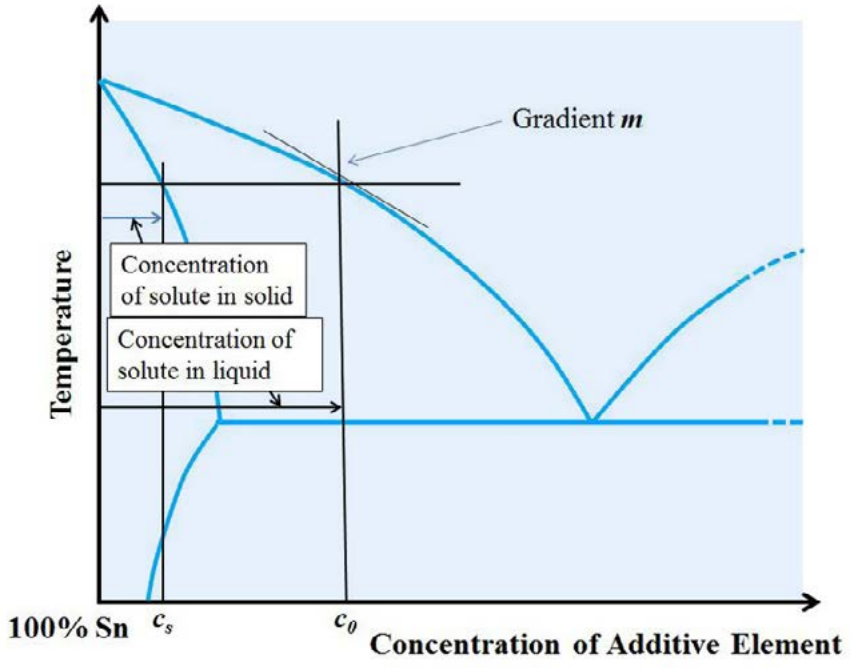

Figure 2: Parameters used in the calculation of the growth restriction factor in non-equilibrium solidification.

undercooling. For elements that function as a promoter of constitutional undercooling there should be a linear increase in grain size with 1/Q. If the additive is acting simple as a heterogenous nucleant the grain size will simply decrease with increasing concentration up to the saturation limit[7].

Selection of Grain Refiners

The elements listed in Table 1 were selected for evaluation as grain refiners on the basis that they met the criteria for promoting significant constitutional undercooling in tin. The values for the liquidus slope, m, and partition coefficient k, were estimated from published phase diagrams. Except for Ag and Cu, the decision to select these elements was reinforced by reports in the literature of grain refining effects in tin and high tin alloys. Ag and Cu were included not only because of their significant growth restrictions factors but because they are the most common alloying additions in lead-free solder.

Experimental Procedure

Alloying

The elemental additions were made to 99.9% tin via master alloys prepared by heating mixtures of the elements to temperatures up to 800°C for 2 hours.

Thermal Analysis

1kg for the alloy was melted in graphite crucibles coated with boron nitride, which is inert to these alloys and not expected to play any role in nucleation. The crucible was stabilized at 332°C (100°C above the melting point of tin) for two hours, the dross removed from the surface and the alloy stirred thoroughly to ensure uniformity. A 30 ml sample was poured

Element	Liquidus Slope m	Partition Coefficient k	Growth Restriction Factor		
			0.3 Wt%	0.5% Wt%	1.0 Wt%
Al	-6.6	0	1.98	3.3	-
Ag	-3.20	0	-	-	- 3.2
Bi	-1.63	0.63	0.18	0.30	-
Co	-2.96	0	0.88	1.48	-
Cu	-7.14	0	2.14	3.57	-
Mg	-13.36	0	4.00	6.68	-
Zn	-3.8	0	1.14	1.90	-

Table 1: Elements selected as potential grain refiners.

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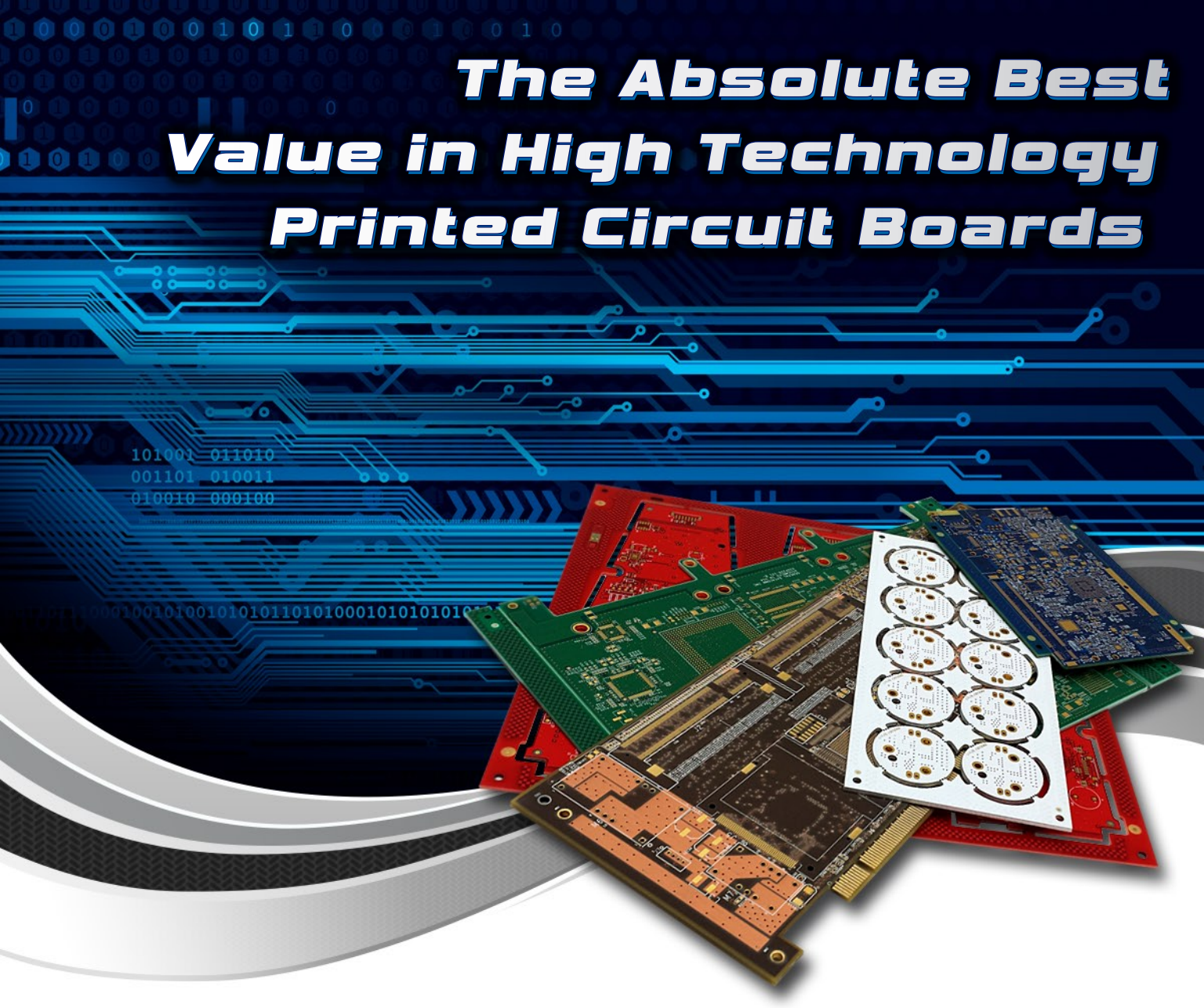

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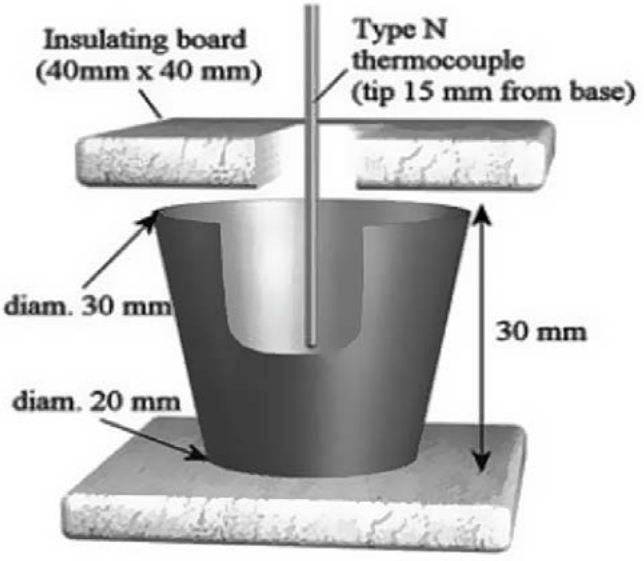

Figure 3. Thermal analysis set-up.

into a non- wetting stainless steel cup and a thermocouple inserted. The crucible was located between insulating boards as in the set up illustrated schematically in Figure 3. In this arrangement heat is lost mainly in the radial direction.

Data was sampled from the thermocouple every 0.2 seconds and written into an ASCII file via a DOS program. The derivative calculated to permit more accurate determination of the liquidus and solidus temperatures. These files were then transferred to Excel worksheets for analysis and plotting.

Grain Size Measurement

The alloys were cast into ingots (Figure 4) for macro examination and cross-sectioning.

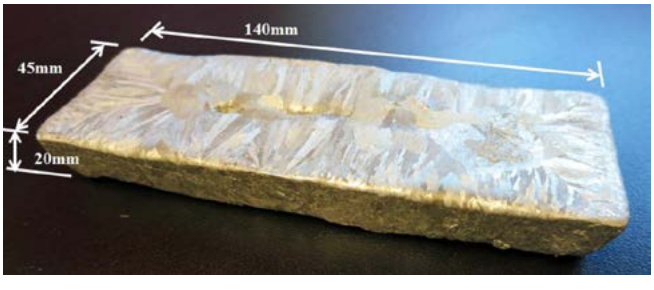

Figure 4: Ingots cast for grain size determination.

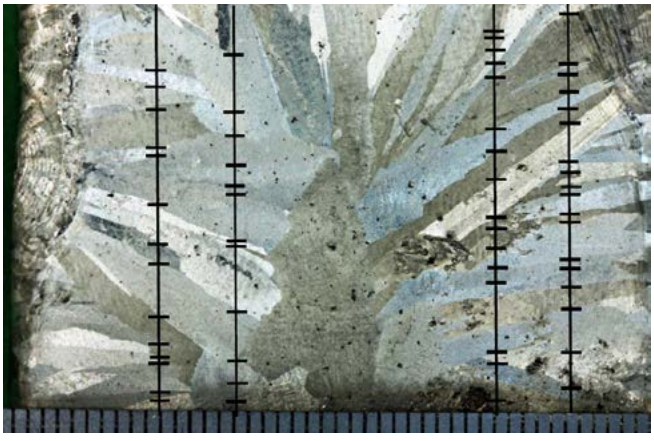

Figure 5: Intercept counting method used to characterize the size of as-cast grains.

It was found that mechanical damage caused by cross-sectioning triggered recrystallization, something that is not unexpected in tin, which is very soft and so vulnerable to deformation and at normal room temperatures is at a relatively high homologous temperature—about $0.6T_m$ which is equivalent to, for example, copper at about 530°C.

The opportunity was thus taken of extending the study to include the effect of the selected alloying additions on the recrystallized grain structure as well as the as-cast grain structure. Because of this recrystallization, with the techniques available the as-cast grain size could be determined only by examination of the exterior surface.

Measurement of As-Cast Grain Size

To reveal the grain structure the as-cast approximately 1kg ingots were etched in a bath of 2% HCl + 5% HNO_3 in ethanol. Macrographs of the etched surface were taken with a 16 Mp SLR camera. Because of the cooling direction in the ingot mould the grain structure was predominantly columnar and the dimension measured was the width (Figure 5). Sufficient measurements were taken to get a statistically significant result.

Measurement of Recrystallized Grain Size

Thermal analysis samples were cut in half and mounted in epoxy resin, ground on silicon carbide paper and polished with 0.5µm diamond with a final finish with SiC. If neces-

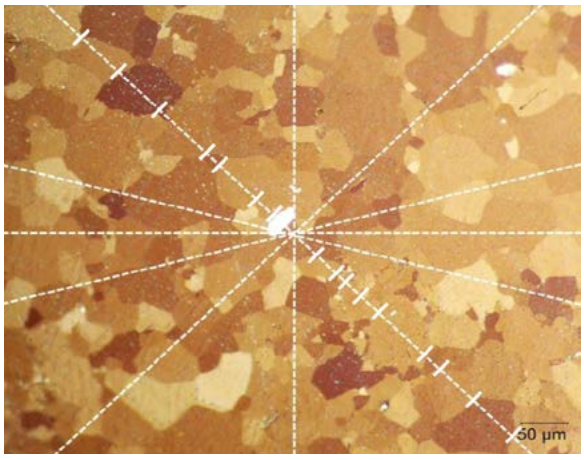

Figure 6: Intercepts along which the recrystallized tin grain were counted in cross sections.

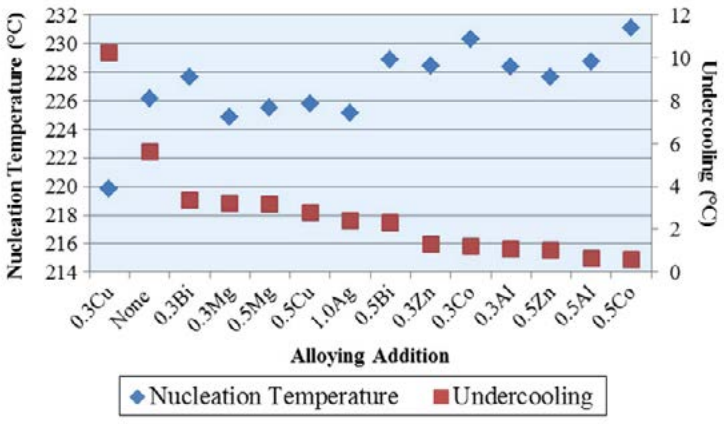

Figure 7: The effect of composition on nucleation temperature and undercooling with the results presented in order of decreasing undercooling.

sary to reveal the grain structure samples were etched in with 5% HNO_3 in ethanol.

The grain size was measured using the linear intercept method. Because of the directional character of the grain structure in some alloys intercepts were measured along lines at right angles and at 45° as well as lines ±15° from the transverse (Figure 6). From the number of grains intercepted the grain size number was calculated. The grain size number was averaged over the samples measure and converted to a grain size in microns with a standard deviation being calculated.

Results

Thermal Analysis

The results of thermal analysis are summarized in Table 2.

The results in Table 2 sorted by undercooling are presented in Figure 7 in which the relationship between undercooling and nucleation temperature is apparent.

Sample Composition	Nucleation Temperature [°C]	Undercooling [°C]	Observations
99.9Sn	226.17	5.63	-
Sn-1.0Ag	225.16	2.42	Low temperature eutectic phase present
Sn-0.3Al	228.40	1.05	-
Sn-0.5Al	228.72	0.64	-
Sn-0.3Bi	227.65	3.35	-
Sn-0.5Bi	228.87	2.33	-
Sn-0.3Co	230.30	1.22	-
Sn-0.5Co	231.12	0.61	-
Sn-0.3Cu	219.86	10.25	Large undercooling possible experimental error
Sn-0.5Cu	225.80	2.78	Clearly defined primary and eutectic phases
Sn-0.3Mg	224.85	3.22	Evidence of a low melting point phase
Sn-0.5Mg	225.52	3.16	Evidence of low melting point phase
Sn-0.3Zn	228.47	1.29	Evidence of two low temperature phases
Sn-0.5Zn	227.63	1.04	Two low temperature phases clearly defined

Table 2: Data from thermal analysis.

Composition	Average Grain Size [mm]
99.9Sn	1.53 ± 0.39
Sn-1.0Ag	1.89 ± 0.46
Sn-0.3Al	0.45 ± 0.17
Sn-0.5Al	0.54 ± 0.20
Sn-0.3Bi	2.01 ± 0.59
Sn-0.5Bi	1.56 ± 0.37
Sn-0.3Co	2.55 ± 0.60
Sn-0.5Co	Larger than 0.3Co
Sn-0.3Cu	2.04 ± 0.46
Sn-0.5Cu	4.09 ± 1.39
Sn-0.3Mg	1.15 ± 0.38
Sn-0.5Mg	1.04 ± 0.21
Sn-0.3Zn	1.26 ± 0.34
Sn-0.5Zn	1.19 ± 0.33

Table 3: As-cast grain size.

Composition	Grain Size Number	Average Grain Size [µm]
99.9Sn	7.11	29.98 ± 13.95
Sn-1.0Ag	8.84	16.41 ± 3.57
Sn-0.3Al	10.47	8.42 ± 0.79
Sn-0.5Al	10.89	7.22 ± 0.65
Sn-0.3Bi	9.39	13.79 ± 2.81
Sn-0.5Bi	9.32	14.11 ± 2.92
Sn-0.3Co	5.67	48.01 ± 10.15
Sn-0.5Co	5.63	48.53 ± 10.33
Sn-0.3Cu	7.80	23.46 ± 5.48
Sn-0.5Cu	8.07	21.61 ± 4.85
Sn-0.3Mg	8.16	20.79 ± 4.95
Sn-0.5Mg	8.38	19.05 ± 4.39
Sn-0.3Zn	7.46	25.94 ± 5.54
Sn-0.5Zn	8.24	19.37 ± 3.80

Table 4: Recrystallized grain size.

As-Cast Grain Size

The results of the measurements of the as-cast tin grain size are summarized in Table 3.

In Figure 8, the data in Table 3 has been ranked in order of decreasing grain size for the alloys with the 0.3 Wt% additions with the results for pure tin and the 1% Ag addition interpolated. It is interesting to note that the two most common alloying constituents of lead-free solder, copper and silver, both appear to have the effect of increasing grain size. Bismuth and cobalt, which are also included in some lead-free solder formulations also appear to increase the as cast grain size. Even allowing for the error bars it is clear that aluminium has a strong effect, reducing the grain size as measured by more than a factor of three.

Recrystallized Grain Size

The results of measurement of the recrystallized grain size are summarized in Table 4. At an average of about 30µm, the recrystallized grains of tin are only one-fiftieth of the measured size of the as cast grains which averaged 1.5 mm.

In Figure 9, the data in Table 4 has been ranked in order of decreasing grain size for the alloys with the 0.3 Wt% additions with the results for pure tin and silver interpolated. While the largest and smallest grain sizes occur in the alloys with cobalt and aluminium respectively as was the case with as-cast grain size the ranking between those two is quite different.

Discussion

The results presented in Figure 8 indicate that zinc, magnesium and aluminium reduce the grain size of that as-cast alloy with aluminium having the greatest effect. When the results are analysed in terms of the growth restriction factor there is evidence of a trend that suggests that aluminium is having a strong growth restriction effect (Figure 10). Copper and cobalt appear to be promoting grain coarsening rather than refinement.

While copper seems to promote a coarse grain size even after recrystallization the other additions all have some effect in reducing the recrystallized grain size. However, aluminium appears to have the strongest effect in promoting a fine recrystallized grain size.

As a matter of interest the ratio of the as-cast to recrystallized grains sizes was calculated and

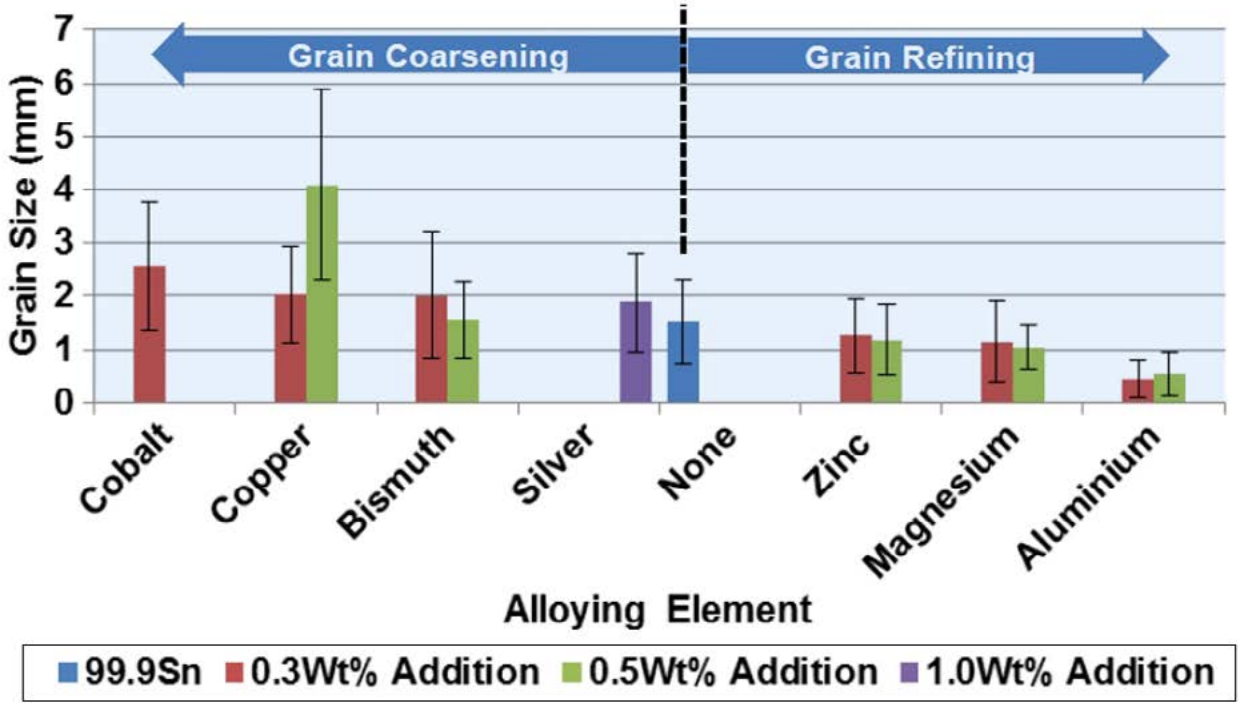

Figure 8: Effect of alloying addition on as-cast tin grain size.

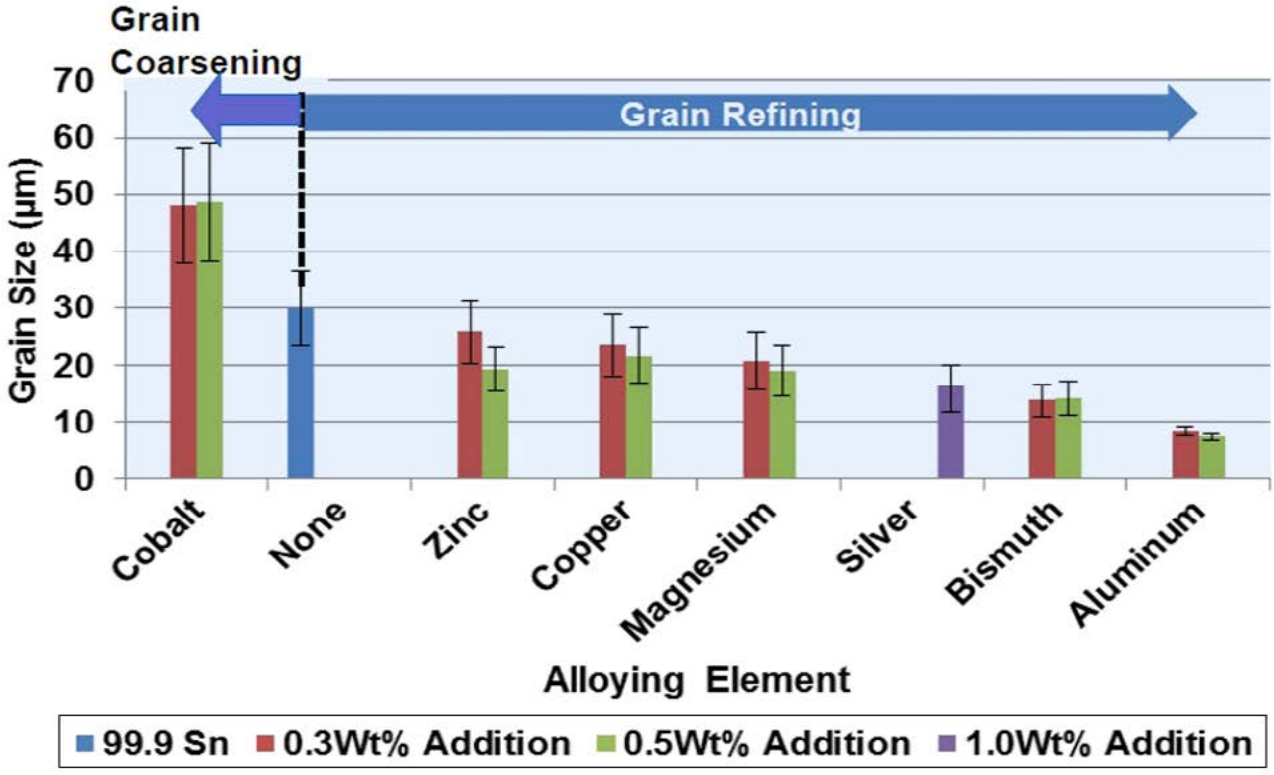

Figure 9: Effect of alloying addition on the recrystallized tin grain size. Results ranked by grain size with 0.3 Wt% addition with results for pure tin and silver interpolated.

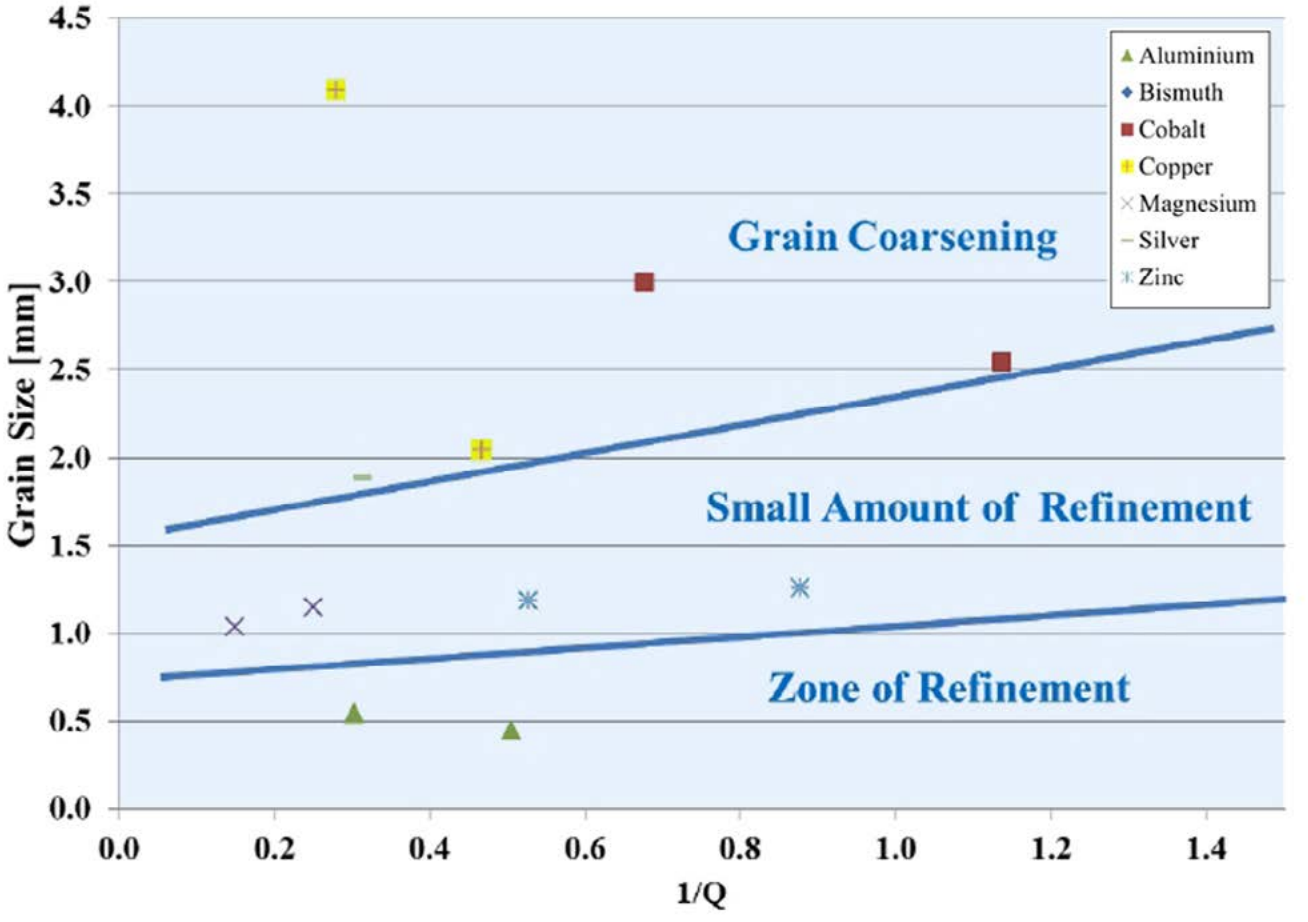

Figure 10: Relationship between the grain and the reciprocal of diffusion rate of solute atoms in the liquid at the solid liquid interface (the growth restriction factor).

plotted in Figure 11. There is a clear trend with additions of copper, bismuth and aluminium and zinc at the 0.5 Wt% levels significantly increasing the extent of grain refinement on recrystallization.

Conclusions

The addition that has emerged from this study with the greatest potential for refining the as-cast and recrystallized grain structure is aluminium. With this candidate identified future work will focus on the effectiveness of the this addition in solder joints. **SMT**

References

1. Bieler, T. Jiang, H. 2006 "Influence of Sn grain size and orientation on the thermomechanical response and reliability of Pb-free solder joints", Electronics Components and Technology Conference 2006.

2. B. Arfaei1, Y. Xing, J. Woods, J. Wolcott, P. Tumne, P. Borgesen, and E. Cotts, "The Effect of Sn Grain Number and Orientation on the Shear Fatigue Life of SnAgCu Solder Joints," 2008 Electronics Components and Technology Conference, pp 459-465.

3. Swenson, D. 2007 "The effects of suppressed beta tin nucleation on the microstructural evolution of lead free solder joints," J. Mater Science, Vol 18, No 39–54.

4.Winegard, W. 1964, "An introduction to the solidification of metals," Institute of Metals, London.

5. Maxwell, I., Hellawell, A. 1975 "A simple model for grain refinement during solidification," Acta Metallurgica, Vol 23, Issue 2.

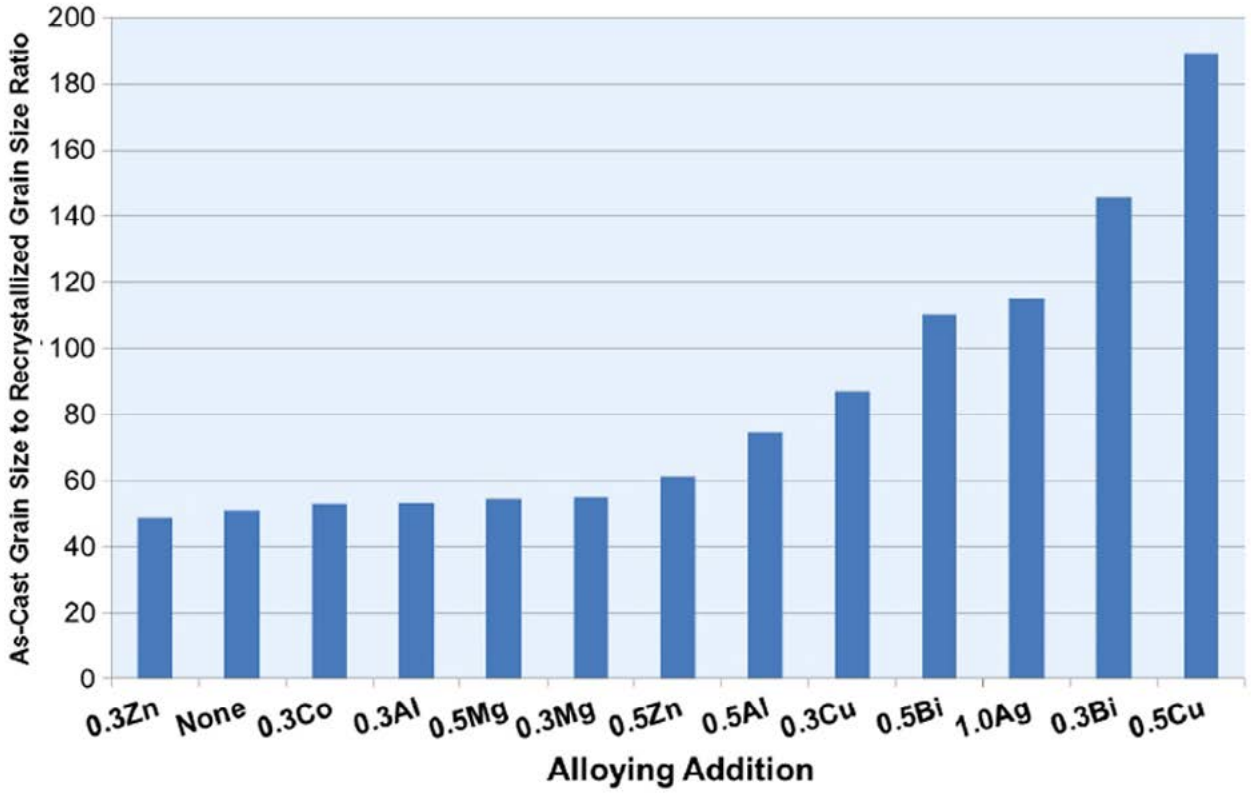

Figure 11: Ratio of as-cast to recrystallized grain size as a function of alloy.

6. Easton, M., St. John, D. 2001 "A model of grain refinement incorporating alloy constitution and potency of heterogeneous nucleant particles, Acta Materialia, Vol 49, Issue 10.

7. Easton, M., St. John, D. 2005 "An analysis of the relationship between grain size, solute content, and the potency and number density of nucleant particle," Metallurgical and Materials Transactions, Vol 36, Issue 7.

Nanometer-scale Machines to Use Graphene-based Nano-antennas

Networks of nanometer-scale machines offer exciting potential applications in medicine, industry, environmental protection, and defense, but until now there's been one very small problem: The limited capability of nanoscale antennas fabricated from traditional metallic components.

With antennas made from conventional materials like copper, communication between low-power nanomachines would be virtually impossible. But by taking advantage of the unique electronic properties of graphene, researchers now believe they're on track to connect devices powered by small amounts of scavenged energy.

Based on a honeycomb network of carbon atoms, graphene could generate a type of electronic surface wave that would allow antennas just one micron long and 10 to 100 nanometers wide to do the work of much larger antennas. While operating graphene nano-antennas have yet to be demonstrated, the researchers say their modeling and simulations show that nano-networks using the new approach are feasible with the alternative material.

"We are exploiting the peculiar propagation of electrons in graphene to make a very small antenna that can radiate at much lower frequencies than classical metallic antennas of the same size," said Ian Akyildiz, a Ken Byers Chair professor at the Georgia Institute of Technology.

Sponsored by the National Science Foundation, the research is scheduled to be reported in the journal *IEEE Journal of Selected Areas in Communications* (IEEE JSAC).

Mil/Aero007 News Highlights

Ducommun Gains Major Parker Aerospace Airbus Contract

The company has received a multiyear contract from Parker Aerospace, a unit of Parker Hannifin Corporation, to produce complex PCBs assemblies for use in the fuel management system of the Airbus A350 family of commercial aircraft. The award has a potential value in excess of $20 million over the contract period.

Sparton, USSI JV Nets $2.8M in Subcontracts

Sparton Corporation and USSI, a subsidiary of Ultra Electronics Holdings plc, announce the award of subcontracts valued at $2.8 million from their ERAPSCO/SonobuoyTech Systems joint venture.

Axis Leads 2014 UK Aerospace Youth Rocketry Challenge

Axis Electronics apprentices joined more than 25 MPs who teamed up with aerospace apprentices from all over the UK to take part in a rocket launching competition. The aim was to achieve the greatest vertical distance.

Blackfox, Lockheed Martin Celebrate 'Hire a Veteran Month'

Last month, Denver, Colorado's 9news featured a segment with Andrew Stone of Lockheed Martin discussing his company's plan to hire nearly 180 veterans for high-tech positions in assembly during Hire a Veteran Month.

ESCATEC is Founding Member of Swiss Photonics Group

"Being a founding member of this SWISSMEN professional group for the Photonics industry, puts ESCATEC in a very good position to support this growing industry in Switzerland with ESCATEC's outstanding knowledge and experience in research, design, and development," said Dr. Thomas Dekorsy, general manager.

IMET is Philadelphia's Manufacturer of the Year

IMET Corporation, a contract manufacturer providing electronics engineering services and PCB assembly, has received the 31st annual Manufacturer of The Year Excellence Award by The Greater Philadelphia Chamber of Commerce.

NASA, CCAM Partner to Advance Technology & Innovation

NASA and the Commonwealth Center for Advanced Manufacturing (CCAM) in Richmond, Virginia, have joined forces to advance technology and innovation.

U.S. Aviation Industry Poised to Enter Second Golden Age

"Emerging foreign competitors are ramping up their capabilities and technological advancements in their home markets, and are even expanding their manufacturing footprint here in the U.S. in ways that will likely alter the industry's competitive landscape through this decade and beyond," said Scott Thompson, PwC's U.S. aerospace and defense leader.

IDtechEx: Electrics Will Be the Future of UAVs

The total market value for electric unmanned aerial vehicles (UAVs) will reach over one billion dollars by 2023 according to findings in the new IDTechEx report, "Electric Unmanned Aerial Vehicles (UAV) 2013-2023."

Total Avionics Sales to Exceed $1.72 Billion

The Aircraft Electronics Association announced its third quarter Avionics Market Report for this year. In the months of July, August and September 2013, total worldwide avionics sales amounted to $1,721,888,397.14, or more than $1.72 billion, as reported by the 20 aviation electronics manufacturers participating in the report.

BLACKFOX EXPANDS

Press Release

Blackfox Training Institute, LLC., headquartered in Longmont, Colorado, reports that it officially expands into three additional locations with new facilities.

November 2013:

Blackfox Training Institute reports that it officially expands its training and certification services to three additional locations with new facilities. In addition to the Blackfox headquarters located in Longmont, Colorado, **Blackfox now has new facilities in Tempe, Arizona, Guadalajara, Mexico, and Penang, Malaysia.** Each of these facilities offers the same IPC Certifications and Blackfox Skill-based Certifications as offered in Colorado. Additional locations are planned in the near future.

This expansion was essential in order to create a channel for delivering the IPC Quality Standards and skill-based training and certification to areas of high demand and reduce the travel costs for customers nearby. Each of the Blackfox Training Centers have resident Master IPC Trainers as well as Master IPC Trainers that travel the world delivering all of the training programs at their customers' facilities.

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Supplier Selection Key to Assembly Reliability

by Steve Williams
STEVE WILLIAMS CONSULTING LLC

SUMMARY: As with any electronic assembly, or electronic device for that matter, the quality of the raw printed circuit board is the most critical link in the product reliability chain. The key to managing this risk is the supplier selection and qualification process.

Defining terms is always a good point to start, and from a practical standpoint, reliability can be simply defined as performance to both the design intent for the expected life cycle of the product.

When asked to discuss supply chain strategy, EMS and OEMs often respond with something like, "Yes of course, we have a purchasing department." Supply chain management has progressed far beyond the old school purchasing mentality to become a key component of the modern business organization. We are all just pieces in the supply chain puzzle that is responsible for getting the ultimate customer's product to market.

The first step in developing an SCM program is to identify all purchased materials (and services) into two categories, standard and critical. Suppliers of critical materials are the ones that need to be controlled; you probably don't want to spend too much time managing your supplier of stationary and paperclips. A raw PCB supplier is a perfect example of a critical material, both from a technology complexity standpoint as well as a risk level. It only takes one defective $25 printed circuit board to destroy $2,500 worth of perfectly good electronic components.

Qualification Criteria

Strategically, deciding how to qualify new suppliers is the most critical step in the process. Of course, there must be an overriding strategy governing supplier identification and selection, but that would be a whole other column. The underlying tool should be an audit/survey that measures the quality system, financial viability and technology. Audits are frequently based on ISO 9000, which would be preferable if ISO registration is another qualification criterion (which is highly recommended). There should be a re-audit frequency established and some provision for the supplier to provide demonstration of continued capability for the time period between audits. This could be in the form

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What is found too often are that suppliers have been grandfathered onto an AVL because they have always supplied materials, and that no one has ever audited the facility. Or, the only existing control is a self-audit that the supplier completes with no verification (which is probably ok since we all know that no one ever embellishes on their capabilities when filling out one of these!).

Product/Process Validation

Printed circuit board supplier qualification should include some form of reliability test, and one that has proven very effective is IST (interconnect stress testing). IST measures the changes in resistance of the PTH, blind/buried vias, micro vias and inner layer connections as holes are subjected to thermal cycling. The ability to distribute this thermal stress will provide an indication of the inherent integrity and reliability of the PCBs.

> ***There are two types of testing: Before Assembly Condition to determine the average cycle to failure and After Assembly Condition to determine the robustness of the PTH structure to withstand the thermal load from an assembly process.***

There are two types of testing: Before Assembly Condition to determine the average cycle to failure and After Assembly Condition to determine the robustness of the PTH structure to withstand the thermal load from an assembly process. Testing completed in accordance to IPC-TM-650 Method 2.6.26. The IST analysis report should include any failure identification, micro sections, pictures, graphs, and tables that represent the testing results.

AVL

Once all critical materials and qualification criteria have been identified, an AVL (approved vendor list) can be developed. This can be called many things; approved supplier list, approved manufacturer list, qualified vendor list, but it is simply a listing of all the suppliers that are approved to supply critical materials to a company. This controlled, living document can be organized any number of ways, but must contain at a minimum the supplier name, material supplied, and current performance ratings. The AVL should be current and updated regularly (usually quarterly).

Supplier Rating

Once all of this is in place, a set of metrics must be developed to monitor the supplies performance on a regular basis. This can be as complicated or simple as the imagination allows, but must include on time delivery, quality, and service as key reporting metrics. This data needs to be communicated to each supplier on a regular basis (usually quarterly) and should become part of the collaborative customer/supplier process.

Printed circuit board manufacturers have always expected their OEM and EMS customers to actively manage them; however, many still have not filtered that expectation down to their sub-suppliers. Customer audits are a way of life for printed circuit fabricators, but it is surprising to see how many of them have never visited, much less audited, their own key strategic suppliers. I think it is reasonable to expect that a supplier actually visit, audit and collaborate with their key sub-suppliers on a regular basis.

Is supplier selection and qualification a magic bullet to cure all reliability risks? Of course not, but without highly qualified suppliers reliability is an unattainable goal. **SMT**

Steve Williams is the president of Steve Williams Consulting LLC (www.stevewilliamsconsulting.com) and the former strategic sourcing manager for Plexus Corp. He is the author of Quality 101 Handbook and Survival Is Not Mandatory: 10 Things Every CEO Should Know About Lean. To read past columns, or to contact Williams, click here.

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Predicting Strength and Pad Cratering Failures Under BGA Pads

by Mudasir Ahmad
and Qiang (Johnson) Wang
CISCO SYSTEMS

Previously published in the 2013 IPC APEX EXPO Conference Proceedings

Abstract

In the past few years, several papers, test methods and methodologies have been developed to estimate pad cratering under BGA pads in PCB assemblies.

However, almost all the tests and methodologies proposed so far have the following shortcomings:

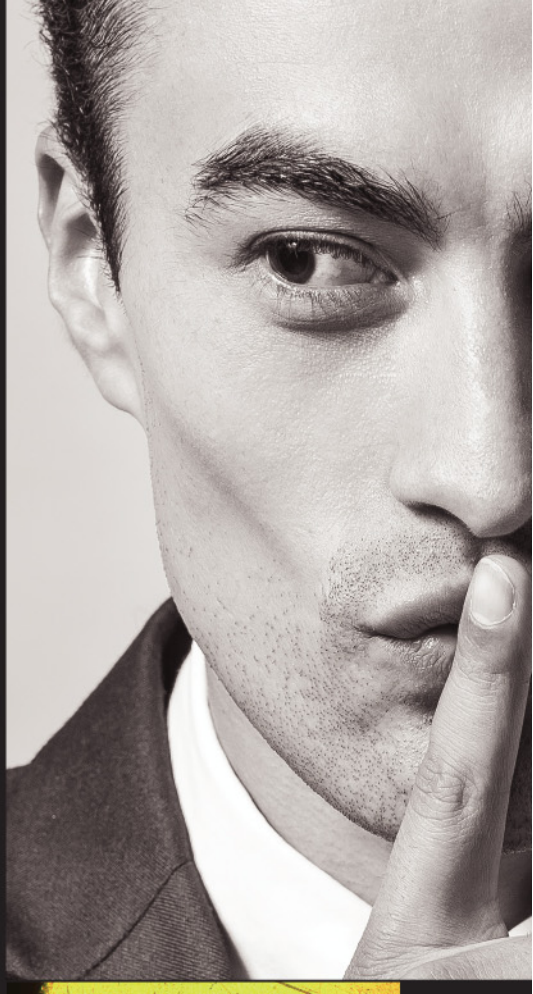
1. They are destructive. The samples tested are broken and the failure mode(s) observed to determine the propensity for cratering.
2. They require testing several samples using different test methods (bend, shock, pull, shear or acoustic), but there is no easy correlation between the different test methods.
3. They can be used for relative comparisons, but there is no easy way to translate the correlations into failures in actual functional board level assemblies.

While these tests have helped mitigate pad cratering significantly, the industry still needs the following:

1. A non-destructive way to predict whether a certain PCBA design (BGA and PCB combination) is likely to result in mechanical strain induced pad cratering failures, long before the product has been built.
2. An easy to use way to correlate PCB level pad pull tests done per IPC-9708 and monotonic bend tests per IPC-9702, so that the design can be optimized to mitigate pad cratering failures during qualification testing.
3. An easy to implement design to detect pad cratering in a functional assembly, so that if a failure is observed in the field, it is easy to determine if the failure is due to pad cratering.

Pad Cratering?

Shhhhh! We don't talk about that. . .



As recent as two years ago, **pad cratering** was something our industry didn't want to talk much about. Whose problem is it? The supplier? The designer? The fabricator? the OEM? the Customer?

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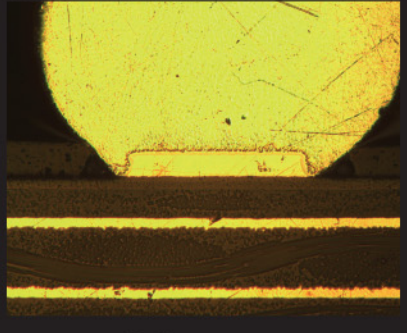

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Detecting a failure as soon as it occurs is critical in identifying the source of the mechanical strain that resulted in the failure, which in turn can help quickly resolve the issue.

In this study, using extensive experimental data, a detailed methodology is outlined to show the relationship between board strain, solder joint strain and force to failure in monotonic bend testing and pad pull testing. In addition, the correlation between monotonic bend testing and pad pull testing is shown, such that the results of pad pull testing can be used to estimate the likelihood of observing pad cratering failures in PCBAs during bend testing and manufacturing operations. The methodology can be used by designers to estimate the optimal combination of package and PCB design variables to minimize the likelihood of pad cratering and other solder joint failures during testing and field operation.

Finally, methodologies to predict and determine pad cratering failures quickly in field operations are also discussed and outlined.

Introduction

The exponential growth of the internet and smart connected devices is driving a need for faster, smaller and more efficient

devices. This exponential growth is being propelled by the indomitable Moore's law, which has aided the rapid miniaturization of transistors. To support the shrinking of transistors, the density of interconnects from the silicon to the system has been rapidly increasing. This increase in density requires reducing the size of interconnects, ranging from the flip chip bumps connecting the chip to the substrate, to the connectors connecting line cards to backplanes to drive networking equipment.

Key to this rapid shrinking of devices and interconnects is achieving an acceptable level of reliability during the expected assembly, manufacturing and use of these devices. The smaller and thinner the device, the more susceptible it could be to mechanical loading conditions (bend, drop, shock, vibration etc.). Over the past several years, the industry has developed multiple test standards to evaluate and benchmark the reliability of devices under different use conditions. Device suppliers are required to demonstrate that their device passes the required tests before the device is accepted as part of a finished system.

However, given the wide range of potential failure modes that could occur, a whole plethora of test methods are currently being used, and suppliers have to perform more standard tests to demonstrate reliability. For example, suppliers need to pass IPC/JEDEC 9701 (Accelerated Temp Cycling), 9702 (Monotonic Bend), 9703 (Shock), 9708 (Pad Cratering) etc., to demonstrate that a BGA component can be reliably mounted on a PCB. While the approach of defining test methods and requiring suppliers to meet test standards is fairly common, it poses several challenges:

1. The tests are expensive and time-consuming. The added cost and time required to perform the tests inevitably gets transferred to the OEM, and eventually to the consumer.
2. Since the tests require physical samples, by the time the tests are performed, several aspects of the device have already been designed. If a device fails the test, more time and cost is involved in root causing the failure and iteratively redesigning and testing the device to pass the test.
3. There is little correlation between the tests, so each test is usually performed sequentially. Consequently, passing one test could invariably mean failing another, making design optimization even more difficult and time consuming. With rapidly shrinking design cycles, repetitive testing and optimization is a luxury most device suppliers can ill afford.
4. There are several "test escapes" because there is virtually no way to guarantee that each potential failure mode can be captured for rapidly evolving devices by the established test methods. Moreover, end-use conditions rapidly evolve too, and even after passing all the tests, when a field failure occurs, it is almost impossible to determine the root cause of the failure (unusual use conditions or a design flaw).

Given all these challenges, there is a growing need to develop ways to predict failures during the design phase, and to correlate failures

from one test condition to another test condition. If designers know a priori the tradeoffs in the design that they need to consider, the design time and optimization can be improved significantly.

In this study, we present the analytical correlations derived between two test standards: IPC/JEDEC-9702 and IPC/JEDEC-

9708, and how those correlations could be used to predict a potential failure much earlier in the design process. Moreover, the predictions can be used to estimate the optimal design to mitigate potential failures both during testing and in the field. Finally, we present potential ways to detect a failure real time in field use conditions.

Variable	Description	Category	Value
A	Package Type	FCBGA 1pc Lid	-276.14
		FCBGA No Lid	-176.21
		Wirebond PBGA	-1137.23
B	Package Size (mm)	-	
C	PCB Thickness (mils)	-	
D	PCB Pad Size (mils)	-	
E	Pkg Pad Size (mils)	-	
F	Ball Pitch (mm)	-	
G	Joint Top Strain (με)	-	

$$PCB\ Strain\ (\mu\varepsilon) = A - 22.02 \times B - 28.43 \times C + 184.74 \times D + 323.14 \times E - 5062.76 \times F + 277445 \times G$$

Table 1: PCB Strain Prediction Model.

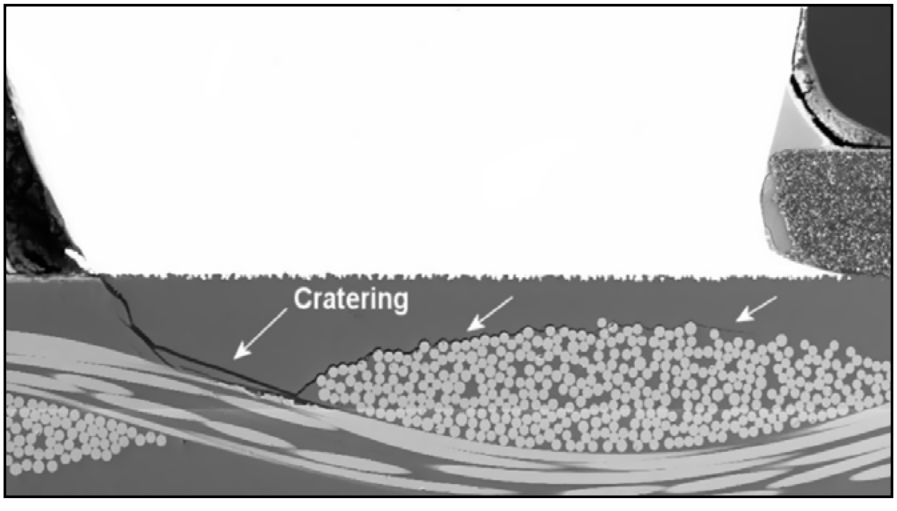

Figure 1: Example of a pad cratering failure[4].

Monotonic Bend Test (IPC/JEDEC 9702)[1]

The monotonic bend test standard was developed specifically to address interconnect failures in BGA components mounted on PCBs, subjected to flexure loading conditions. As many as seven potential failure modes could occur in the immediate vicinity of the BGA interconnects during monotonic bending conditions. The test method strives to derive a single damage metric (board strain) that could result in failure. Board strain can then be used to determine how much flexure a given BGA/PCB combination can handle, and to establish minimum strain levels that a given assembly can be expected to withstand.

In a recent publication[2], we have demonstrated using extensive numerical analysis that a combination several design variables could be used to predict board strain to failure, with reasonable accuracy, and to help designers optimize the parameters to achieve a target board strain. The prediction equation is shown in (Table 1 and Figure 1).

This model can be used to estimate the PCB strain to failure for a given package and PCB combination during the design phase even before samples are built. A few important caveats to note:

a. The model itself does not give the definitionof a failure. It provides the correlation between design variables and joint strain. The

typical joint top strain (G) values observed are approximately 20,000 με for an electrically open solder joint failure. This value can be used to estimate the PCB strain to failure with an appropriately selected safety margin.

b. The model is based only on the failures associated with joint top strain (such as brittle solder joint fracture), so it is applicable only to packages in which the ratio of joint top and bottom strain is equal to, or close to 1.

Details on how this relationship was derived are outlined in[2]. However, we still need to develop a similar predictive capability for the pad cratering test method (IPC 9708).

Pad Cratering Test Method (IPC-9708)[3]

The IPC-9708 test method was developed to address a specific failure mode: pad cratering. Pad cratering is known to occur as a cohesive failure in the PCB laminate directly underneath a BGA at the corners, when subjected to mechanical loading conditions (Figure 1).

The IPC-9708 test method comprises of three different test methods: a pin pull test, a cold ball pull test and a shear test. Each test is aimed at determining the force it takes to induce a pad cratering failure underneath a BGA pad, but each test has different tradeoffs.

In this study, we focused specifically on the pin pull test because it minimizes the effect of the solder from the test by attaching a pin directly to the pad.

The experimental pin pull data derived from the testing is shown in Figure 3.

The results of this testing indicate a clear and strong relationship between pad size and the average pull force (for the case of a 90° pull). Given the strong correlation of the average pull force to pad size, we can determine if the stress underneath the PCB pads is the same for each pad size. If the postulation is valid, then the stress-to-failure for the experimentally derived pull forces-to-failure should be constant for all the pad sizes tested.

Numerical Model

Consequently, a set of numerical models were developed, to estimate the stress underneath the PCB pad corresponding to each pad size. A detailed numerical model was built to simulate the pin pull test. BGA pads of varying diameter were simulated and pulled to estimate the tensile stress built underneath the pad. Quarter symmetry was used to model the pads, as shown in Figure 4. The force applied in the model corresponded to the forces applied to the pad sizes shown in Figure 5.

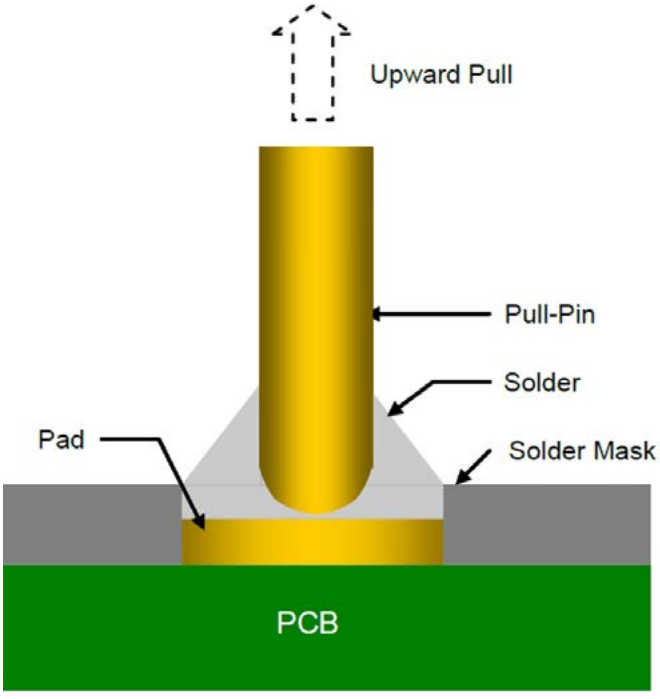

Figure 2: Test setup schematic[4].

The results of the numerical analysis are shown in Table 2. SY represents the vertical tensile stress, while VM represents the Von Mises Stress (max and min values). The percent change is the difference between the max and min values.

The simulation results show that the stresses (SYmax – SYmin) underneath the PCB pad are within 20% of each other, and about 6% on average. This variation is within the experimental data variation for pull force values as shown in Figure 3. Consequently, one can use the average Delta SY value to establish that the threshold stress-to-failure underneath the PCB pad for this material (dicy cured high-T_g FR-4 (HTD) is approximately 333,706 Pascal (48,400 PSI).

From Figure 3, it can also be seen that for the high T_g filled phenolic (HTFP), the pull

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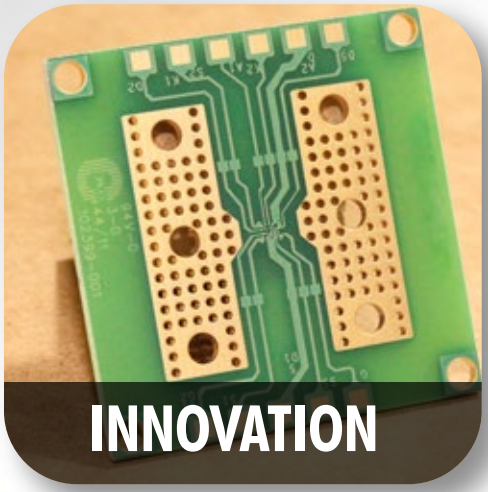

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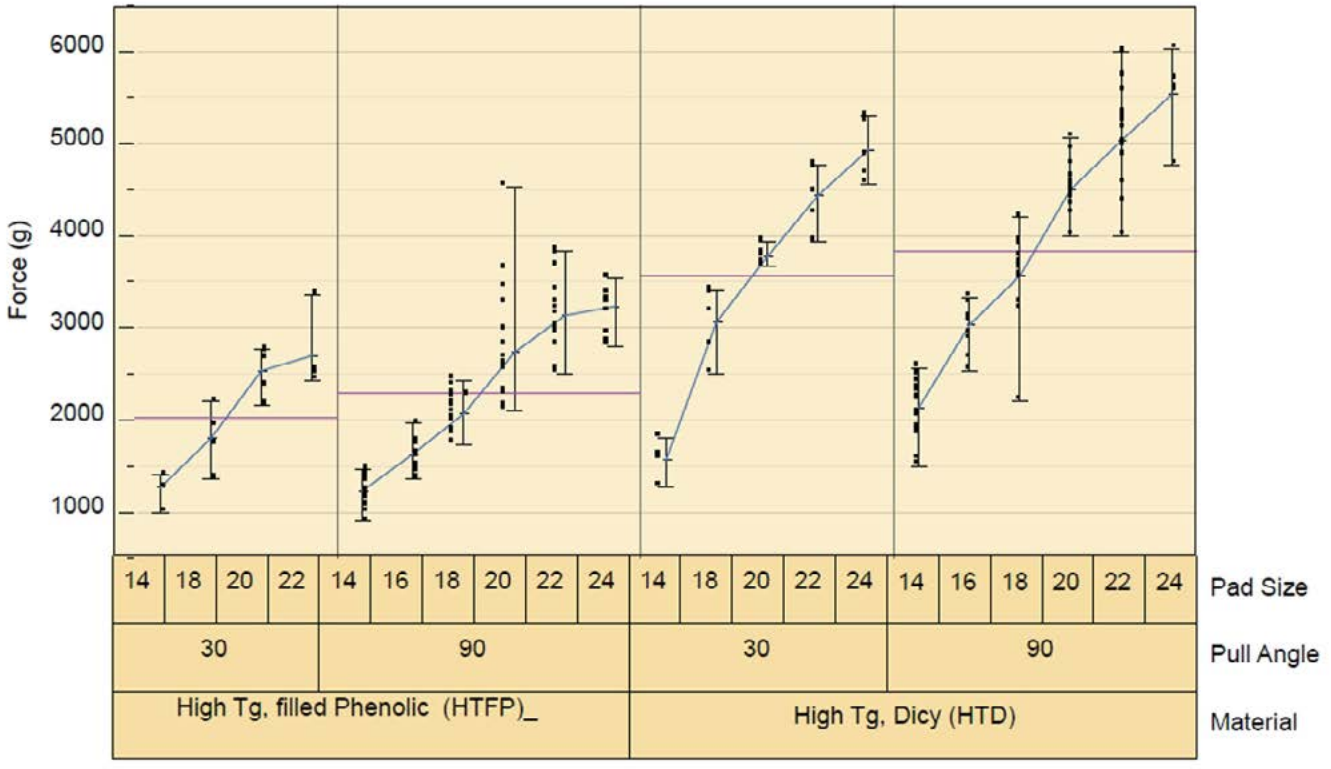

Figure 3: Effect of pull angle (5 mil stencil, 5 mm/sec pull speed, 500 µm pin size)[4].

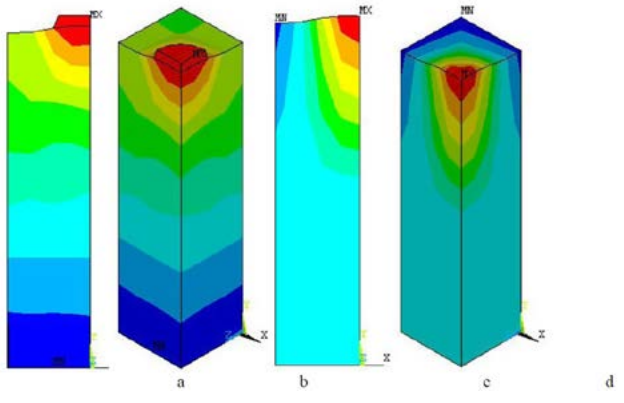

Figure 4: Numerical analysis results: (a) vertical deformation, front view; (b) vertical deformation, isometric view; (c) vertical tensile (sy) stress, front view; (d) vertical tensile (sy) stress, isometric view.

force values are also linear (for the 90° pull) and scale linearly with the values of the HTD. A comparison of the two sets of pull force values yields a ratio of 0.6. Consequently, it can be estimated that the threshold stress-to-failure underneath the PCB pad for the HTFP material is roughly 199,285 Pascal (28,903.93 PSI).

Now that we have the estimated failure threshold stresses for the two materials from the pin pull test, we can re-run the monotonic bend test analysis and extract the typical stresses seen under the BGA pad on the PCB during bending.

Correlation Between Monotonic Bending and Pin Pull Testing

The entire monotonic bend model was re-run to derive the correlation between board strain and stresses under the BGA PCB.

The PCB material assumed for the analysis was the HTD material. Guidelines for HTFP could be derived from the same analysis, by using a de-rating factor of 0.6. These guidelines could also be used for any new material other than HTD and HTFP, as long as the de-rating factor of the new material relative to HTD can be derived. The de-rating factor can derived

Pull Test Modeling Results										
Pad Size (mils)	Force (g)	U_Y (Inch)	SY_{min} (PSI)	SY_{max} (PSI)	SY_{max} - SY_{min} (PSI)	% Change	VM_{min} (PSI)	VM_{max} (PSI)	VM_{max} - VM_{max} (PSI)	% Change
24	**5500**	7.17E-04	2.20E+04	6.68E+04	4.48E+04	0	1.92E+04	5.73E+04	3.81E+04	0
22	**5000**	6.67E-04	1.86E+04	6.68E+04	4.82E+04	-0.00449	1.68E+04	5.84E+04	4.16E+04	9.35
20	**4500**	6.16E-04	1.56E+04	6.76E+04	5.20E+04	1.179994	1.47E+04	5.98E+04	4.52E+04	18.65
18	**3500**	4.95E-04	1.13E+04	6.03E+04	4.91E+04	-9.63462	1.12E+04	5.38E+04	4.26E+04	11.998
16	**3000**	4.40E-04	9.05E+03	6.06E+04	5.16E+04	-9.18389	9435.7	5.43E+04	4.48E+04	17.804
14	**2100**	3.22E-04	5.92E+03	5.10E+04	4.50E+04	-23.6912	6558.2	4.57E+04	3.92E+04	2.8442
Average				**6.22E+04**	**4.84E+04**	**-6.88904**	**1.30E+04**	**5.49E+04**	**4.19E+04**	**10.10862**

Table 2: Pull force and stresses underneath BGA pad.

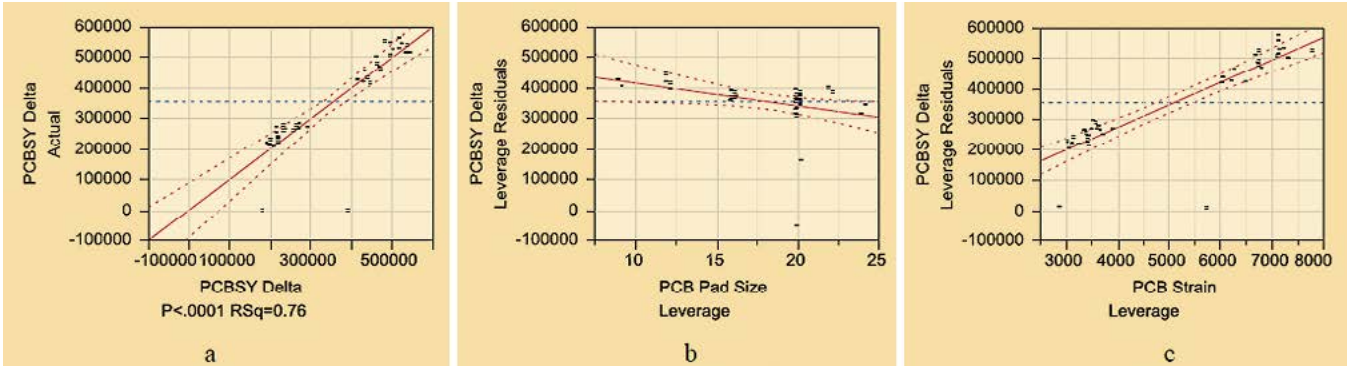

Figure 5: (a) Accuracy estimate of prediction model; (b) correlation between PCB SY and PCB pad size; (c) correlation between PCB SY and PCB global strain.

from pin pull tests performed in accordance with IPC-9708 for the new PCB material(s) and compared with HTD data.

Since the board strain can be predicted by the assembly design variables (Table 1), all we need to do is derive the relations hip between board strain and PCB BGA pad strain. That way, we can predict what amount of board strain can result in pad cratering failures. It is important to note that 3 strain gages are attached to a PCBA during monotonic bend testing per IPC/JEDEC 9702: (1) at a location far afield from the package perimeter (global strain), (2) underneath the cornermost BGA (local strain) and (3) underneath the package center (local strain). Since local strain is very difficult to measure accurately, the global strain has been used to derive all the guidelines. The results of the analysis are shown in Figure 5.

The prediction equation relating PCB pad size, PCB global strain and PCB pad cratering stress is shown below:

$$PCB\ Pad\ Cratering\ Stress = 114506.246 - 7432.648 * PCB\ Pad\ Size\ (mils) + 73.96825 * PCB\ Global\ Strain\ (ue)$$

From the results, one can conclude that a stress-to-failure threshold stress under the BGA pad of 333,706 Pa (HTD) translates to a global PCB strain of about 5000 με (Figure 5). That means that if a given package assembly is subjected to more 5000 global microstrain, it could result in complete pad crater rupture. It is important to note that this is strain to complete rupture, not partial pad crater. Similarly, for the HTFP material, the global PCB strain to crater translates to 3000με (corresponding to a threshold stress of 199,285 Pascal).

It can also be seen from Figure 5 that the selected pad size can significantly alter the PCB strain. For pad sizes that are 20 mils and below, the PCB stress is higher than the threshold stress value. This is borne out in experimental bend test results, where for pad sizes 20 mils or below, the failure mode is predominantly pad cratering. In addition, it has been shown in experimental tests that increasing the pad size from 20 mils to 25 mils significantly reduces the propensity for pad cratering[4].

Detecting Pad Cratering Failures

Now that we have a criterion for acceptable PCB strain (3000–5000 με), we face another challenge. How do we determine if this threshold has been exceeded in a real assembly? It is impractical to place strain gages on live boards because they cannot be calibrated to reflow temperatures and cannot easily be assembled on every location on every board in production. We need some way to indicate when the strain threshold has exceeded the 3000–5000 με range. The indicator does not have to be as precise as actual strain gages, but accurate enough to give an estimate that the strain exceeded the design threshold.

One possibility is to design the trace from the cornermost BGA pad to fail at a preset strain threshold. The trace could be narrowed down to create a stress concentration that could result in the trace cracking at a level corresponding to the failure threshold (Figure 6).

However, in looking at the stress/strain curve of the typical trace copper material used in PCBs (HTE, Figure 7), it is clear it will take an applied strain of 60,000 με (6% elongation) to cause complete rupture. Making a trace that could rupture at a strain level in the 3000–5000 με strain range without significant process/design modifications does not appear to be practical for high volume manufacturing.

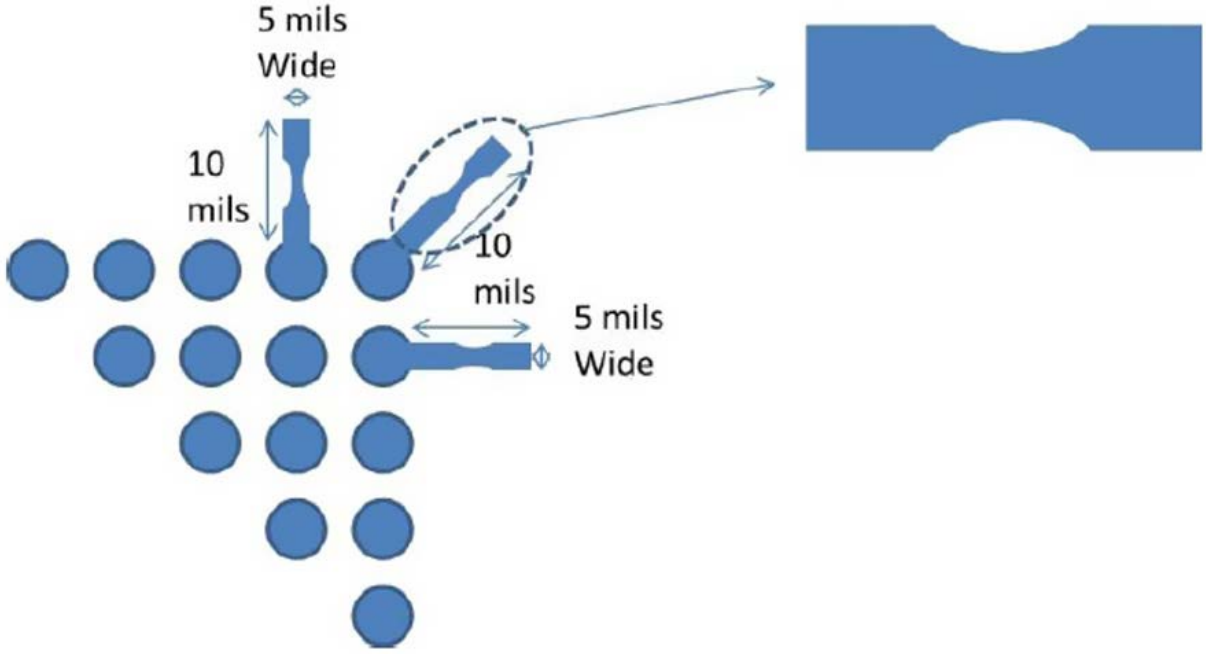

Figure 6: "Mousebite" trace design to fail at preset strain threshold.

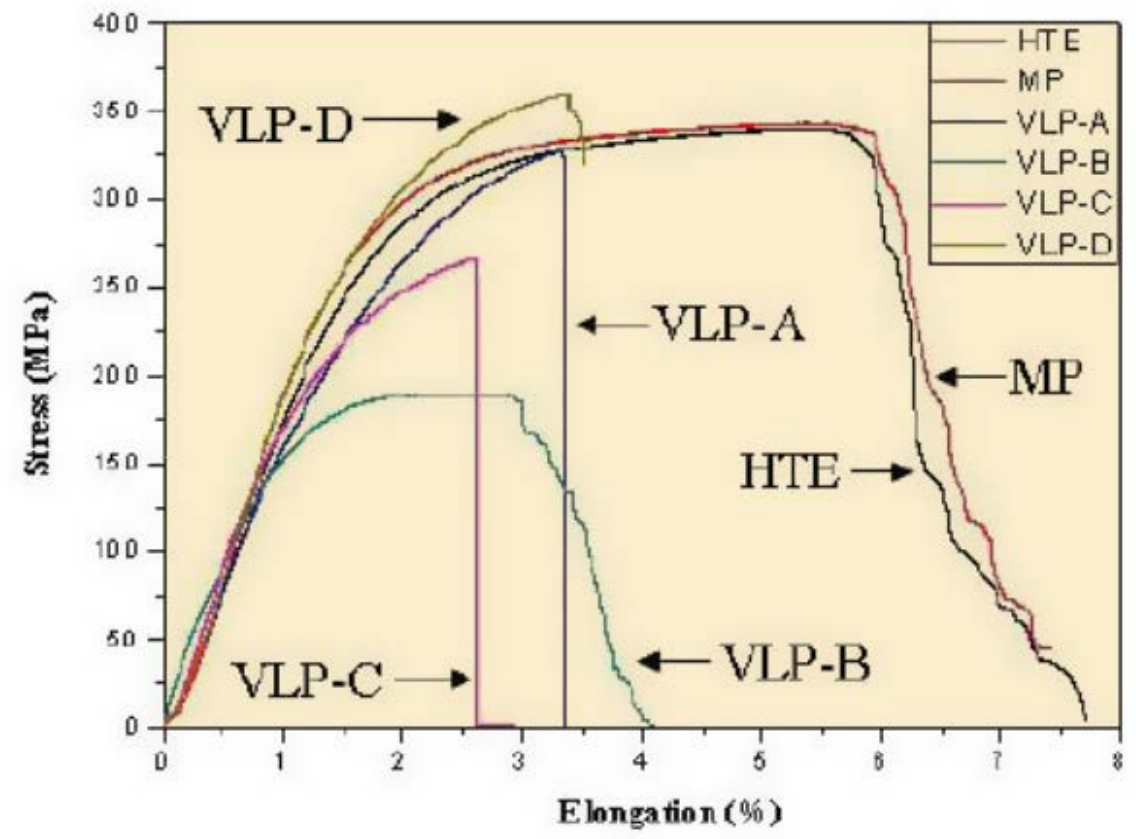

Figure 7: Stress/strain curve of different PCB copper trace materials. The most commonly used is high-temperature electrolytic (HTE)[5].

Consequently, a different solution was sought, that was easier to implement in high volume production and could be scaled easily and cost effectively. While other techniques for in-situ monitoring have been proposed, they require custom connectors and designs that are not very easy and cost effective to deploy on hundreds of components on linecards in production [6]. It has been known for quite some time in the industry, that ceramic capacitors are prone to mechanical strain related failures. In fact, the strain-to-failure of ceramic capacitors under flexural loading has been very well characterized for a whole range of capacitor sizes (Figure 8).

It can be seen from Figure 8 that if a 2225 capacitor is mounted at the diagonal location closest to the corner of a BGA, it is likely to fail at strains in excess of 3000–5000 με. The failure rate is expected to be high enough to reliably detectable. An electrical circuit such as that shown in Figure 9 can be used to monitor the capacitor in real time, and to determine the precise time at which it has failed. Knowing the time of failure is critical to a root cause analysis: if it failed during assembly, the precise assembly process step that caused the failure can be identified. If it failed during use conditions, the specific instance of usage could be identified.

The methodology for detection involves connecting the capacitor (SMD) to a 555 Timer Circuit and an Electrically Erasable Programmable Memory (E^2PROM). The memory register will be set to First-In-First-Out (FIFO), to record x-minutes of data. This will serve as a "black box." A threshold value of baseline capacitance can be preset or programmed into each board based on the T0 capacitance value. The circuit will log the time vs. capacitance over time and will show any changes in capacitance over time—caused by a crack in the capacitor. The

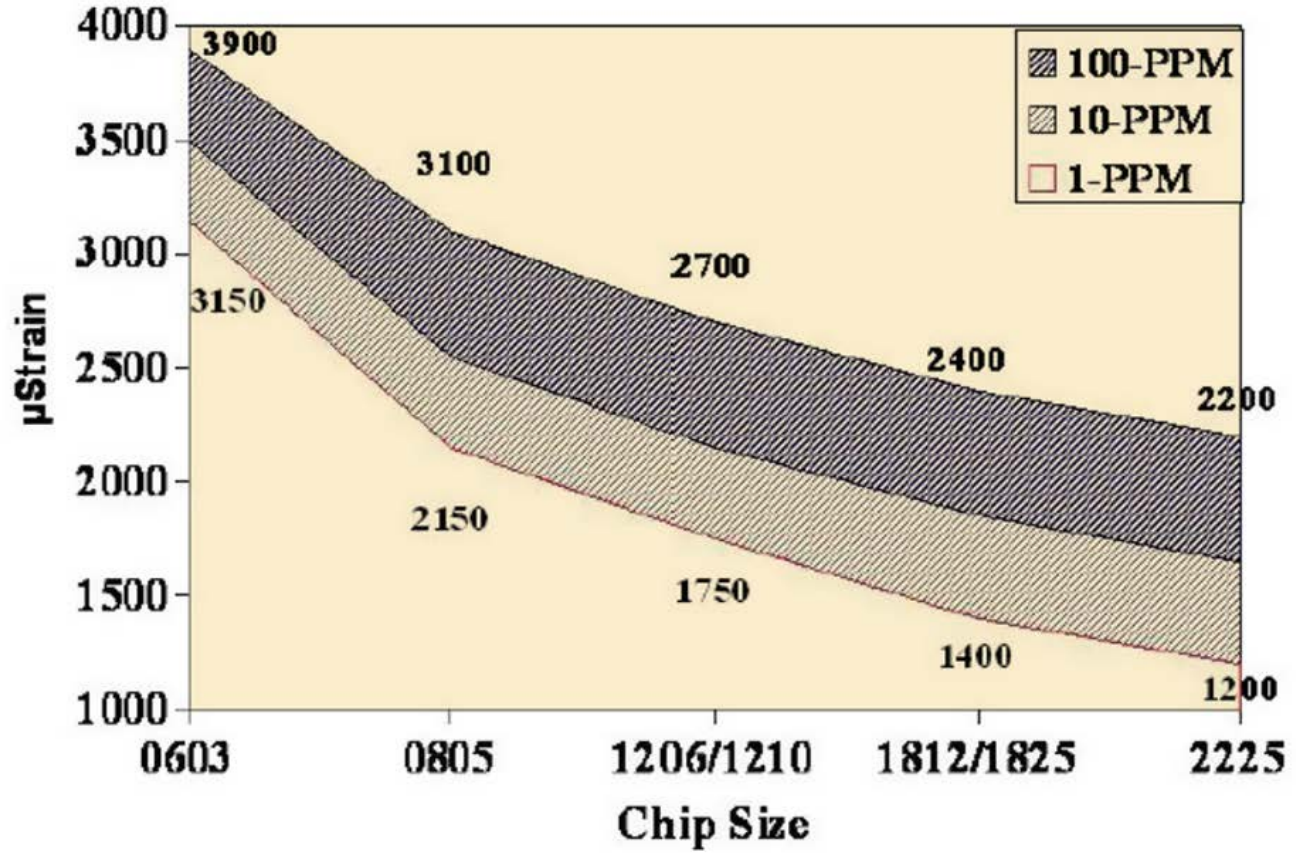

Figure 8: Chip size versus strain required to achieve 100, 10, and 1 ppm failure rates (typical)[7].

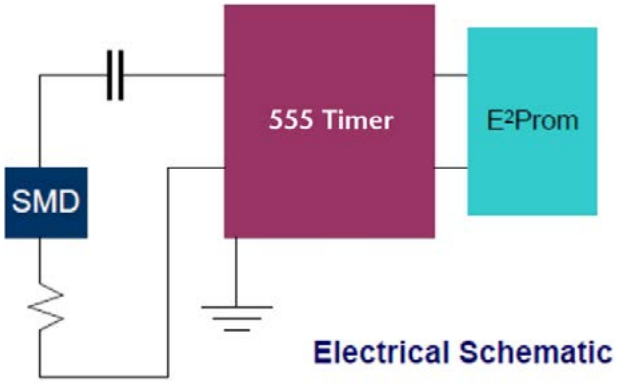

Figure 9: Electrical schematic of circuit to detect capacitor change (capacitor is strain monitoring device, or SMD).

timer and memory could be located at a convenient distance away from the part(s). Several devices can be connected in parallel to the same Timer/E^2PROM circuit, to give the effective capacitance change. If any device fails, the circuit will record the event.

Relatively simple cross section analysis can also be performed later to reveal the classical flexure-induced failure mode as shown in Figure 10, thus verifying the failure.

Thus, a commonly known and understood failure mode in ceramic capacitors could actually be turned into an easy to implement detection method for excessive strains in PCB assemblies. Ceramic capacitors are cheap, easy to mount and require no significant changes to the standard SMT assembly process. The region around the diagonal of a BGA is generally known to be a high strain region and no active components are recommended for mounting in this region. Mounting the sensing capacitor in this location should not result in significant loss of board real estate either.

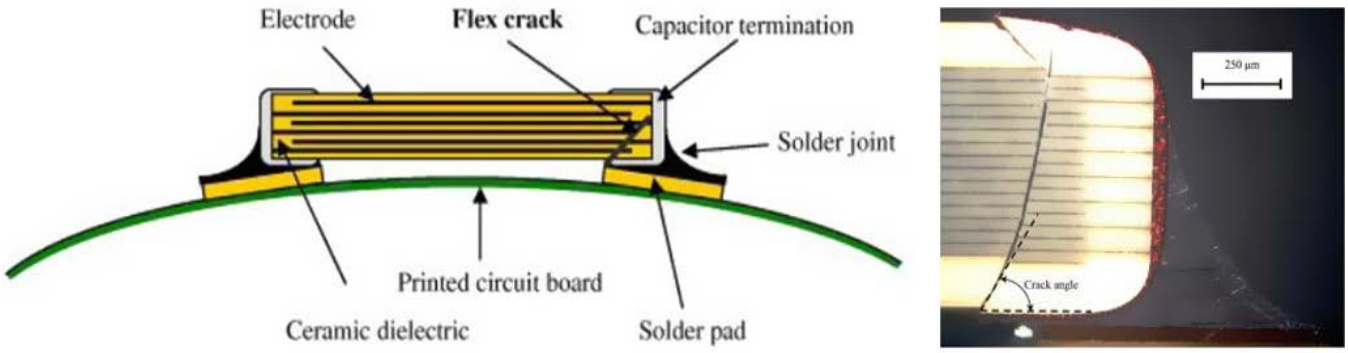

Figure 10: Typical crack signature of chip capacitor under flexural loading[8].

Conclusions

A detailed methodology for correlating pin pull testing with monotonic bend testing metrics has been presented. With the data presented in this paper, the threshold stress in the PCB material for creating full pad craters has been derived. In addition, the global PCB strain range to reach the threshold stress in the PCB material has been derived. Thus, the amount of strain it could take to cause a full pad crater in a PCB material can be estimated upfront. The prediction can be used to optimize the package and PCB design variables required to minimize the likelihood of pad cratering. Finally, a methodology for real time detection of high strains, which could result in pad cratering failures, has been outlined.

Future Work

A detailed test vehicle to validate the correlation between monotonic bend testing, pin pull testing and capacitor sense testing is currently being developed. The results of the experimental data will be used to further refine the results presented in this paper. **SMT**

Acknowledgments

The authors would like to thank the team and management of the Component Quality and Technology Group at Cisco Systems, Inc.

References

1. IPC-JEDEC 9702, "Monotonic Bend Characterization of Board-Level Interconnects,"

2. Wang, Q., Xie, W., Ahmad, M., "Experimentally Validated Analysis and Parametric Optimization of Monotonic 4-point Bend Testing of Advanced BGA Packages", ICEPT-HDP, 2012.

3. IPC-9708, "Test Methods for Characterization of Printed Board Assembly Pad Cratering,"

4. Ahmad, M., et. al, "Comprehensive Methodology To Characterize And Mitigate BGA Pad Cratering In Printed Circuit Boards", Journal of SMT, Volume 22-1, 01/31/2009.

5. Wang, D-S., et al, "Mechanical properties of electrodeposited copper foils for PCB applications", International Microsystems, Packaging, Assembly and Circuits Technology Conference (IMPACT), International Conference on Electronics Materials and Packaging (EMAP).

6. Uppalapati, R.; et al, "Voltage in-situ electrical metrology for test-to-failure BGA component shock margin assessment", Electronics Components and Technology Conference (ECTC) 2012.

7. Prymak, J., et. al, "New Improvements in Flex Capabilities for MLC Chip Capacitors", 2006 CARTS Conference, Orlando, FL., April 3-6.

8. Keimasi, M. et. al, "Isothermal aging effects on flex cracking of multilayer ceramic capacitors with standard and flexible terminations", Journal of Microelectronics Reliability, Volume 47, Issue 12, December 2007, Pages 2215–2225.

Reliably Clean

by Barbara Kanegsberg
BFK SOLUTIONS

Does cleaning contribute to reliability? Cleaning darn well better contribute to reliability, or else why bother? In fact, since all cleaning processes, including defluxing processes, have the potential to modify surfaces, cleaning should happen only when needed.

No-Clean Flux

In the far-distant past, electronics assemblers assumed that cleaning electronics assemblies was a necessary evil or an exercise to satisfy some long-established contractual requirement. That cleaning requirement may or may not have related to performance.

The development of no-clean fluxes eliminated the need for cleaning in many, although not all, applications. RMA flux was and still is required for some high-reliability applications. However, defluxing, which is cleaning, has gradually reappeared, for a number of reasons. A no-clean flux is not a zero-residue flux. No-clean fluxes leave a residue on the electronics assembly. However, the flux residue may not degrade performance for the intended application.

Understanding the application is the key to figuring out where cleaning is needed. In military, aerospace, and biomedical applications, the customer requires long-term reliability; and there are potential catastrophic consequences of residue on even short-term performance. Electronics assemblies have changed. Miniaturization, dense population, and low-standoff assemblies are more likely to entrap even low-residue fluxes; and these entrapped fluxes can be sources of performance problems.

This brings us to the concept of soil and cleaning. Soil is matter out of place. Cleaning is removal of matter out of place, without damage to the product and without undesirable, sometimes subtle, surface modification. Soils include manufacturing process materials, such as flux, which serve an important function during assembly. Soils encompass both conductive and non-conductive materials. Industry standards for electronics assemblies deal mostly with conductive residues. Be aware that non-conductive residues can also be sources of reliability problems.

Do Cure-Alls Exist?

True story! Grandpa, an engineer, was babysitting our daughter. We returned to find the young lady's diaper firmly affixed at half-mast and secured by what seemed like yards and yards of duct tape. Duct tape was an expeditious quick-fix. But duct tape is not a cure-all. When

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we hear comments to the effect that cleaning is not needed because the assembly will be coated, we recall the duct-taped diaper episode. Electronics assemblies are coated to protect the assemblies from the environment. Attempting to use conformal coating as a short-cut to avoid cleaning is ill-advised, particularly for high-reliability parts. Poor adhesion of the coating to the assembly is a symptom of inadequate cleaning. Poor adhesion is sometimes a blessing in disguise, because it is a signal to improve the cleaning process. Even worse is the situation in which soils are trapped under the coating, only to cause performance problems later on.

Attempting to use conformal coating as a short-cut to avoid cleaning is ill-advised, particularly for high-reliability parts.

But it Passed the Tests

We hear comments that run along the lines of: "It passed the tests, but the customer didn't accept the assembly. They said it wasn't reliable." Industry standard tests for resistivity may be sufficient, but maybe not. Maybe the tests that were performed were not sensitive enough or sufficiently specific. Understanding the details of ionic tests matters very much [9]. Perhaps ion chromatography that allows you to distinguish among the types of ionic species is the right approach [4].

Perhaps the testing is not capturing the full range of contaminants of concern. Electronics assemblers have generally been concerned with ionic contamination, with conductivity issues. Conductive residue results in immediate performance and reliability issues. But non-conductive residue has also been found to be responsible for long-term reliability issues. H. Schweigart asserts that "flux removal after soldering is only one process step when using cleaning solutions to solve or avoid climatic problems." He explains that in addition to flux residue, dust combined with moisture can result in dust dendrites. In addition, other contaminants can result in long-term delamination of coatings through hygroscopic effects and hydrolytic processes [10].

Therefore, establishing reliability may involve testing for organic, non-conductive, contaminants. This process can be time-consuming, costly, and, unless tests are designed thoughtfully, may provide at best ambiguous results. The goal is to set a baseline for reliability, not to do university research.

The right testing involves partnering with your customers and the testing lab. Here are a few examples of tests that might provide additional information about interfering residue. Since, total residue should often be of concern, sometimes non-volatile residue (NVR) or total organic carbon (TOC) is the way to go. NVR can be particularly useful in that many methods involve gravimetric determination of dissolved materials after separating particles by filtration.

People like Fourier transform infrared spectroscopy (FTIR) as a monitoring method; we see it used in aerospace and in other high-value electronics applications. Sometimes, it is allows us to look at the morphology of particles as well as the level of particles. FTIR can provide a picture of typical organic contamination. You can use FTIR as a monitoring method to provide a profile of organic contamination. FTIR won't provide exact identification of a compound. It will show you a typical picture, and you can often tell if the picture has changed.

FTIR works much like the way police use profiling to narrow down the list of suspects—it's not definitive. There are untold numbers of organic compounds (chemicals containing carbon). Therefore, it's important to find a laboratory with experience in the field of electronics assembly. The lab has to have a library of reference compounds (the equivalent of an electronic book of mug shots of criminals with experience in crimes of concern to you). Further, the lab techs must have experience understanding the limits of the field. Otherwise, you end up with misleading results.

Some groups use high-performance liquid chromatography (HPLC) to separate organic

compounds. In fact, ion chromatography is a variety of HPLC. We've heard HPLC dubbed "high-priced" liquid chromatography, so it has to be used judiciously. A fair amount of method development is needed for new HPLC methods.

Before embarking on a series of costly and perhaps non-definitive tests, check with your customer to find out if they have any particular analytical techniques that they use for initial acceptance and/or monitoring. If they work with an outside laboratory, try to find out which lab they use. Find out if your customer has adopted or modified an industry standard or an EPA method. Before you run any lab tests, determine what those modifications consist of.

Your Suppliers

Analysis is not a substitute for appropriate manufacturing practices. Whatever laboratory tests you choose for acceptance and monitoring, achieving reliability means achieving a reasonable level of cleanliness. This involves starting with clean components. It should also involve starting with a product design that can actually be assembled and cleaned. This should go without saying; however, very often the design is complex out of functional necessity. So, at this point, let's assume that you have determined that you need to do at least some cleaning of the assembly.

To obtain clean components, you'll have to select reliable suppliers and partner with them. You focus on flux as a contaminant; your suppliers may use an assortment of process fluids, including lubricants. Metalworking fluids are complex blends of organic and inorganic compounds. Your suppliers may select process fluids based on economics; the choice may be left in the hands of the purchasing department. In addition, metalworking fluids have been reformulated in response to environmental requirements. The reformulated products are designed to volatilize less than the versions they replaced. They are therefore likely to leave more residue [6]. This residue can be carried forward to your electronics assembly process.

Figure 1: An acid bright dip can lead to blistering after heat exposure. (Photo courtesy of David Hillman, Rockwell Collins)

In some applications, a supplier may use a chemical to make the plated surfaces of the component look shiny. However, the result is not always as pretty as desired; shiny does not necessarily mean clean [2]. Visual flaws due to insufficiently cleaned surfaces may be present when these surfaces experiences the high temperatures associated with reflow (Figure 1).

In addition, attempts at Lean manufacturing by your suppliers along with environmental regulatory constraints on using effective cleaning processes may lead your suppliers to gradually reduce the level of cleaning they perform. They may even eliminate cleaning steps.

One approach to coping with this problem is to clean incoming parts prior to assembly. However, adding a cleaning process is costly and time-consuming. Further, cleaning processes are more effective if they take place immediately after fabrication; cured soils are more difficult to remove. You can't always correct for ineffective cleaning. Here's another approach: Find high-quality suppliers who are concerned with effective cleaning and reliability; reward those suppliers with your business. Write your cleaning requirements into new contracts.

Whatever flux you use, optimizing the soldering process can make a big difference in cleanability. If you are modifying a no-clean process to achieve higher reliability, consider the flux. Some no-clean fluxes can be cleaned; others degrade. Organic acid fluxes are one answer, but not necessarily. OA fluxes can be cleaned with water. However, with densely-populated assemblies having close-spacing, flux residue is more likely to occur. There is a limit to the wettability of water. After a point, the surface tension prevents penetration under closely-spaced components—it's just the molecular nature of water. Additives, including surfactants help, but then you have to remove those additives at the rinse stage. Even after thorough rinsing, there is likely to be at least some flux reside. And residue from OA flux tends to be somewhat more active than other varieties. Active flux residue is not compatible with long-term reliability. Therefore, OA flux may not be the appropriate answer.

"There is a limit to the wettability of water. After a point, the surface tension prevents penetration under closely-spaced components—it's just the molecular nature of water."

Reliable Assembly and Cleaning

So, basically, for high-reliability assemblies, we need a reasonable amount of cleaning, to remove not only flux residue but also an assortment of soils that encompass particles and thin films that are organic, inorganic, or perhaps a mixture. In fact, flux is itself a complex mixture.

Ask assemblers about choices in cleaning processes, and most of them will allude to in-line cleaning and batch cleaning. These terms are industry jargon, and most of us know what they mean for electronics assemblers. For most assemblers, in-line and batch systems are aqueous. Both are spray-in-air. Batch systems, in the jargon of electronics assembly, means systems that look on the outside like a high-end kitchen dishwasher. In well-designed machines, the system has been totally redesigned to provide more effective cleaning forces. Batch systems save space and can be very effective for lower volume applications.

An in-line cleaning system carries assemblies down a conveyor belt and cleans them by spraying with water. Let's consider the wash, rinse, and dry sections. The wash step removes soils from the part and keeps soils from settling back. The rinse step continues the process of soil removal and, since residue of the cleaning chemistry can be considered a soil, it removes the cleaning agent. Recall that the physics of chemistry means that water has limited wettability, so you need to employ temperature, force, and time to have even a chance of penetrating tight spaces. This means that most in-line systems have to operate as slow as 0.5 feet per minute, particularly for closely-spaced components.

As a rule of thumb, if you have the equivalent of less than 5 mil standoff, even with unencumbered components, the cleaning system

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will move at 0.5 feet per minute conveyor belt speed. Try moving a pencil across your desk at 0.5 feet per minute (1/10 inch per second)—it's a bit like watching paint dry. Some suppliers of cleaning equipment explain that you can actually run the system at 1.5 feet per minute; while we try to be optimistic, it is probably more important to achieve reality. Half a foot per minute is reality for many, if not most, high-reliability applications. Drying also takes a fair amount of time, depending on the complexity of the part. So, we're talking about a pretty long conveyor belt—maybe 30 feet or so.

Cleaning Beyond the Jargon

In cleaning high-reliability assemblies, it is often effective to move beyond the jargon of what batch and in-line mean. Some batch systems are designed to monitor process cleanliness, at least in terms of ionics. They clean until the assemblies "pass" an industry standard, or some other standard that has been set. In-line systems may provide additional cleaning action, notably agitation under immersion. This flooding, an immersion approach, promises to avoid some of the problems associated with "line-of-sight" cleaning.

Batch systems can be composed of sequential tanks and chambers for wash, rinse, and dry. There are also single chamber systems designed to use a wide range of aqueous and solvent alternatives. There are solvent cleaning systems, co-solvent cleaning systems, vapor degreasers, enclosed solvent systems.

Ultrasonics is Not a Four-Letter Word

Ultrasonic cleaning, immersion cleaning using high frequency sound, is used in many industries for precision cleaning. It is a very effective technique that allows cleaning under closely-spaced components; it is "surround sound," not line of sight. Historically, ultrasoniphobia is a condition that has afflicted many experts in electronics assemblies. There is a fear that the harmonics created could damage components. Ultrasonics has been distinguished from megasonics, where very high frequencies are used in the line of sight cleaning in wafer fabrication. Increasingly, higher-frequency ultrasonic systems (80KHz to several hundred KHz) have become available. Newer techniques can be used to clean effectively and at the same time to avoid damage [5]. As with many cleaning techniques, ultrasonics must be used with caution; and there is always a balance between removal of soil and modification of the product surface. If you fear ultrasonics for high-reliability products, you should also fear other sources of product damage, such as the high pressure spray used in currently-accepted cleaning systems.

> ***If you fear ultrasonics for high-reliability products, you should also fear other sources of product damage, such as the high pressure spray used in currently-accepted cleaning systems.***

To achieve high reliability electronics assemblies, there has to high reliability cleaning. Achieving high reliability cleaning may involve expanding the types of cleaning agents and cleaning systems under consideration. Resources abound. At least two recently-updated resources are available. One is an industry handbook for electronics assemblies [3]; the other is a two-volume reference book that covers cleaning, equipment, and processes used in high-value manufacturing, including electronics assembly[7]. You Can't do it All

Partnering is one secret to electronics assembly of high-reliability products. Manufacturing is complex; supply chains are complex. Customer requirements can be a mystery. Work with your customers, and with your supply chain [8]. A successful supply chain involves understanding the customer's focus and requirements, defining that focus, and sharing that focus with your suppliers. It involves development of mutually agreed on processes, including cleaning processes. It involves selecting the correct partners for the application at hand [1]. **SMT**

References

1. G. Burnett, "Problem-Solvent Partners," Medical Products Outsourcing Magazine, September 2012.

2. D. Hillman, "Hold My Circuit Board and Watch This! The Consequences of Poor Design and Assembly Decisions for High Performance Electronics," SMTA/IPC Cleaning and Coating Conference, November 2012.

3. IPC, "Guidelines for Cleaning of Printed Boards and Assemblies," ISBN 978-1-61193-004-7, 2011.

4. IPC, "Test Method 650.2.3.28 - Ion Chromatography test method for Ionic Cleanliness,"

5. B. Kanegsberg and E. Kanegsberg, "Ultrasonics vs. Megasonics," CleanRooms Magazine, Semiconductor Supplement, July 2002.

6. B. Kanegsberg and E. Kanegsberg, "Finding the Optimal Analytical Test: Parts 1 and 2," Controlled Environments Magazine, November and December 2010.

7. B. Kanegsberg and E. Kanegsberg, Editors, Handbook for Critical Cleaning, Second Edition, CRC Press, 2011.

8. B. Kanegsberg and E. Kanegsberg, "On the Surface: The Right Surface for Electronics Components," Metal Finishing Magazine, January 2013.

9. G. Naisbitt & A. Naisbitt, "A R.O.S.E. is still at Rose? Ionically, it makes a difference!" Global SMT & Packaging Magazine, April 2013.

10. H Schweigart, "Contamination-Induced Failure of Electronic Assemblies," Chapter 21, Handbook for Critical Cleaning, Applications, Processes, and Controls, (Book 2), CRC Press/ Taylor & Francis Group, 2011, pp. 333–344.

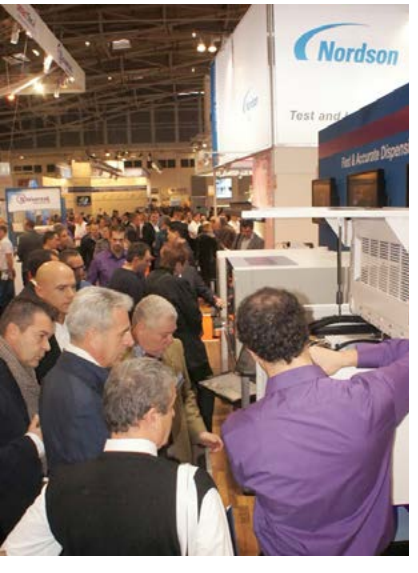
Barbara Kanegsberg is president of BFK Solutions, LLC, and a recognized expert in critical/industrial cleaning and contamination control. As an independent consultant, she develops critical cleaning processes, resolves product-related regulatory issues, and assures that processes meet worker safety and environmental requirements. To contact her, click here.

productronica 2013

by Pete Starkey
I-CONNECT007 TECHNICAL EDITOR

Four November days in Munich—the 20th productronica. More than just an exhibition: an international trade fair for innovative electronics manufacturing. In all, 1,220 companies from 39 countries exhibited their equipment, materials, processes and services to 38,000 visitors from 83 countries.

I haven't missed productronica many times over the last 30 years; I've always seen it as the one event that represents the whole electronics supply chain and offers a glimpse into the future of the industry. It hit an all-time low in 2009, and I recall John Ling's wistful analogy of visiting a much-loved but ailing elderly relative in hospital, and fearing the worst. Two years later, the elderly relative was showing signs of improvement and this year appeared to be recovering to a state



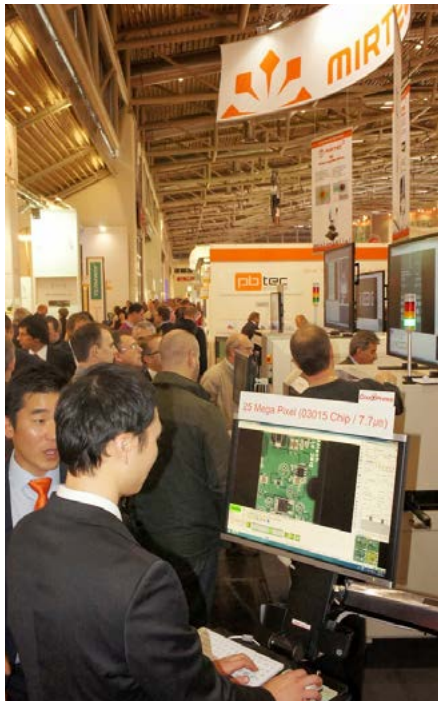
productronica 2013

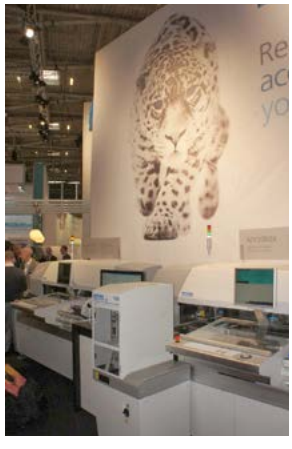
of robust health! The organisers reported a sharp increase in the number of visitors from abroad—especially from non-EU countries, and particularly from the Russian Federation, China and Turkey.

There was a positive energy about the place—plenty of traffic, plenty of activity and real business being done by the exhibitors. No tire-kickers this year, people were not dreaming of what they might have liked to buy if they could have afforded to. They had come with real money to spend, and they were prepared to spend it, albeit selectively in carefully-considered transactions.

Although it is subject to increasing competition from far-Eastern events, productronica is still rated the number one electronics industry gathering in the world. And it didn't snow this time! Interesting to see what 2015 brings…

But for now, enjoy these images from the show! For full Real Time with... video coverage, click here. **SMT**





SMTonline Supplier/New Product News Highlights

Atotech's New Immersion Tin Process for QFN Packages

The Stanna-Q process covers the exposed lead frame copper on the side of the QFN package by immersion tin to form a solder filet during assembly. The product can be applied in vertical-basket, horizontal, and vertical-barrel mode for singulated QFNs.

LPKF Unveils ProtoMat D104

LPKF Laser & Electronics AG presents a spectacular new development: The LPKF ProtoMat D104 unites the best features of advanced LPKF ProtoMats with the high precision of the ProtoLaser systems. The highlight of this product innovation is a special UV laser.

Indium Instructors Support SMTA Recertification Process

Three Indium Corporation experts and SMTA-certified instructors will assist recertification efforts: Dr. Ron Lasky, senior technologist; Ivan Castellanos, technical services manager, Latin America; and David Hu, technical manager, China.

ACD Promotes Tsui to Director of Manufacturing Operations

The company, a leading supplier to the electronics industry, announces the promotion of Tim Tsui to director of manufacturing operations. All assembly operations will now report to Tsui, from supply chain through test. He remains responsible for the development of new processes while maintaining current processes.

E2open Earns ISO 27001 Certification

Information security is of the highest importance today, especially in terms of supply chain management, as it has far-reaching implications for daily business.

Indium Introduces New Lead-free Solder Paste

Tim Jensen, global product manager for PCB assembly products, says "Our customers have been asking for a high-performance solder paste that combines excellent printability with probe-testability. This solder paste delivers on all counts. What this means is that Indium8.9HF1-P will deliver long-term reliability for our customers' end products.

Digicom's Diamond Track Program Assists Medical Industry

Digicom Electronics, Inc. has designed a Diamond Track Program to help medical device companies with their complete process. As part of the program, Digicom performs a design review and collaborates with the device designers to make sure the design is manufacturable and to ensure that the necessary information is available to complete the transition of the design to manufacturing.

Evana Automation to Streamline Manufacturing Process

Evana Automation Specialists, a subsidiary of Phillips Service Industries and leading systems integrator and builder of custom, automated assembly and test systems, has received a contract from a Tier 1 automotive supplier to provide a multi-cell assembly system to simplify the process of manufacturing steering gear sub-assemblies.

Collaboration Forms ITRI-IPC China Solder Technology Group

The key objectives for this new group are to initiate cooperative projects and focus on discovering solder application problems within the electronics industry and to begin to build a solder alloy database, which will provide a platform for research and development.

Dethon Industrie Selects DEK as Printing Partner

Dethon Industrie, a Netherlands-based manufacturer of products for multiple markets including electronics, has chosen DEK as its printing partner, leveraging the advanced technology of the DEK Horizon 03iX print platform as well as the company's full suite of stencils and process support products.

Goodbye to Trial and Error?

by Eric Klaver
ASSEMBLÉON

All the time you spend at the production line for trial-and-error runs, just to get your production board right, takes away from your real production time. It comes on top of the time spent for trial and error at the screen-printer, and any other equipment in the line. All this can take an hour or more for each production board but, with all the tools now available, it can easily be significantly reduced. In addition, though, there are time-consuming actions (like loading all the feeders) to get right before the first error-free board comes out of the machine.

So, how do you minimize the whole trial-and-error process to ensure that, when a program starts up and feeders and toolbits are already on the system, the first board coming out of the machine is immediately good?

A perfect first board would mean that the correct components were all picked from the correct feeder and placed on the correct location at the correct placement angle. Guaranteeing this means ensuring that all the many pre-defined variables are correct: enough paste, exact board positioning, precise artwork, correct components picked by the correct toolbits and placed exactly. The more variables that are incorrect, the longer the ramp-up will take. The more programs each shift that require correcting, the shorter your effective production time and thus fewer boards produced. And during ramp-up, it's better that the system stops to signal a fault than finding it out at the end during board test. It also helps save ramp-up time if all components are actually picked to get the program started immediately without false starts.

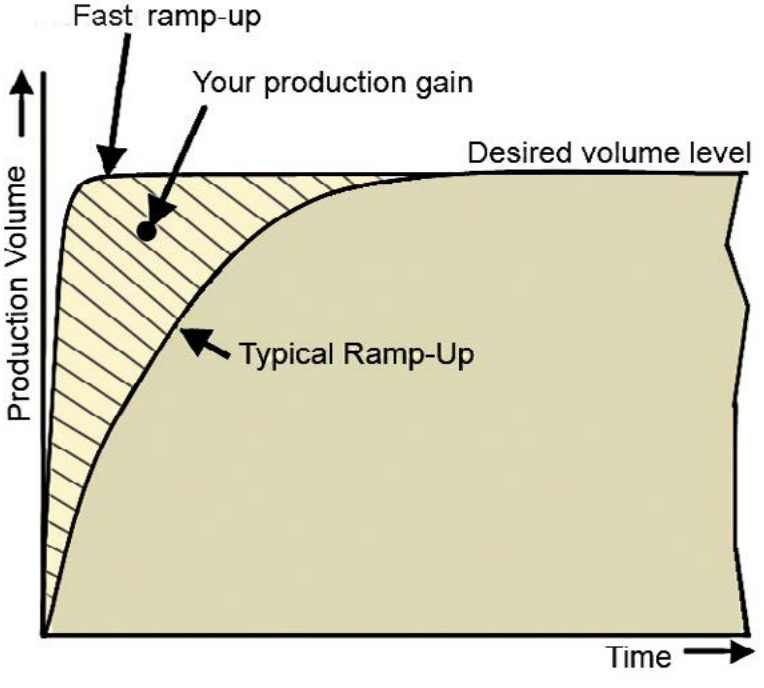


Figure 1: Fast ramp-up adds to production levels, particularly for high-mix production.

Software Helps Improve Ramp-Up

For the pick-and-place equipment, software plays an important role in improving the equipment's ramp-up time.

Teaching a PCB at the machine is time-consuming and error-prone, and starting from good CAD data is a solid basis for quality manufacturing. The same goes for defining the shapes and sizes of new components, which is also very consuming and not something you want to repeat too often. A good data preparation program should have an option like virtual sticky tape, which maps the parts onto the PCB and can immediately be checked for exact location as defined by the CAD data. Polarity and placement angle, pick angle, pocket orientation and packaging type can be checked at the same time.

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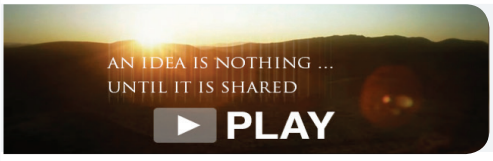

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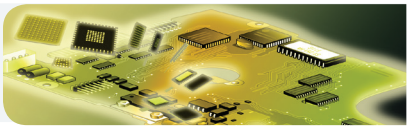

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GOODBYE TO TRIAL AND ERROR? *continues*

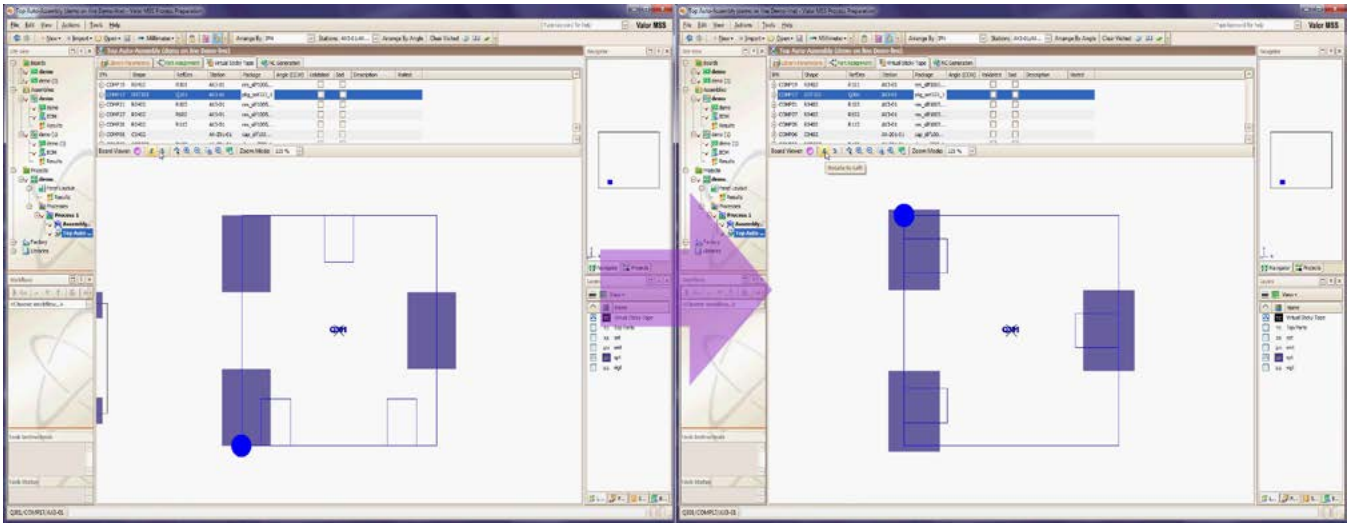


Figure 2: Tools, such as virtual sticky tape, check on correct shape, polarization and placement angle.

Going through the placement program line by line helps correct any deviations immediately. Then, placements exactly match the PCB layout defined by CAD, filtering out any possible mistakes or offsets. Depending on the number of unknown new components, subscriptions to large shape libraries can save considerable work in entering all the component data into local libraries. If not, software should ensure that, once programmed, shape data on an offline tool or at a machine should be fed back to the data preparation program, preferably via a library manager that controls and releases parts. That way, the work doesn't have to be repeated and you are sure that the data is correct.

Data that can be re-used 100% reduces ramp-up time significantly. So, doing new product introductions on a line similar in setup and machine type to the volume production allows all the data (program, process, shapes, and supply forms) to be re-used without alteration. Factory programs can help this by having processes in place for version control, authorization and release. And if you can co-ordinate all the software versions on your equipment to make the outcome of your processes the same, you can save a lot more time. So it is always good to have compatible software or firmware versions for all your equipment.

Once a verified program is sent to the equipment, the next action is to ensure correct setup of feeders, support pins and nozzles. Setup verification can ensure that feeders with the correct parts are available to the system, whether or not they are at optimum locations. Software should also be able to change over to second-source components without halting ramp up. Printed or digital lists should always include visual checks on package type and the orientation of the part in its package.

If the setup is verified and the components are good, software routines can ensure that there is indeed a first component at the pickup position and that the pick is made exactly in the center of the pocket. In general this is not necessary, but for the smallest (or pick-critical) components the total tolerance train of the tape and feeder can cause pick errors to hamper ramp-up or actual placement quality. So, start-up routines need to check and verify the correct pick location of critical components and check that a component is actually in the pocket. At the end the rule is "the basis for a perfect placement starts at a perfect pick."

Manual pin setup can be accomplished faster if done offline or by automating it with automatic placement. Flexible board support systems can give near-zero support setup times and fewer errors when placing components on the first run. The more nozzles that are used, the more chance there is of error. Minimizing the number of nozzles used, and including nozzle

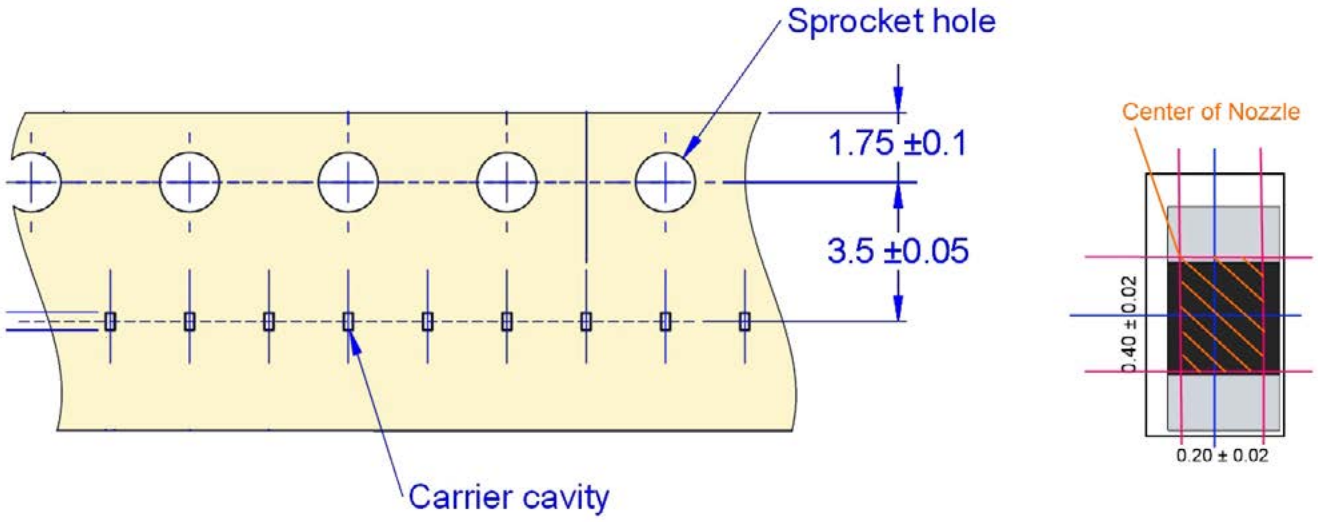


Figure 3: Worst-case tape tolerances may cause a too large off-centered pickup.

verification marks, ensures that only the correct nozzles are on board and that the right ones are used immediately.

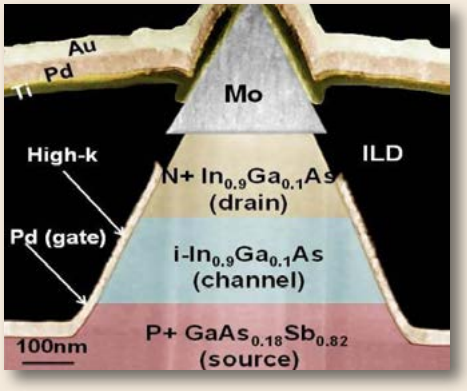
And if the CAD data did actually match your board layout and the initial parameters have been correctly set, then you will produce the first boards' right first time. Over a year, that will save many hours of production ramp-up time and correspondingly increase your actual production time. **SMT**

Eric Klaver has been with Assembléon since 1998. He specializes in vision technology and feeding, and is currently chairman of the IEC work group TC-40WG36, which specializes in component packaging. To read past columns, or to contact him, click here.

New Transistor for Low-power, High-performance Devices

A new type of transistor for fast and low-power computing devices for energy-constrained applications such as smart sensor networks, implantable medical electronics and ultra-mobile computing is feasible, according to Penn State researchers. Called a near broken-gap tunnel field effect transistor (TFET), the new device uses quantum mechanical tunneling of electrons through an ultrathin energy barrier to provide high current at low voltage.

Penn State, the National Institute of Standards and Technology and IQE, a specialty wafer manufacturer, jointly presented their findings at the International Electron Devices Meeting in Washington, D.C. The IEDM meeting includes representatives from all of the major chip companies and is the recognized forum for reporting breakthroughs in semiconductor and electronic technologies.



Tunnel field effect transistors are considered to be a potential replacement for current CMOS transistors, as device makers search for a way to continue shrinking the size of transistors and packing more transistors into a given area. The main challenge facing current chip technology is that as size decreases, the power required to operate transistors does not decrease in step. The results can be seen in batteries that drain faster and increasing heat dissipation that can damage delicate electronic circuits. Various new types of transistor architecture using materials other than the standard silicon are being studied to overcome the power consumption challenge.

SMTonline Market News Highlights

November Manufacturing PMI Registers 57.3%

"The PMI™ registered 57.3%, an increase of 0.9% from October's reading of 56.4%. The PMI™ has increased progressively each month since June, with November's reading reflecting the highest PMI™ in 2013. The New Orders Index increased in November by 3% to 63.6%, and the Production Index increased by 2% to 62.8%."

Survey Reveals Technology Investment Predictions

"CFOs continue to seek out technology which allows them to improve business performance and increase employee productivity," said Jay Cary, VP, Digital, Global Corporate Payments at American Express. "Mobile in particular is leading the way—both because of CFOs' familiarity with the technology and for the real-time benefits it offers employees."

Reliability Hinders Printed Electronics Market Growth

The major barrier inhibiting the growth of the market, currently, is the reliability of the end products (printed electronics), and it is expected that this issue will be overcome by the advancement in the functional printing technology.

Medical Automation Market to Hit $66 Million by 2018

Automated monitoring devices help reduce rising healthcare costs, the major factor driving the growth of this market. Furthermore, growth in the use of point-of-care testing devices such as glucose meters, digital blood pressure monitors, pregnancy test kits, and HIV test kits is another factor that is propelling the market.

Total Personal Computing Systems to See 11% Growth

IC Insights forecasts total personal computing unit shipments (desktop PCs, notebooks, tablets, and Internet/cloud portables) to grow an average of 10.6% from 2012 to 2017, reaching 770 million systems at the end of the forecast period.

Global Chip on Board LED Market to See CAGR of 40.71

One of the key factors contributing to this market growth is the declining ASP of LEDs. The global chip-on-board LED market has also been witnessing the increasing demand of COB LED in general lighting applications.

Functional Printing Market to Reach $13.79B by 2020

The demand for a new variety of low-cost electronic products, made possible by a range of printing techniques and materials, has pushed the demand for "functional printing" across geographies.

Conductive Ink Markets to Reach $3.36B in 2018

Conductive inks are a simple and unglamorous layer, but they will constitute a hefty $2.86 billion market in 2012. This market is forecasted to rise to $3.36 billion in 2018, with $735 million captured by new silver and copper nanostructure inks.

Consumer Confidence Continues to Drop in November

The Conference Board Consumer Confidence Index, which had decreased sharply in October, declined again in November. The Index now stands at 70.4 (1985=100), down from 72.4 in October.

Semiconductor Sales Recover in 2013; Up 4.9% YoY

Following a 2.5% decline in 2012, the global semiconductor market has regained its footing in 2013 with revenue set to expand by nearly 5% because of the strong performance of the memory sector.

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SMTA International
Abstract Deadline: **February 28,**
Sept 28 – Oct 2, 2014
Rosemont, IL
*Paper required

Counterfeit Electronic Parts and Electronic Supply Chain Symposium
Abstract Deadline: **March 7th**
June 24 - 26
College Park, MD
*Presentation Only

IWLPC – Int'l Wafer-Level Packaging Conference
Abstract Deadline: **May 2nd**
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San Jose, CA
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A SHORT SCOOP

Electroformed Stencils

by Rachel Short
PHOTO STENCIL

The continued drive in electronics to place increasingly smaller components on boards poses continuing challenges to board manufacturers. Tight pad spacing as well as placement of small 0201 and 01005 components is becoming more commonplace on board assemblies. Not only are the parts nearly invisible when placed, but their small size causes challenges with the solder paste application and release needed to yield reproducible, low-defect solder joints. The short scoop this month is that you can meet the challenges of paste application for difficult assembly printing processes by using electroformed stencils.

It may seem that a stencil is a rather simple device; after all, in its basic form it is just a sheet of metal stretched taught with hole patterns placed in it to allow application of solder paste in the open areas. The stencil and its fabrication have a great influence over the ability of the circuit board assembly manufacturer to reliably reproduce the desired depositions necessary for paste application.

Stencils can be laser cut with or without post-processing, which for many applications is sufficient to get the paste application process completed reliably. Both of these fabrication techniques are currently employed in main-

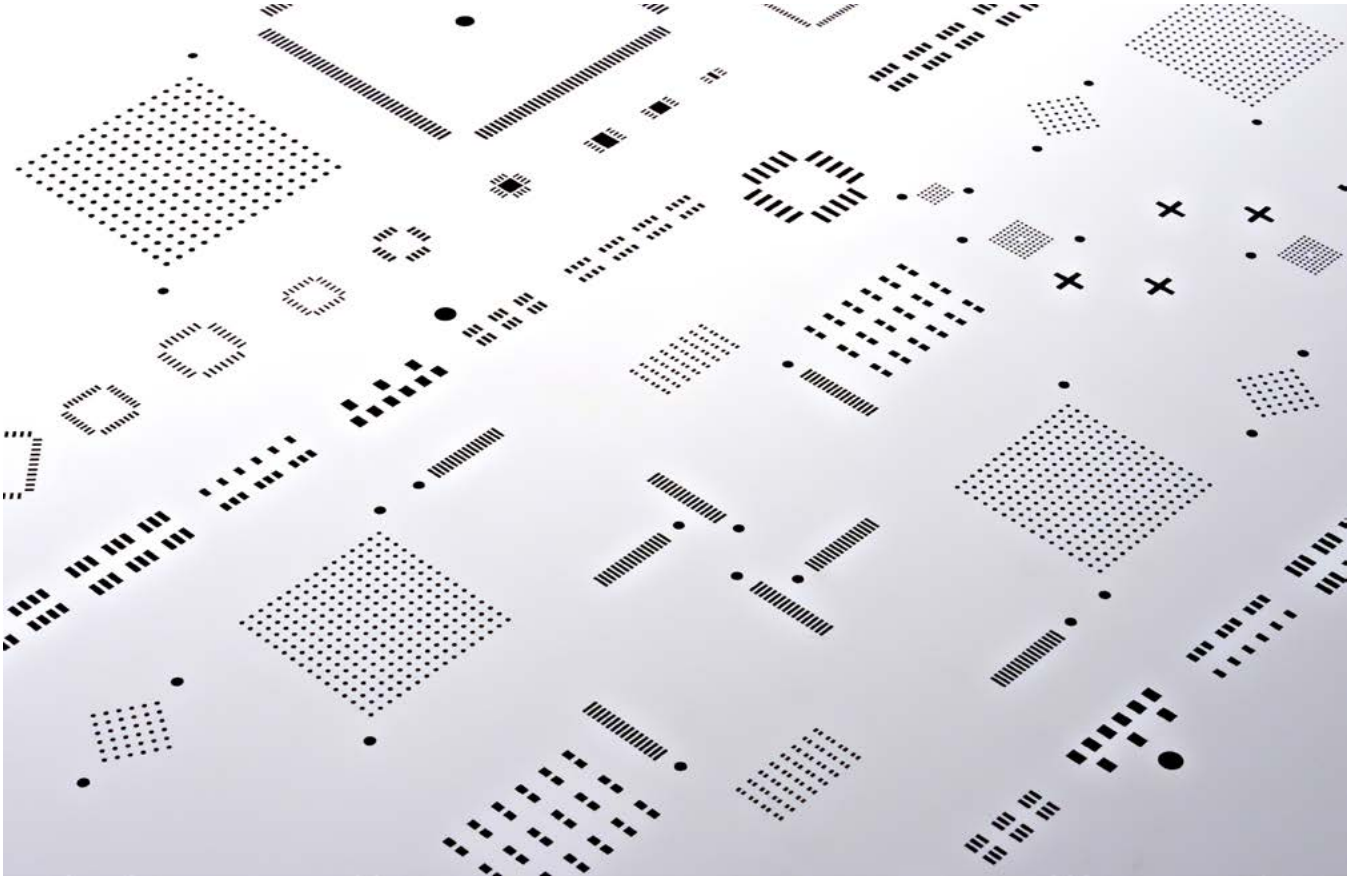

Figure 1: Standard electroformed stencil image.

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ELECTROFORMED STENCILS *continues*

stream stencil production, but they both start to exhibit their limitations as pattern features decrease in size. The roughness of the stencil wall is one of the major influences on how well paste will release from the stencil. The rougher the sidewall of the aperture, the more the paste is prone to sticking onto the edge of the wall. The apertures used with larger pad features are somewhat more tolerant to edge roughness due to usually higher area ratios. As the pattern features decrease in size, the amount of paste that does not release due to a rough edge becomes an increasingly larger portion of the target application volume. So as feature size decreases, the fabrication of the stencil needs to be constructed for enhanced release capability.

One handy predictor of the stencil's ability to effectively transfer solder paste is the area ratio. The area ratio is defined as the area of the aperture opening divided by the area of the aperture side walls. It was discovered that for smaller area ratios, the smoothness of the nickel electroformed stencil walls provide superior paste transfer; and, area ratios down to .50 with uncoated electroformed stencils could be achieved where conventional stencils use a guideline of a minimum of 66. With additional release coatings applied to the stencil, area ratios as low as .43 are achievable.

Creating the stencil through the electroforming process has the advantage of keeping the inside release edge of the stencil perfectly smooth. Where other stencil types create the aperture by removing stencil material through processes like chemical etching or laser cutting, electroformed stencils are created through an additive process, building up material thickness atom by atom. Once a stencil design is finalized, a negative image of the stencil pattern is transferred onto a mandrel as a plating resist. The mandrel is then connected into a plating circuit and placed into electrically charged nickel baths where it will be left to slowly grow to the desired thickness. Any metal surface exposed directly to the bath will build up material thickness; however, areas where the resist is applied to the mandrel are not electrically connected to the circuit through the plating bath so growth in these areas is inhibited. The plating obstructions caused by the application of the resist negative are the features that determine the aperture characteristics that form around it as the electroformed stencil is grown. Since the plating resist pillars can be created with extremely smooth edges, the electroformed stencil that builds up around the resist takes on the wall characteristic of the perfectly smooth resist plating obstruction as it is grown.

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While electroforming produces an extremely smooth release edge, it is a significantly more time-consuming process to create a stencil using this method. Unlike stencils produced by removing material which can be fabricated in a few hours, the electroformed stencil is left in the plating bath for many hours to slowly grow to the desired thickness. Because of the processing involved, these stencils inherently require a slightly longer lead time to produce and are typically more costly than other stencil technologies. While they have beneficial qualities when used with larger components, they truly show their advantages when used with today's small format parts.

Electroformed stencils have been around for quite some time. Initially a patented Xerox process, Photo Stencil purchased the patent and developed the process in the mid-'90s and has been making them since. While initial applications were more limited, the ever-con-

tinuing trend towards miniaturization of electronics has made electroforming fabrication technology much more popular for electronics production.

Electroformed stencils have become much more of a necessity as pitches and components become smaller. They are typically used for active component pitches below 20 mils, for 0201 and 01005 chip component applications such as SMT, µBGAs, flip chip, and also for wafer bumping (12 mil to 6 mil pitch). These stencils are strongly recommended for projects exceeding 10,000 apertures, since the additional stencil cost verses potential defects related to printing and subsequent rework cost become negligible.

The most common thicknesses for electroformed stencils are 2, 3, 4 and 5 mils, but they are not limited to a specific thickness. Electroformed stencils can be tailored to specific thickness requirements and can be ordered in 0.1 mil increments for further refinement of solder paste deposits for use in demanding applications.

While this Short Scoop has focused on fine-pitch applications and the need for high-quality stencils, special 3D electroform stencils can also be fabricated for other needs. If resist is stripped and reapplied as a secondary pattern, selected areas of the stencil can be grown in excess of the initial electroforming through a secondary application of the same basic process. These 3D stencils can be an excellent solution for odd PCBs that have raised areas on the board (up to 0.120" high).

With stencils, it all boils down to choosing the right tool for the application. While electroformed stencils are not required for all applications, they do afford the user a tool that will reliably perform over time. **SMT**

Rachel Short is vice president of sales and marketing at Photo Stencil LLC. She may be contacted here, or by phone at 719-304-4224. To read past columns, click here.

TOP TEN

News Highlights from SMTonline this Month

1 Clarke and Delaney Join Sanmina's Board of Directors

Sanmina Corporation, a leading integrated manufacturing solutions company making some of the world's most complex and innovative optical, electronic and mechanical products, announces the appointment of Michael J. Clarke and Eugene A. Delaney to the company's Board of Directors, effective December 9, 2013.

2 Creation's Wisconsin Facility Earns FDA Registration

"FDA registration is a key supplement to the ISO 13485 certification we have in 12 of our business units, including here in Milwaukee," said Dan Dery, general manager. "It was a logical extension of existing capabilities given our history of delivering regulatory success to our customer base."

3 IPC APEX EXPO 2014 to Feature Swarm Robotics Tech

Roboticist and inventor James McLurkin will share his research and insights into the future of multi-robot systems or "swarm robotics" during his keynote session at IPC APEX EXPO 2014 on Wednesday, March 26, in Las Vegas, Nevada.

4 Imergy, Flextronics Partner on Energy Storage Solutions

The partnership, the first step in a new global expansion strategy for Imergy Power, will help the company accelerate its product pipeline, develop and market a wider variety of products, and lower overall costs. The first product from the collaboration will be a 5 kilowatt/30 kilowatt hour system for telecom, hybrid, and residential applications.

5 OnCore Launches Interconnect Business

"We have assembled an engineering and operations team with an average of 18 years of cable and harness manufacturing experience," commented Bob Weber, vice president of manufacturing. "OnCore Interconnect fulfills our customers' requirements for a high-quality interconnect source that is integrated into their product's manufacture."

6 Winchester Electronics Completes Acquisition of Haverhill

Winchester Electronics Corporation, a portfolio company of Audax Private Equity, has completed the acquisition of Haverhill Cable and Manufacturing, Corporation.

7 Nortech's Degen Retires as CEO; Wasielewski Takes Over

In a planned transition, Nortech Systems Incorporated has announced that Michael J. Degen will retire as CEI on January 1, 2014, and become executive chairman of Nortech's board.

8 Axis Electronics Earns National Recycling Gold Accreditation

Axis Electronics is pleased to announce that E2B pulse, the UK Carbon Reduction Network has awarded Axis Electronics a National Recycling Gold Accreditation.

9 Foxconn Opens New R&D, Testing Center in Nanning, China

Foxconn, world's leading manufacturer of computer components and systems, hosted an opening ceremony for its R&D and testing center in Nanning, China. The new R&D center will feature several labs for experiments such as reliability, failure analysis, and electromagnetic compatibility testing, as well as a cloud computing datacenter.

10 CTS Adds Three Executives to Senior Leadership Team

CTS Corporation has appointed three new leaders to its senior leadership team: Ashish Agrawal as VP and chief financial officer, Anthony Urban as VP and general manager of CTS' Sensors and Mechatronics business, and Robert J. Patton as VP, general counsel and secretary.

EVENTS

For the IPC's Calendar of Events, click here.

For the SMTA Calendar of Events, click here.

For the iNEMI Calendar, click here.

For a complete listing, check out *SMT Magazine's* full events calendar here.

International Electronic Components Trade Show
January 15–17, 2014
Tokyo, Japan

Microtech Japan
January 15–17, 2014
Tokyo, Japan

Electrotest Japan
January 15–17, 2014
Tokyo, Japan

Material Japan
January 15–17, 2014
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NEPCON Japan
January 15–17, 2014
Tokyo, Japan

PWB Expo
January 15–17, 2014
Tokyo, Japan

15th IC Packaging Expo
January 15–17, 2014
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Tokyo, Japan

EV Japan
January 15–17, 2014
Tokyo, Japan

DesignCon 2014
January 29–30, 2014
Santa Clara, California, USA

SPIE Electronic Imaging
February 2–6, 2014
San Francisco, California, USA

Pan Pacific Microelectronics Symposium
February 11–13, 2014
The Big Island, Hawaii, USA

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AD DESIGN: **SHELLY STEIN, MIKE RADOGNA**
INNOVATIVE TECHNOLOGY: **BRYSON MATTIES**
COVER ART: **BRYSON MATTIES AND SHELLY STEIN**

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SMT® (Surface Mount Technology) is published by BR Publishing, Inc., PO Box 50, Seaside, OR 97138

January 2014, Volume 29, Number 1 • SMT© (Surface Mount Technology©) is published monthly, by BR Publishing, Inc.

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Don't miss our upcoming issues!

- **February:** SMT Assembly, Part 1: Preparation for Soldering
- **March:** SMT Assembly, Part 2: Making the Connections
- **April:** SMT Assembly, Part 3: After the Soldering Process

Interested in being a contributor to *SMT Magazine?* Drop us a note here!

See you next month!