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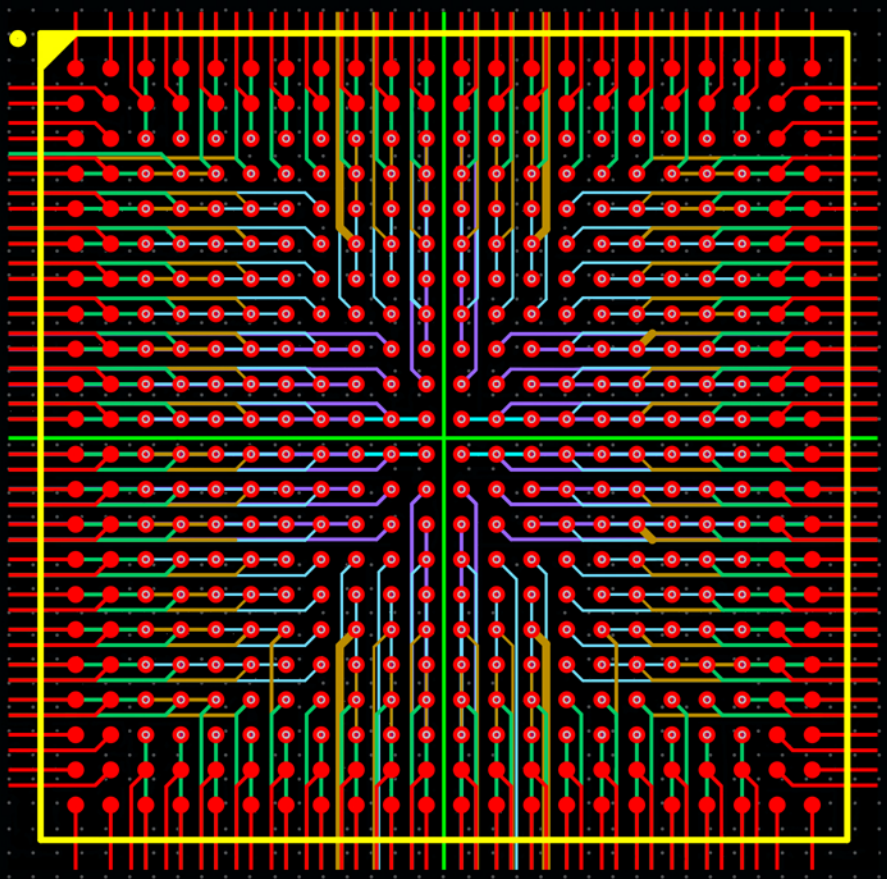

the ADVANCED future

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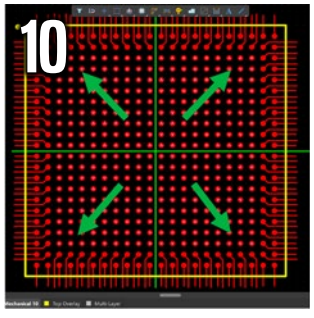
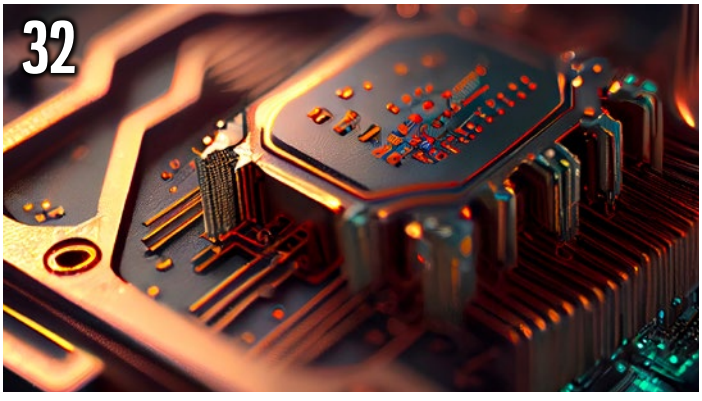
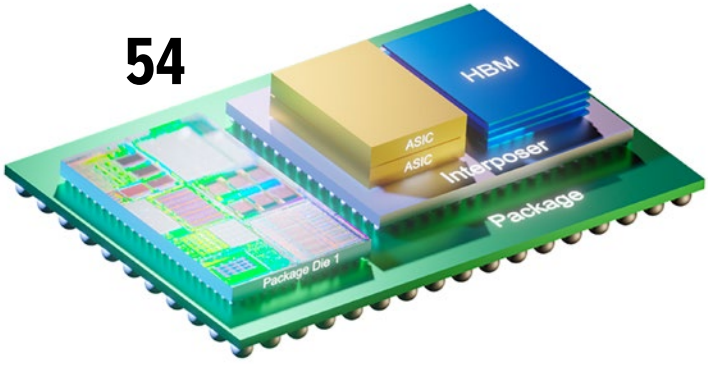
The Advanced Future

The year 2022 might be remembered as the Year of Advanced Packaging. The Department of Defense got the ball rolling last summer with the CHIPS Act, and the IPC Advanced Packaging Symposium helped outline the hurdles we're facing with complex packaging. In this issue a variety of experts discuss the challenges and trade-offs that PCB designers and design engineers are seeing today with advanced packages.







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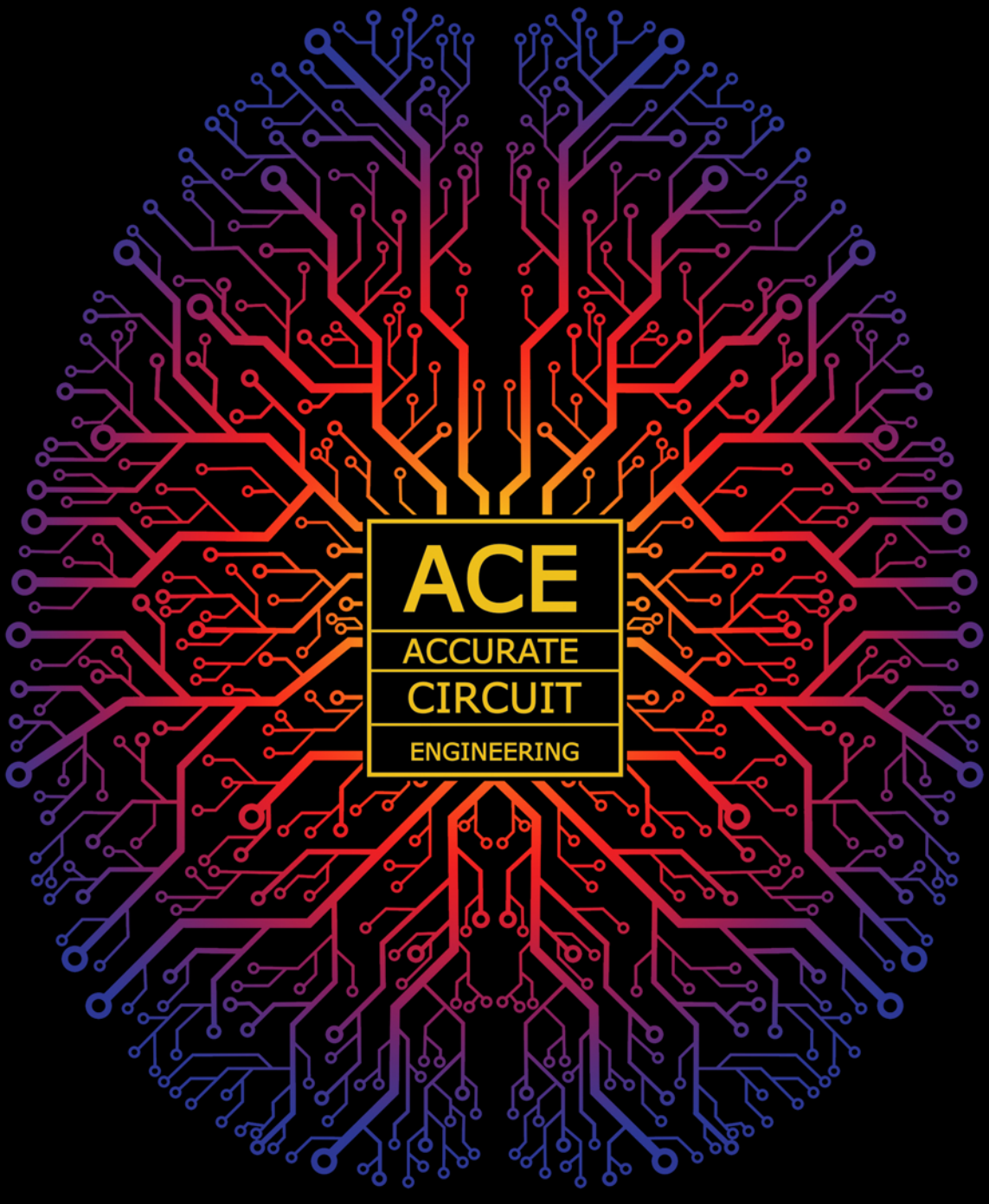

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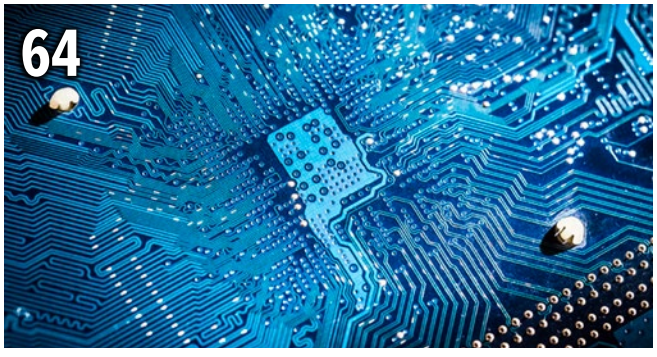

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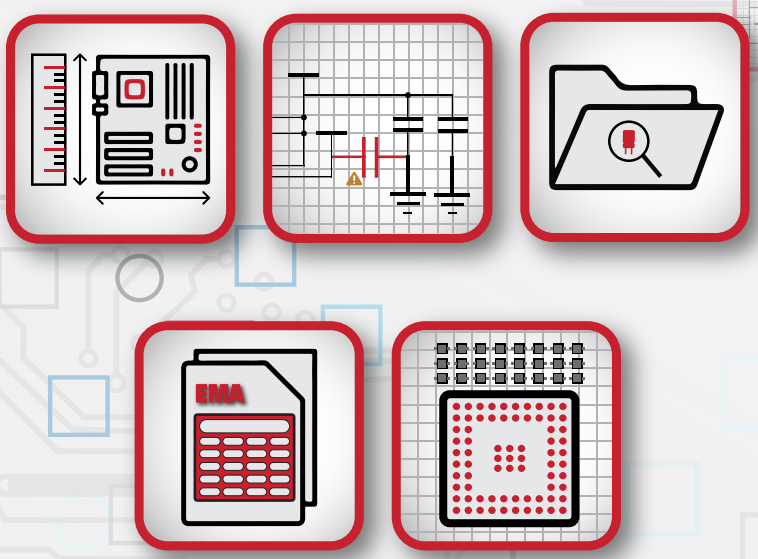

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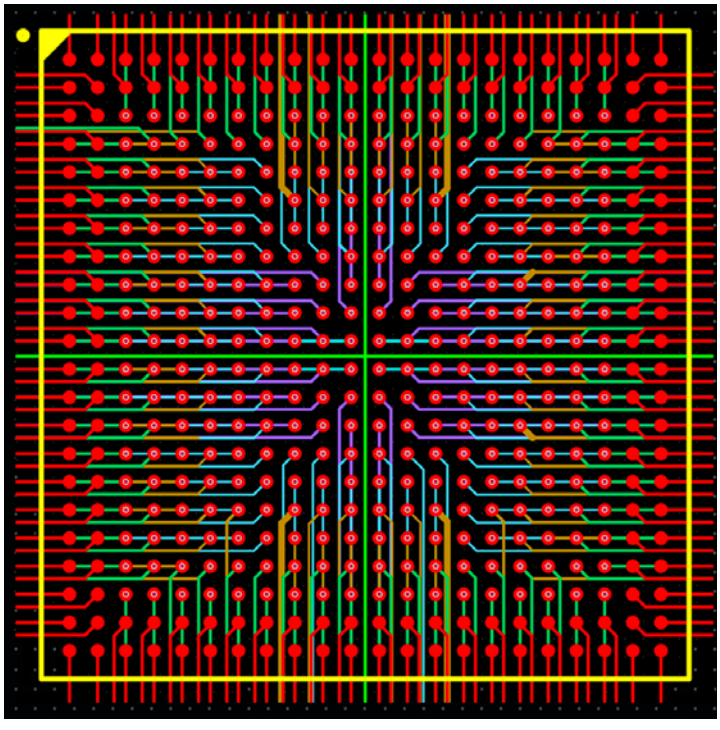
PCB Design and Advanced Packaging

The Shaughnessy Report

by Andy Shaughnessy, I-CONNECT007

It's hardly an exaggeration to say that 2022 might be remembered as the Year of Advanced Packaging. The Department of Defense got the ball rolling last summer with the CHIPS Act, which pointed out how far the United States has fallen behind the rest of the world in microelectronics. A few months later, the week-long IPC Advanced Packaging Symposium took place in Washington, D.C., and I-Connect007 covered this event from start to finish.



Among the things we learned from the symposium: There's a great deal of innovation taking place in advanced packaging now, and it all starts with PCB designers and design engineers making the correct decisions early in the design cycle.

When we started planning this issue, we wondered: What exactly do we mean by the term advanced packaging? IPC's Kris Moyer teaches a PCB design course on this topic, and he was kind enough to provide us with a two-pronged definition of advanced packaging:

"The first definition is with respect to IC packages. For this, advanced packaging refers to the interposer boards that are made with advanced specialty materials, typically non-FR-4, along with advanced special manufacturing techniques and methodologies.

"The second is with respect to system/product design. For this, advanced packaging is a description of any advanced techniques and methodologies used in the design of PCBs for non-standard products. These include sequential lamination and microvias used in HDI/fine-pitch products, chip-on-board/chip-on-flex, direct wire-bond of bare silicon die to the board, non-standard board geometry, extreme reduction in board area, non-standard board mounting, etc." —Kris Moyer

Yes, even the definition of advanced packaging is, well, advanced. Every step of the design cycle is a potential trade-off that must be managed when working with non-standard PCBs. As we'll see with this month's features, the needs of the PCB designers and the designers of chips and packages are beginning to converge, and PCB designers now find themselves learning about chiplets and 3D-IC technologies. Will PCB designers of the future be experts at silicon interposer design?

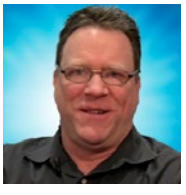
We asked a variety of experts to discuss the challenges and opportunities that PCB designers and design engineers are seeing today with advanced packages, as well as trade-offs.

This issue leads with an article by Kris Moyer, who focuses on the routing techniques necessitated by advanced packaging. Next, Lee Ritchey discusses a challenge that's facing aerospace PCB designers who use stacked microvias, and he offers a variety of methods for circumventing this problem, including using staggered microvias. Columnist Tim Haag shares his take on designing complex packaging, and he tracks how complicated some designs have become over the past few decades.

Ashutosh Mauskar breaks down the nearly "perfect storm" of drivers affecting the semiconductor industry and packaging trends, including supply chain issues, artificial intelligence, EVs and autonomous vehicles. And columnist John Watson explains why packaging is likely to continue shrinking and pushing Moore's Law to its limits: "We are simply running out of room."

We have columns from our regular contributors Barry Olney, Matt Stevenson, Joe Fjelstad, Anaya Vardya, and Saskia Hogan, as well as an article from Zachariah Peterson and an interview with Ventec's Alun Morgan and Mark Goodwin.

I hope you all had a great New Year's cel-ebration, and that 2023 is better than 2022. We'll be covering IPC APEX EXPO and DesignCon soon. I look forward to seeing you on the road. **DESIGN007**



Andy Shaughnessy is managing editor of *Design007 Magazine*. He has been covering PCB design for 23 years. To read past columns, click here.

Feature Article by Kris Moyer
IPC INTERNATIONAL

In today's ever-shrinking world of electronics designs, the use of BGA parts with very fine pitch features is becoming more prevalent. As these fine-pitch BGAs continue to increase in complexity and user I/O (number of balls), the difficulty of finding escape routes and fan-out patterns increases. Additionally, with the shrinking of silicon geometry leading to both smaller channel length and increased signal integrity issues, some of the traditional BGA escape routing techniques will require a revisit and/or adjustment to allow for not only successful fan-out, but also successful functioning of the circuitry of the BGA design.

Historically, BGAs could be routed using traditional full through-via structures, with dog-bone traces off the BGA pad. These BGAs were typically 1.27 mm in pitch and had sufficient clearance between the pads to place a Class 3 Level A via without violating any design rules. Additionally, the feature sizes of these packages were sufficient to fabricate in 1-ounce copper without any issues. With increases in chip complexity and I/O density, most BGA packages are now 1 mm or smaller pitch, with some packages as small as 0.4 mm pitch. With these finer pitch packages, it is no longer possible to use traditional full-thru via structures under the BGA. This, in turn, will require the use of sequential lamination and micro-via structures in order to successfully escape route the BGA. Figure 1 shows a comparison

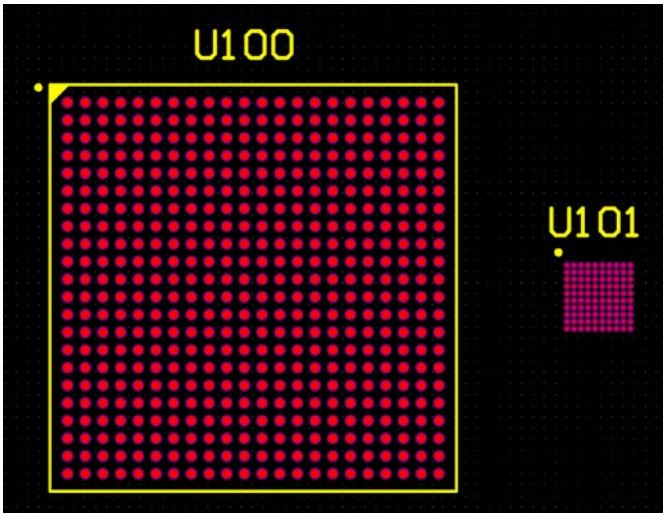


Figure 1: Comparison between the package and feature sizes of a 484-ball 1 mm pitch BGA (U100) and a 100-ball 0.4 mm pitch BGA (U101).

PCBs are complex products which demand a significant amount of time, knowledge and effort to become reliable. As it should be, because they are used in products that we all rely on in our daily life. And we expect them to work. But how do they become reliable? And what determines reliability? Is it the copper thickness, or the IPC Class that decides?

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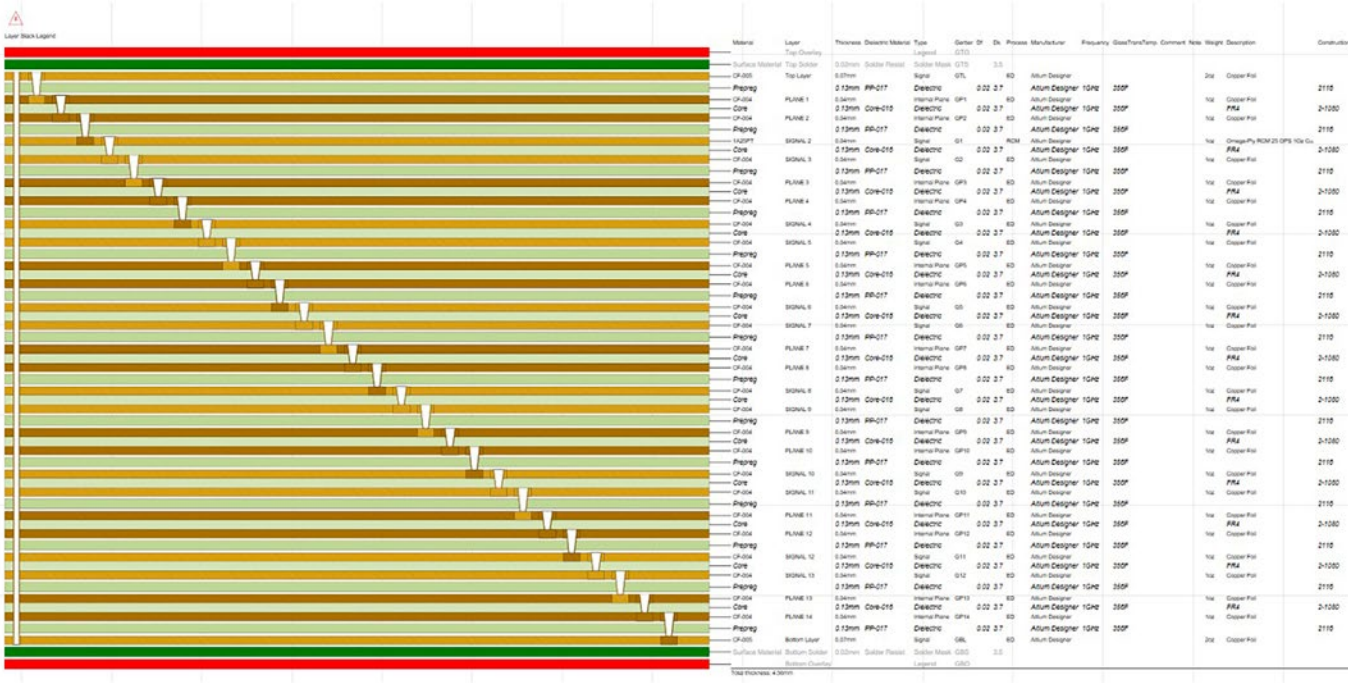

Figure 2: A structure with every layer of a 28-layer board constructed as an HDI layer. This is not possible with today's fabrication processes.

between the package and feature sizes of 484-ball 1 mm pitch BGA (U100) and a 100-ball 0.4 mm pitch BGA (U101).

First, we look at the 1 mm pitch part, then evaluate what it will take to escape all balls to the outside perimeter of the BGA. For this evaluation, we will only consider the use of stacked microvias. Staggered microvias will also work, but require significantly more board area. Additionally, the stackup will assume dual stripline for all internal signal layers.

The first challenge in routing the BGA is to define how many HDI (sequential lamination/microvia) layers will be needed. Figure 2 shows a structure with every layer of a 28-layer board as an HDI layer. This, however, is not producible with current HDI fabrication techniques—more on this later.

The basic technique to escape route the BGA is the quadrant method. With this method, we will divide the BGA into four quadrants and then use a standard pattern in each quadrant. Figure 3 shows the basic quadrant pattern.

Once the quadrants are defined, we will route the BGA in two-row patterns. The outside-most rows will be routed straight. The inside row will be routed in the direction of the quadrant, and then straight. Here the two outer-most rows will route on the top layer.

The next two rows will route on the first internal signal layer, and so on. Figures 4 and 5 show the routing of first internal signal layer.

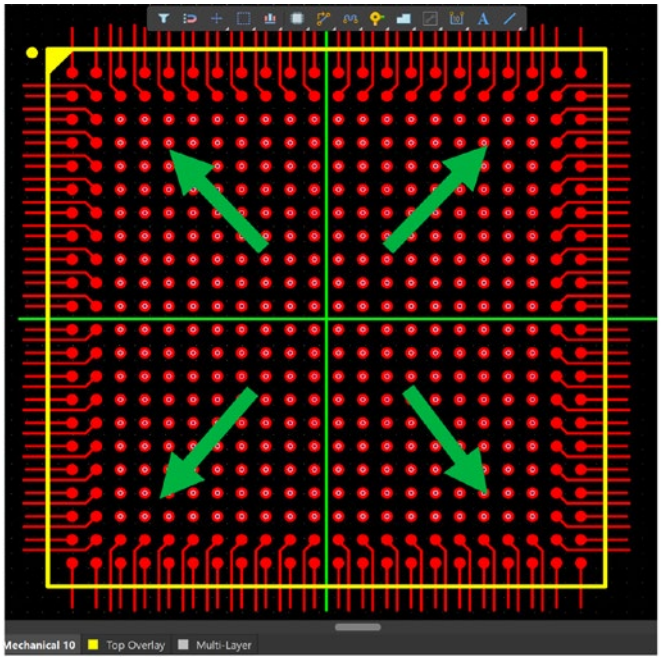

Figure 3: A quadrant pattern used to escape route a BGA.

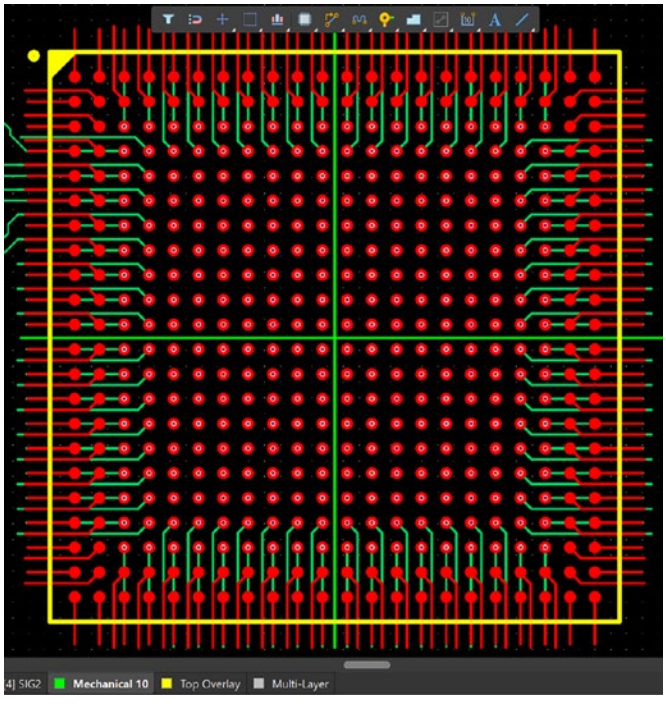

Figure 4: Routing of the first internal signal layer.

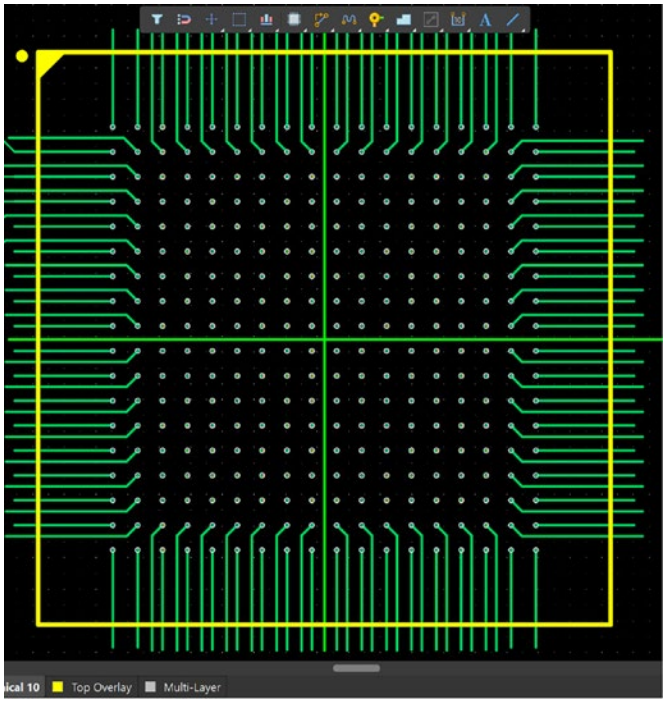

Figure 5: Routing of the first internal layer, continued.

Board Layer Stack | + Add | Modify | Delete

#	Name	Material	Type	Weight	Thickness	Dk	Df
	Top Overlay		Overlay				
	Top Solder	Solder Resist	Solder Mask		0.8mil	3.5	
1	Top Layer	CF-005	Signal	2oz	2.756mil		
	Dielectric 13	PP-017	Prepreg		5.1mil	3.7	0.02
2	PLANE1	CF-004	Plane	1oz	1.378mil		
	Dielectric 14	Core-016	Core		5mil	3.7	0.02
3	PLANE2	CF-004	Plane	1oz	1.378mil		
	Dielectric1	PP-017	Prepreg		5.1mil	3.7	0.02
4	SIG2	CF-004	Signal	1oz	1.378mil		
	Dielectric 15	Core-016	Core		5mil	3.7	0.02
5	SIG3	CF-004	Signal	1oz	1.378mil		
	Dielectric 16	PP-017	Prepreg		5.1mil	3.7	0.02
6	PLANE3	CF-004	Plane	1oz	1.378mil		
	Dielectric 17	Core-016	Core		5mil	3.7	0.02
7	PLANE4	CF-004	Plane	1oz	1.378mil		
	Dielectric 18	PP-017	Prepreg		5.1mil	3.7	0.02
8	SIG4	CF-004	Signal	1oz	1.378mil		
	Dielectric 19	Core-016	Core		5mil	3.7	0.02
9	SIG5	CF-004	Signal	1oz	1.378mil		
	Dielectric2	PP-017	Prepreg		5.1mil	3.7	0.02
10	PLANE5	CF-004	Plane	1oz	1.378mil		
	Dielectric 3	Core-016	Core		5mil	3.7	0.02
11	PLANE6	CF-004	Plane	1oz	1.378mil		
	Dielectric4	PP-017	Prepreg		5.1mil	3.7	0.02
12	SIG6	CF-004	Signal	1oz	1.378mil		
	Dielectric5	Core-016	Core		5mil	3.7	0.02

Stackup | Impedance | Via Types

Figure 6: The first 12 layers of this sequence.

At this stage, it should be pointed out that the stackup being employed is one that is proper from a signal integrity point of view (more on SI later). Figure 6 shows the first 12 layers of the sequence. In this figure you see that you need three microvia transitions to transition from

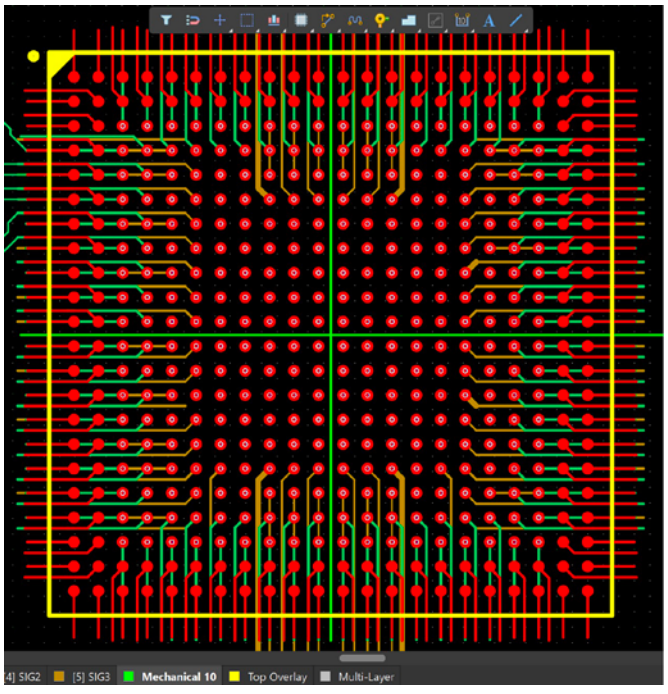

Figure 7: Screen shot of another step in the sequence.

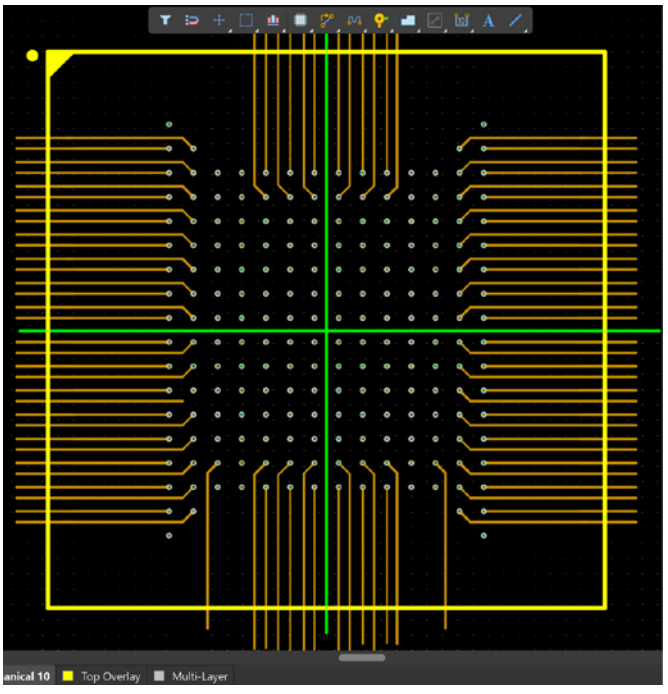

Figure 8: Escape routing sequence, continued.

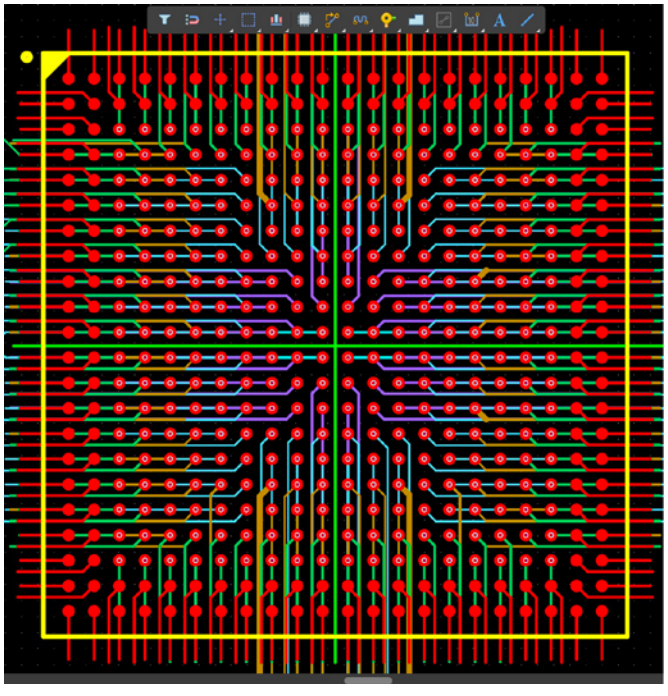

Figure 9: Escape routing screen shot illustrates the complexity of BGA routing today.

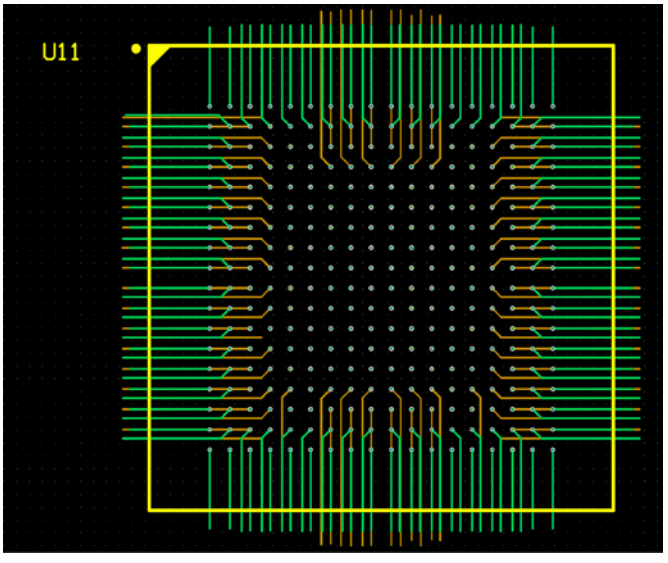

Figure 10: Two adjacent signal layers—a dual stripline structure.

top layer to sig 2, the first internal signal layer, top-plane 1, plane 1-plane 2, plane 2-signal 2. This is due to a need for planes to act as shields between pairs of signal layers and the need for planes to be added as pairs to form planar capacitance to handle the high-speed switching current demand of the digital circuits.

Regarding some of the signal integrity issues that might be encountered using this technique, we will look at two adjacent signal layers—a dual stripline structure (Figure 10). First, you will notice parallelism between the traces

PCBs are complex products which demand a significant amount of time, knowledge and effort to become reliable. As it should be, because they are used in products that we all rely on in our daily life. And we expect them to work. But how do they become reliable? And what determines reliability? Is it the copper thickness, or the IPC Class that decides?

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on the same signal layer, as well as traces on the adjacent signal layers of the dual stripline. The parallelism on adjacent layers is the bigger problem for signal integrity, as this can lead to crosstalk if the critical length is exceeded.

To understand this concern we must understand that critical length is half the transition electrical length (TEL). To understand this, we must understand that TEL is the distance the signal will travel on the transmission line (trace) during the time the signal is being actively driven. This is the rise time/fall time of the digital signal. To calculate the TEL we must determine the velocity of propagation on the transmission line, using the following equation.

$$\sqrt{D_k} = \frac{c}{v}$$ Equation 1

Where:

D_k = dielectric constant

c = speed of light

v = velocity of propagation

Using a little algebraic manipulation, Equation 1 becomes:

$$v = \frac{c}{\sqrt{D_k}}$$ Equation 2

Now assuming a standard FR-4 with a Dk of 4.0 and using imperial units (inches), we get the following:

c = 983.6 x 10^6 ft/s

√Dk = √4 = 2

v = (983.6 x 10^6 ft/s) / 2 = 491.8 x 10^6 ft/s

(491.8 x 10^6 ft/s) x (12 in/ft) = 5.901 x 10^9 in/s

(5.901 x 10^9 in/s) x (1 x 10^{-9} ns/s) = 5.901 in/ns

From this we see that if our rise time/fall time is 1 ns, we have approximately 6 inches for our TEL, making the critical length of half TEL about 3 inches. From this we can see that we can very easily escape out of our FPGA without significant SI issues before we need to add our series termination resistors.

Modern FPGAs such as the AMD Xilinx Virtex UltraSCALE+ FPGA in 16 nm process have switching speeds as fast as 0.250 ns (Figure 11). From this, and by returning to Equation 2 again, we get a TEL of 1.475" and a critical length of 0.738".

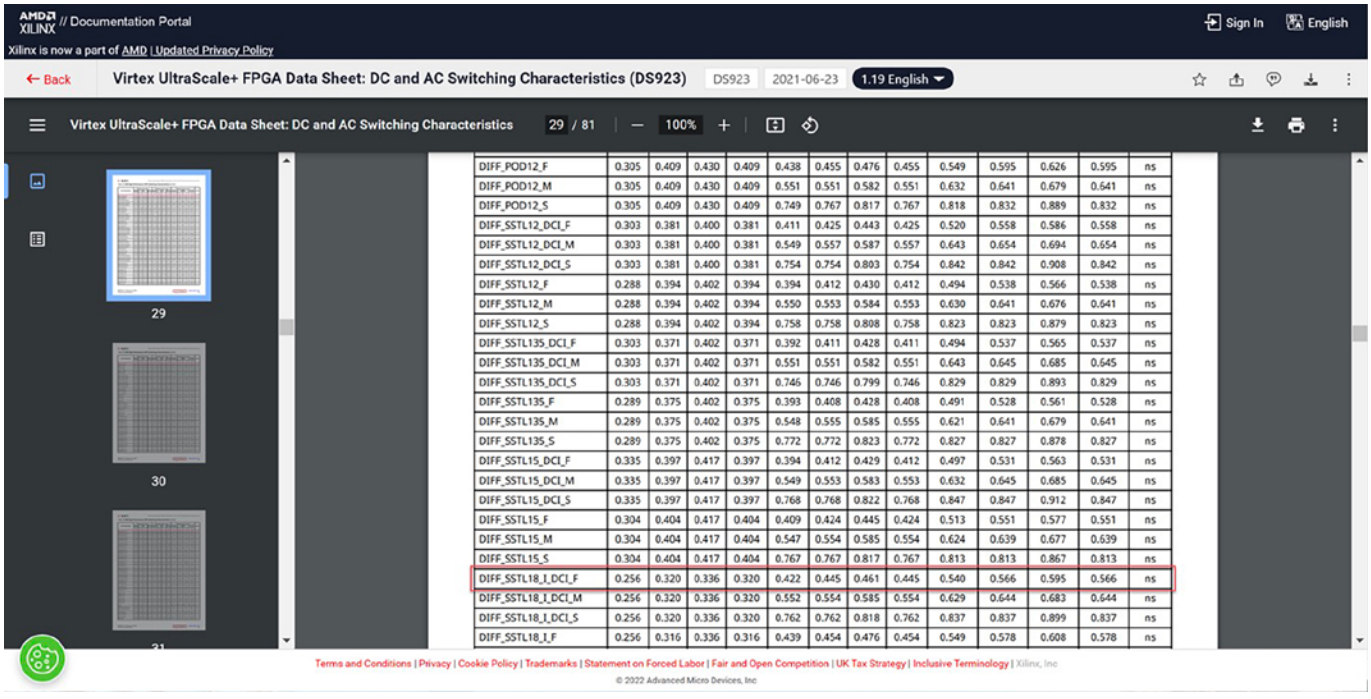

Figure 11: Modern FPGAs have switching speeds as fast as 0.250 ns.

In next-generation devices that are being fabricated in process nodes of single digit nm channel lengths, we are seeing rise times/fall times of 0.1 ns (100 ps) or faster. This gives us TELs of about 0.6 inch and critical lengths of 0.3 inch or shorter. From this we can see that we can no longer expect to be able to route our FPGA traces outside the perimeter of the FPGA body before adding our series termination resistors for successful signal integrity performance.

To successfully solve this problem, the board designer will need to employ formed embedded resistors to the PCB structure. This technique uses a specialty layer of the PCB structure that has two different conductive materials on the same layer. One is the traditional copper, while the other is a resistive material such as nickel-phosphorous (Ni-P) that is used to create the resistors in line with the pins/vias of the FPGA/BGA ball.

Now, to the question of process node: Process node refers to the length of the channel formed between the drain and source of a MOSFET by the gate of the MOSFET. Figure 12 shows an example of a traditional MOSFET structure. As the length of the channel gets shorter, the time it takes an electron to move from the drain to the source gets shorter (faster). This, in turn, is what leads to the faster and faster rise times/fall times in modern devices. This is also why we say that rise time/fall time and not clock frequency is the determining factor for when signal integrity rules must be applied to a design. But that is a discussion for a future article.

Regarding the issue of how to escape route out of modern FPGAs: After we incorporate the embedded resistor for the series termination we need for signal integrity, we still have the issue of crosstalk for the parallel traces on adjacent layers. The main technique to use is trace separation in the Z-axis.

In the event that you are not able to get a sufficient amount of separation/offset between the traces on the adjacent layers, it will be necessary to add additional plane layers to provide shielding/isolation between the trace layers. This approach has its own problems due to the need to add many layers to the board, which increases both mass and overall manufacturing complexity from the increased layer count, as well as the signal integrity desire to always add planes as pairs for Vcc/RTN both for planar capacitance for signal integrity and for proper Z-axis copper balancing for manufacturability. This too is a discussion for a future article.

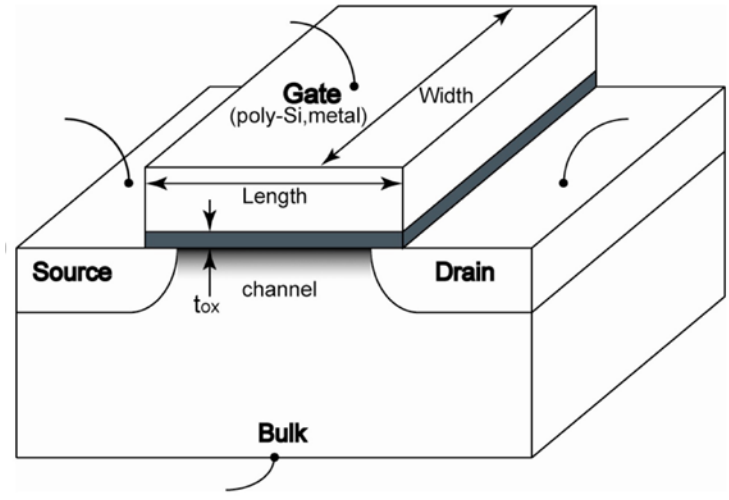

Figure 12: Schematic view of a surface channel MOSFET device indicating physical gate length, channel width, and physical gate dielectric oxide thickness (t ox)[1].

As we have seen, with the reduction in package size and increase in device speeds, escape routing FPGAs/BGAs continues to pose significant challenges to the modern PCB designer. **DESIGN007**

References

1. "Simulation study of scaling design, performance characterization, statistical variability and reliability of decananometer MOSFETs," PhD thesis by Xingsheng Wang at University of Glasgow, May 2010.

Kris Moyer, CID/CID+, is an IPC design instructor and chair of the IPC 1-13 committee.

The Eye Diagram

Beyond Design

by Barry Olney, IN-CIRCUIT DESIGN PTY LTD / AUSTRALIA

An eye diagram is a useful tool for the analysis of signals used in digital transmission. It provides a quick scan of system performance and can offer insight into the nature of channel imperfections. An eye diagram is simply a graphical display of a serial data signal with respect to time that shows a pattern that resembles an eye. Careful scrutiny of this visual display can give one a first-order approximation of signal-to-noise, clock timing jitter, reflections and skew. In this month's column, I will take an eye-ball look at the eye diagram.

An eye diagram overlays the signal waveform over many cycles. The stimulus is normally a pseudo-random bit stream (PRBS). Each cycle waveform is aligned to a common timing reference, typically a clock. An eye diagram provides a visual indication of the voltage and timing uncertainty associated with the signal. In an ideal world, eye diagrams would look like rectangular boxes. However, in reality, communications are not perfect, so the transitions do not align perfectly, resulting in an eye-shaped pattern.

A pseudo-random bit stream is a program that applies mathematical algorithms to simulate randomness. It generates a sequence of binary numbers, synchronized by a clock, approximating the properties of random numbers. The triggering edge may be positive or negative, but the resultant pulse that appears after a delay period may go either way. Therefore, when many such transitions are overlaid, positive and negative pulses are superimposed on each other. Overlaying many such bits produces an eye diagram. This sequence (up to

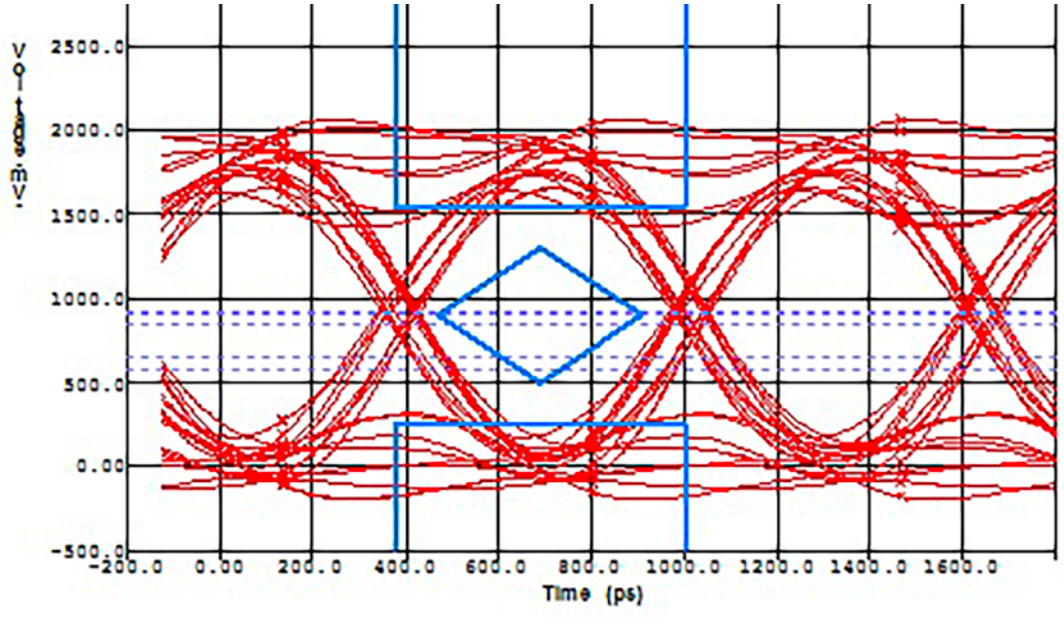

Figure 1: Eye diagram of a serial data stream with an eye mask.

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1024 bits/s) is used to stimulate IBIS models in a transmission line configuration and, at the receiver, results in an eye diagramthat visualizes the signal quality. To get a quantitative view of signal integrity performance, other measurements can be applied to the eye-diagram pattern, including eye height, eye width, signal amplitude, comparative delay, slew rate and setup/hold times. The measured values can then be compared with the JEDEC specification.

The quality of a high-speed digital signal can be quickly determined by using a compliance mask overlay on the eye diagram display (Figure 1). A typical mask includes both time and amplitude limits. The blue area is keep-out.

The mask template can be configured based on the JEDEC specification, in which the middle section of the mask is made up of the setup/hold time and stable voltage threshold specifications. Masks can also be customized to test certain specifications. By applying a mask test to the eye diagram, one can quickly tell if the signal can meet the overall signal integrity requirement. Unfortunately, mask dimensions are often difficult to determine from the specifications.

Eye diagrams include voltage and time samples of the data acquired at some sample rate below the data rate. In Figure 2, the bit sequences (left) are superimposed over one another to obtain the final eye diagram (right).

What an eye diagram (Figure 3) can tell us:

- AC timing noise or jitter, which is indicated by horizontal thickness
- AC noise or reflections, which is indicated by vertical thickness of the bunches
- The unit interval or symbol duration, which is equivalent to the center-to-center spacing of the crossovers
- The peak-to-peak voltage
- Overshoot and undershoot above/below the peak-to-peak waveform
- Whether the ring back is above or below the peak-to-peak waveform
- Rise/fall time, which can be measured from 10% to 90% of the rising/falling edge
- The comparative delay between two or more signals

Jitter arises when a rising or falling edge occurs at times that differ from the ideal. Some edges occur early; some occur late. In a digital circuit, all signals are transmitted with reference to a clock signal. The deviation of the digital signals as a result of reflections, inter-

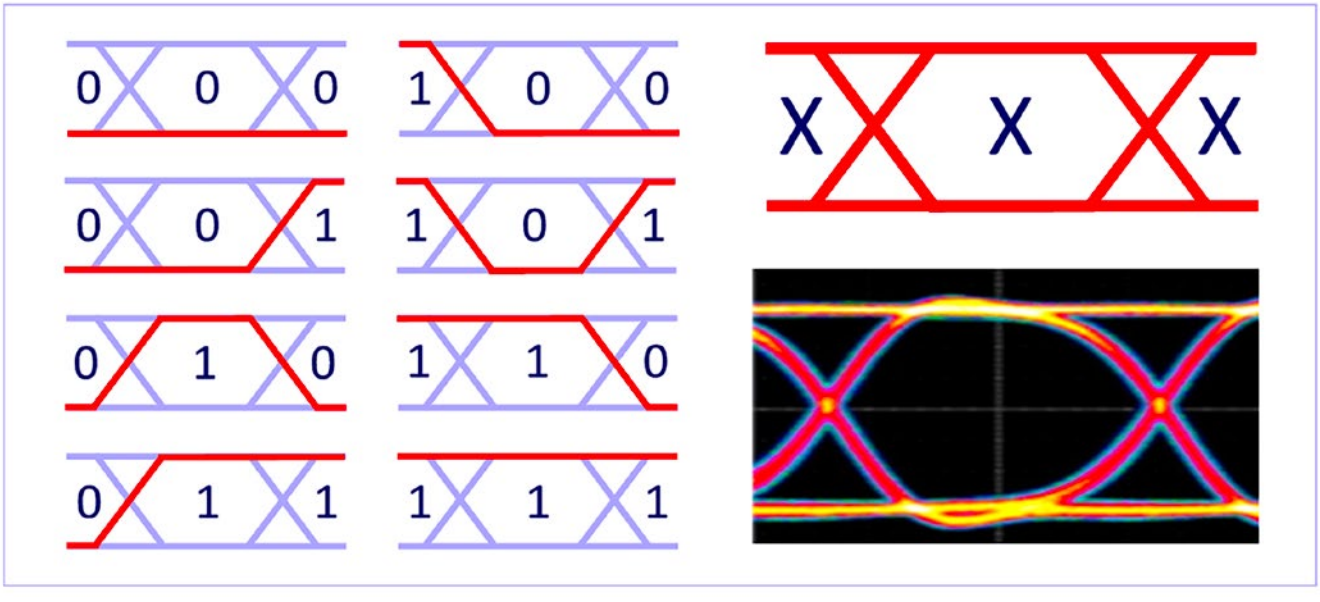

Figure 2: Formation of an eye diagram.

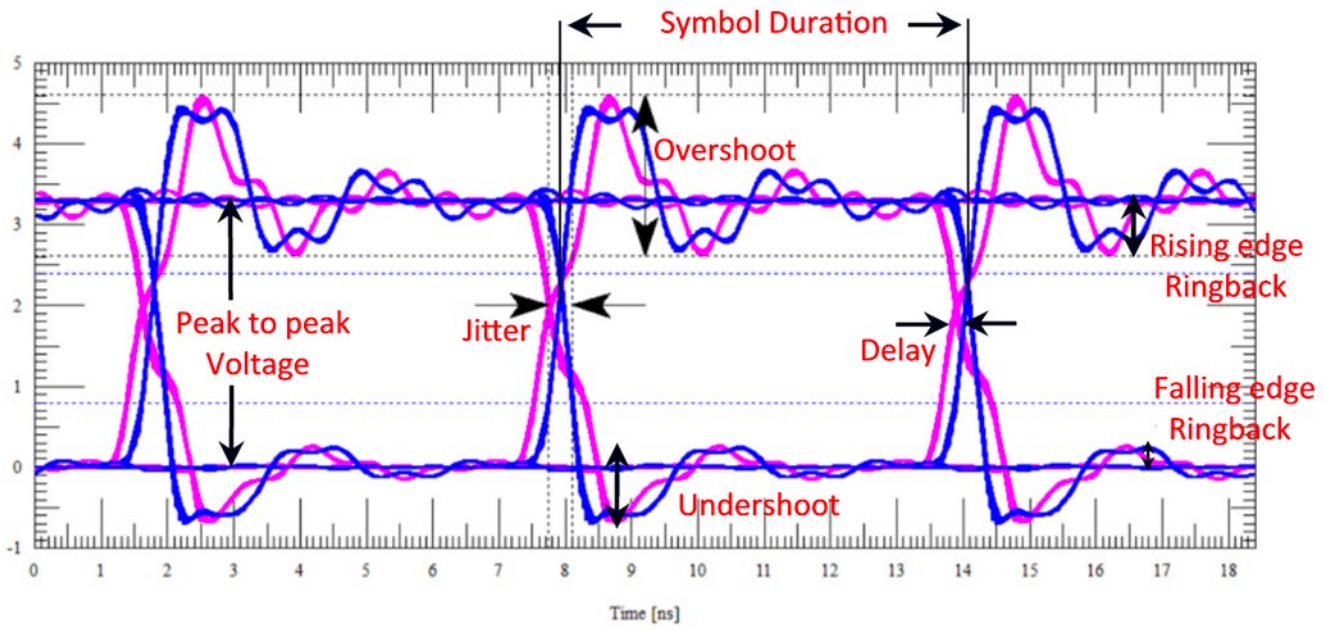

Figure 3: Eye diagram measures signal quality.

symbol interference, crosstalk, process-voltage-temperature variations, and other factors amounts to jitter. Some jitter is simply random.

The impact of termination is clearly visible in the eye diagrams generated. With improper termination, the eye looks constrained or stressed; with improved termination schemes, the eye becomes more relaxed (open). A poorly terminated signal line also suffers from multiple reflections.

A practical way to analyze DDR signals is via the eye diagram. Either read or write DQ is folded into an eye based on the reference clock recovered from the DQS strobe edge. A composite eye diagram can tell the exact jitter content and distribution in your memory interface, as the DQ signals are referenced to a clock (strobe signal). Additionally, it can display reflections from incorrect driver selection and on-die-terminations (ODT), as in Figure 4. Variations (reflections) at the peaks on the waveform indicate inappropriate termination.

Eye diagrams can also pickup stubs on high-speed serial links. Figure 5 shows the effects of excessively long via stubs on a high-speed differential pair. On the left, the differential pair is simulated using a pseudo-random bit stream with lossy transmission lines enabled—note the open-eye pattern. However, on the right, I have included via modelling, which enables the via parasitics and highlights the effects of via resonance. The high frequency harmonics

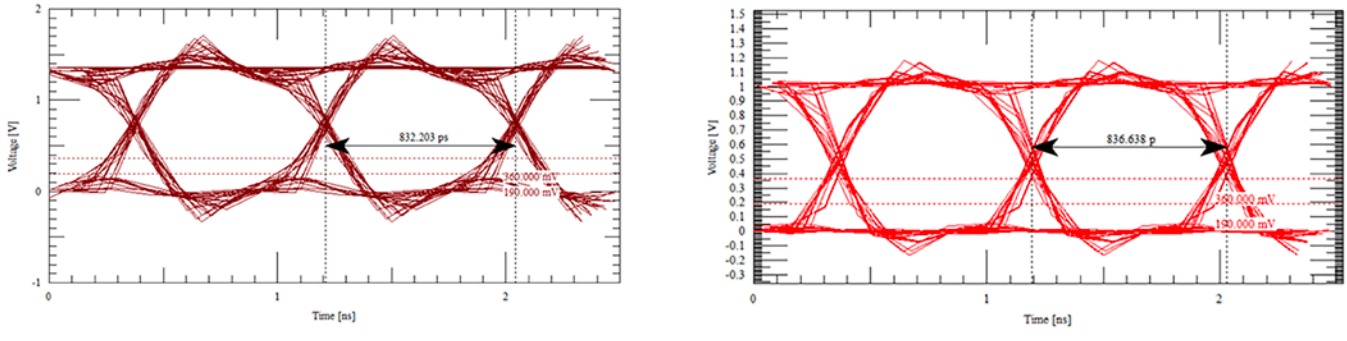

Figure 4: DDR3 data streams. 40Ω driver withno ODT (left); 40Ω driver with 80Ω ODT (right).

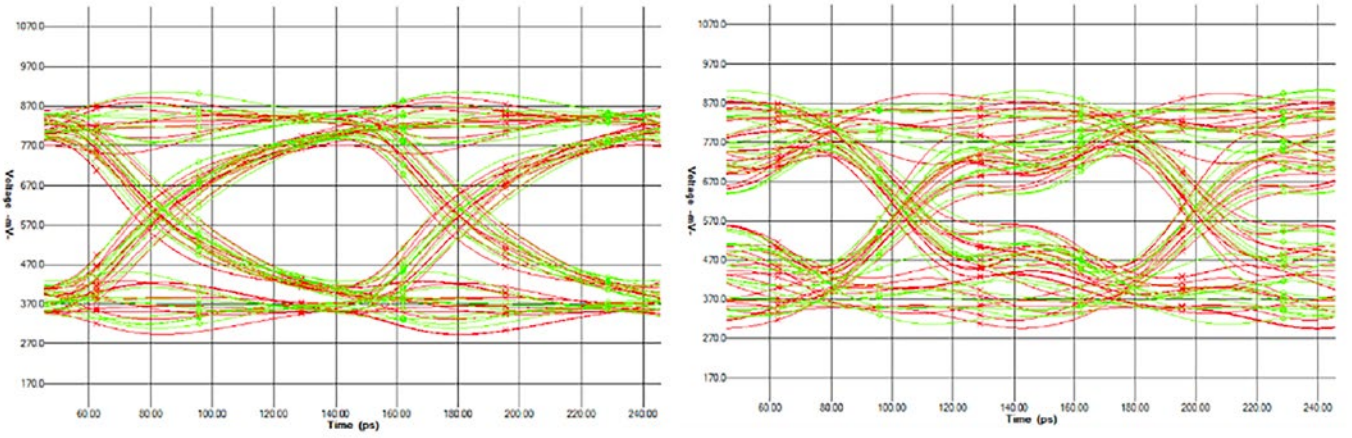

Figure 5: High-speed 10Gbps. Ethernet differential signal (left), and with via resonance (right).

are attenuated, rollingoff the signal rise time, distorting the signal, reducing bandwidth, and closing the eye.

Reflections are reduced dramatically by eliminating the stub. Back-drilling the via stub is a common practice on thick PCBs to minimize stub length for bit-rates greater than 3Gbps (1.5GHz). However, at transmission rates >10Gbps (5GHz), back-drilling alone may not be adequate to reduce jitter and bit error rate.

Eye diagram analysis is not the same as a bit error rate (BER) analysis, but the two techniques are often used in conjunction. The bit error rate percentage is calculated as the number of bit errors per unit of time. Bit synchronization errors are a factor, as well as distortion, interference, and noise.

The eye pattern is a composite signal that indicates the channel bandwidth, attenuation, jitter, reflections, comparative delay, and rise/fall time variations. Eye pattern measurements can show the overall signal integrity of a data path. They provide instant visual data that digital designers can use to check the signal integrity of a design and uncover problems early in the design process.

Key Points

- An eye diagram provides a visual indication of the voltage and timing uncertainty associated with the signal.
- The stimulus is normally a pseudo-random bit stream. Each cycle waveform is aligned to a common timing reference, typically a clock.
- Overlaying many bits produces an eye diagram.
- The quality of a high-speed digital signal can be quickly determined by using a compliance mask overlay.
- The eye mask is made up of the setup/hold time and stable voltage threshold specifications.
- Jitter arises when a rising or falling edge occurs at times that differ from the ideal.
- The impact of termination is clearly visible in the eye diagrams generated.
- A practical way to analyze DDR signals is via the composite eye diagram.
- A composite eye diagram can tell the exact jitter content and distribution in your memory interface, as the DQ signals are referenced to the strobe signal.
- Reflections at the peaks on the waveform indicate inappropriate termination.
- Eye diagrams can also pick stubs on high-speed serial links.
- Back-drilling the via stub is a common practice on thick PCBs to minimize stub length for bit-rates greater than 3Gbps (1.5GHz).

- Bit error rate is calculated as the number of bit errors per unit of time. DESIGN007

Resources

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- *Signal and Power Integrity – Simplified,* by Eric Bogatin, Jan. 2019.

Barry Olney is managing director of In-Circuit Design Pty Ltd (iCD), Australia, a PCB design service bureau that specializes in board-level simulation. The company developed the iCD Design Integrity software incorporating the iCDStackup, PDN, and CPW Planner. The software can be downloaded at www.icd.com.au. To read past columns, click here.

At the Edge of Graphene-Based Electronics

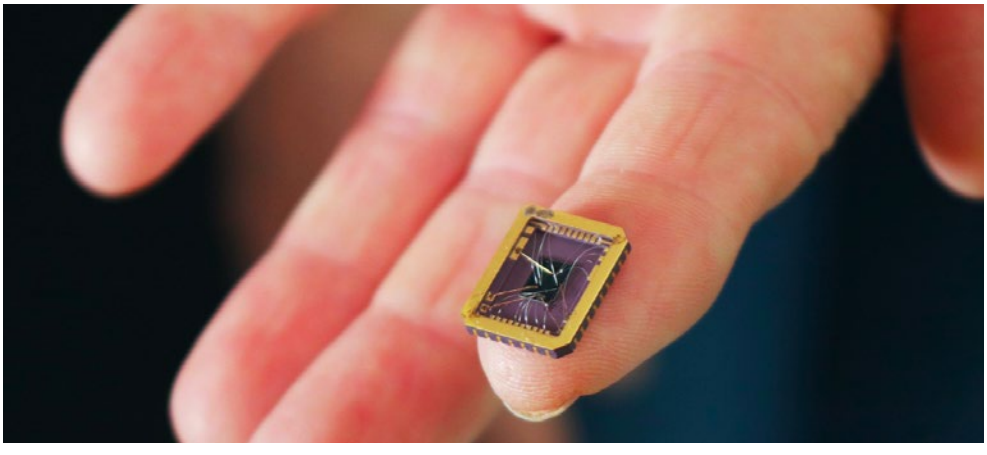
A pressing quest in the field of nanoelectronics is the search for a material that could replace silicon. Graphene has seemed promising for decades. But its potential faltered along the way, due to damaging processing methods and the lack of a new electronics paradigm to embrace it. With silicon nearly maxed out in its ability to accommodate faster computing, the next big nanoelectronics platform is needed now more than ever.

Walter de Heer, Regents' Professor in the School of Physics at the Georgia Institute of Technology, has taken a critical step forward in making the case for a successor to silicon. De Heer and his collaborators developed a new nanoelectronics platform based on graphene—a single sheet of carbon atoms. The technology is compatible with conventional microelectronics manufacturing, a necessity for any viable alternative to silicon. Their discovery could lead to manufacturing smaller, faster, more efficient, and more sustainable computer chips, and has potential implications for quantum and high-performance computing.

To create the new nanoelectronics platform, the researchers created a modified form of epigraphene on a silicon carbide crystal substrate. In collaboration with researchers at the Tianjin International Center for Nanoparticles and Nanosystems at the University of Tianjin, China, they produced unique silicon carbide chips from electronics-grade silicon carbide crystals. The graphene itself was grown at de Heer's laboratory at Georgia Tech using patented furnaces.

This process mechanically stabilizes and seals the graphene's edges, which would otherwise react with oxygen and other gases that might interfere with the motion of the charges along the edge.

It will likely be another five to 10 years before we have the first graphene-based electronics, according to de Heer. But thanks to the team's new epitaxial graphene platform, technology is closer than ever to crowning graphene as a successor to silicon.



(Source: Georgia Tech, photo credit: Jess Hunt-Ralston, Georgia Tech)

A Challenge Facing Aerospace Designers in 2023

Feature Article by Lee Ritchey
SPEEDING EDGE

As the aerospace industry has been tasked with fitting increasingly complex electronics in existing airframes the demands on PCB substrates have begun to overtask the existing state of the art in PCB fabrication.

Recently, I was called in to troubleshoot some reliability problems with a very dense PCB that had components on both sides and required the use of stacked blind vias and buried vias. The usual name for this kind of design is "build-up fabrication," requiring many trips through the lamination, drilling, and plating operations at a fabricator.

The designers decided to reach down from the outer layer to the third layer below the surface using stacked blind vias, much like that shown in Figure 1.

The process used to create the structure in Figure 1 is to fabricate a PCB using the ordinary lamination, drilling, and plating processes employed for any multilayer PCB. Once this is done, a laser drill is used to create the

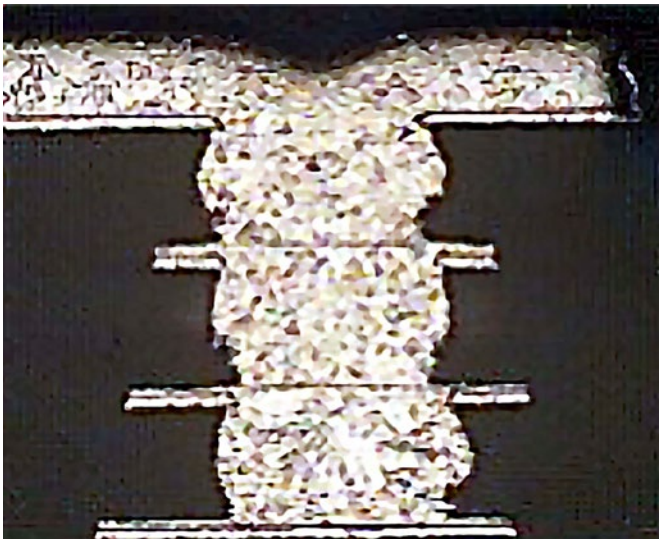


Figure 1: An example of stacked microvias.

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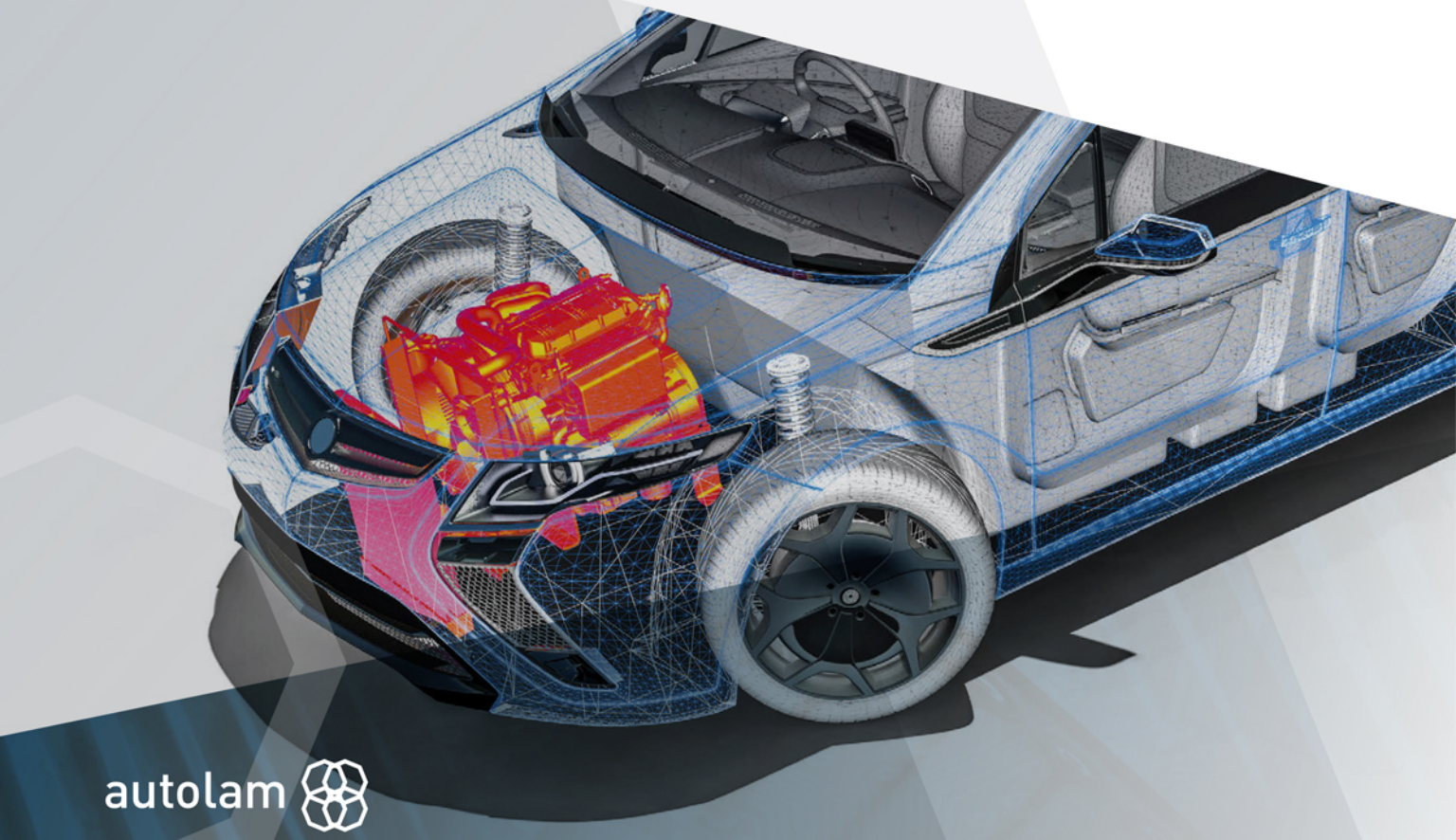

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Figure 2: Close-up of an unfilled laser-drilled blind via.

first blind via at the bottom of the stack as shown in Figure 1. As can be seen in Figure 2, at this point, the blind via has not been filled with copper.

To stack another blind via on top of the first one, the void must be filled with copper by employing an operation called "button plating." This results in tiny bumps of copper sticking up above the surface at each blind via. These bumps are removed by sanding to make the surface flat again. This is followed by laminating another layer of prepreg and copper thus creating a new outer layer.

The blind via laser drilling is repeated above the existing blind via and the plating steps are repeated to create the next blind via and then the third stacked blind via, resulting in a set of stacked blind vias like that shown in Figure 1.

The problem with reaching down to layer 3 is that the copper bond between the lowest blind via and the copper in the layer it attaches to is very weak. As the operating temperature of the device containing the PCB increases, the resin in all three laminate layers containing these stacked vias expands, pushing up on the copper pad on layer 1. This stress pulls the copper in the bottom via away from the layer it is in contact with, creating an open circuit.

When an assembly with this kind of defect is returned to the factory for repair, it has cooled off, the resins have contracted, and the circuit works properly. The assembly is returned to the field where it fails again. This process repeats until someone discards the assembly. Sometimes these PCBs are referred to as "rubber band" PCBs because they keep bouncing between the factory and the field as if they are

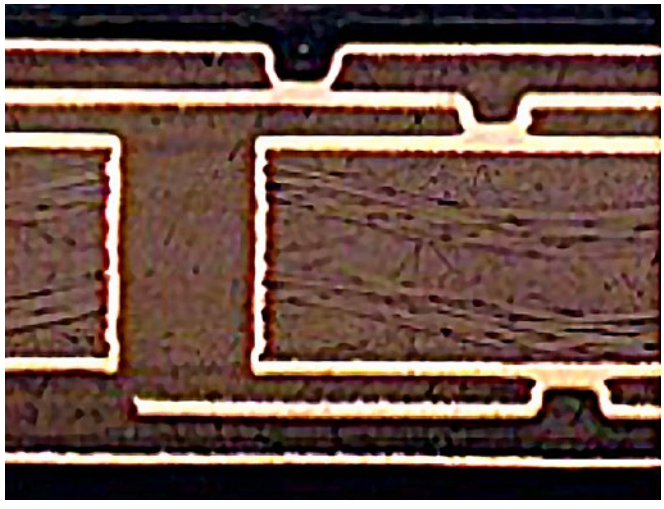

Figure 3: Staggered blind vias.

connected to the factory with a rubber band. Unfortunately, there is very little that can be done during fabrication to increase the bond strength between the bottom blind via and the layer it contacts.

But there is an alternative that can implemented early in the design cycle: The use of staggered blind vias as shown in Figure 3. Staggering vias precludes the above problems.

Engineers and designers from around the globe are looking into this problem, including the IPC's Weak Interface Microvia Failures Technology Solutions Subcommittee. But in the meantime, designers—particularly in the aerospace segment—should consider using staggered vias for complex PCBs like this.

With the demand for increasingly dense electronics in avionics and other military products, this kind of failure is going to appear more frequently unless designers find other ways to make connections deep into a PCB using blind vias. **DESIGN007**

Lee Ritchey is the founder of Speeding Edge and a signal integrity instructor who estimates that he has taught more than 11,000 engineers during his career.

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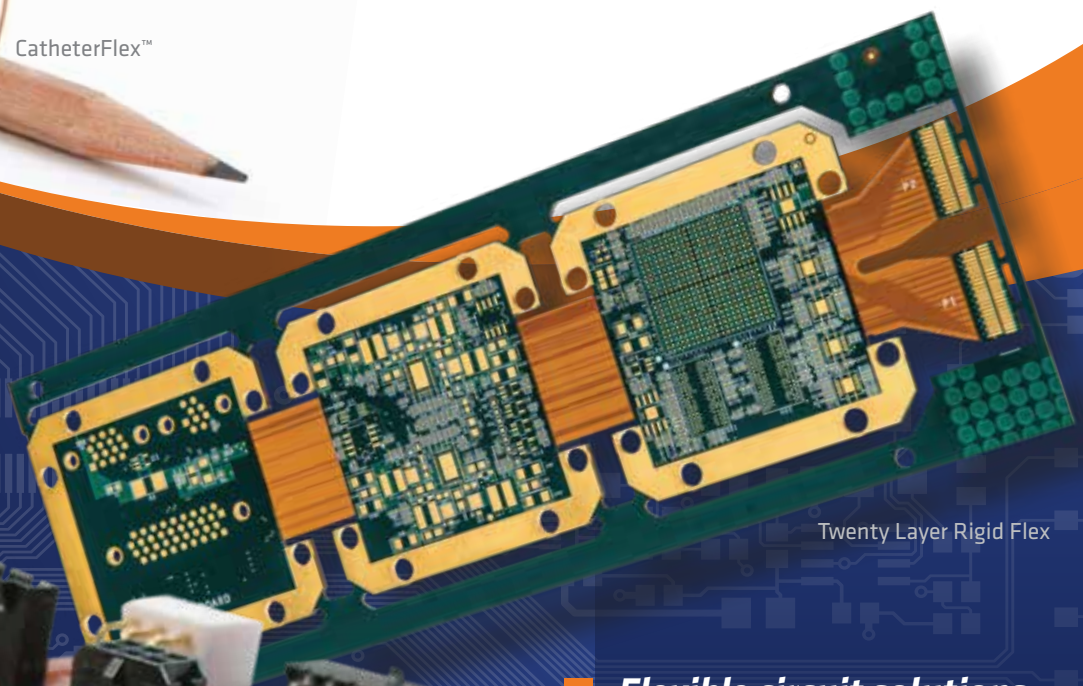

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Threading the Needle Through Advanced Packaging

Tim's Takeaways

Feature Column by Tim Haag, FIRST PAGE SAGE

Last week, my wife started a new sewing project that required a trip to the craft store for supplies, and she invited me to join her on this errand. This is not the first time I've faced this scenario: do I choose to follow her around the craft store pushing the miniature cart that will, by the time we get to the register, barely contain all her chosen fabrics and materials, or stay at home and watch TV? Thankfully, by this point in my life I've learned which is the right choice, so we hopped in the car and headed down the road to the craft store.

I've been involved in electronics for a very long time now, and I am very familiar with the various manual and automated methods used for PCB design, as well as the different tools and machinery used in their manufacturing. With this background, a simple project using needle and thread should be a cakewalk for me, don't you think? So—somewhat arrogantly, I must confess—I figured that my wife would ultimately benefit from my experience and expertise when it came to putting her project together.

Boy, do I feel like an idiot now.

The first thing that caught my eye in the craft store was an aisle loaded with assorted tools, where I noticed a selection of cutting instruments. Now I've always called them "scissors," but here was my first lesson of the day: Do you have any idea just how many types of scissors are used when sewing? The type of scissors you'll need is dependent on whether you are working with small fabrics, embroidery, or double-curved embroidery. Then there are dressmaker shears, pinking shears, and tailor shears. But before we're done, you also need to know about snips, heavy duty shop snips, applique, and of course, general purpose scissors. It doesn't stop there. You also need to know when to use serrated blades, non-stick coating, what kind of grip is best, which brands

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are recommended—and that's all just for the scissors. We could continue with a discussion on the whole line of rotary cutters, but let's escape from the sewing tool aisle while we're still young.

My wife expertly navigated her way through the various areas of the store, choosing between different fabrics, trims, and zippers. Next, she explored several different types and colors of thread, plus the bobbins required to install this thread in her own sewing machine. Buttons and interfacing had to be selected based on color, size, and durability. Just for kicks, we looked at patterns for potential future projects. However, all this took far less time than I would have expected because she had already planned how much fabric she would need, as well as how all the seams, hems, and stitching would be coordinated. Then she said something about a phone, and I thought that we were headed to the Verizon store next. Nope, she meant "foam," not phone, which was another unique yet crucial component of this project. Would you like me to tell you how many different types, styles, and sizes of foam there are to work with? I didn't think so.

Would you like me to tell you how many different types, styles, and sizes of foam there are to work with? I didn't think so.

By the end of the day, I had come to realize that my extremely naïve and rather arrogant perspective on my wife's sewing was completely out of line. She obviously has just as much—and probably a whole lot more—experience and expertise in the world of sewing as I do in PCB design. After following her around the craft store, I know that I would much rather spend the day puzzling together some complex DDR routing than trying to understand how to sew. But isn't that the case with most things? There will always be those who have a greater amount of experience and expertise in a specific subject matter. To quote an adage: "There's always a bigger fish." An excellent example of this is the advanced packaging of PCB components, and how part selection affects the way we lay out a design.

When I first started designing circuit boards, components were less dense and more generic in both size and shape. I remember being told to leave enough room at the top of my through-hole 14-pin DIPs for a bypass cap. When I asked for the size, shape, or part number, I was told that it wasn't important; I just needed to create a generic part with a 0.4" x 0.1" rectangle using 62-mil pads spaced 300 mils apart from each other. They (whomever "they" were) would figure out later what to put in there, or they would just leave that part location empty. I wouldn't recommend using a relaxed component selection technique like that on a next generation smartphone design, as it probably won't get you many admirers.

Today, there are many component packaging variables that designers must consider when designing a board. Here are a few that come to mind:

- Functionality
- Power
- Price
- Availability
- Component life cycle
- Routability
- Human interface

Depending on the options, designers need to choose the part that will work best for their circuit, but they also must take into account the part's power needs and thermal issues, as well as whether the board design will support it. Before they can check off component selection on their to-do list, they also need to consider the part's price and availability, and

whether that availability will extend throughout the life of the project. Then they will have to verify that the component's footprint and density will work with the layer stackup and anticipated routing parameters. Lastly, the ability to manufacture, test, configure, rework, or manipulate the part by technicians and/or end users must also be considered. Yes, there's a lot to consider when choosing parts, and making a mistake can be costly.

One board that I designed many years ago had a new, unique through-hole connector placed in the middle that spanned almost the complete width of the narrow board being designed. This was a new part, and those that planned the interconnect strategy of the device had carefully chosen the connectors on the different boards for their size and pin density. The plan was to leverage the multiple layers of the board to route out of the connector, as well as to route all the other board traces between its pins. The problem was that the connector specifications called for a pad size that didn't allow for trace routing between pads, but no one had thought to check on this critical detail when the connectors had been chosen. By the time this design got into my hands, the mating connector had already been built into the other boards in the device—we were stuck. If memory serves, I think that we had to get a special exemption from our manufacturers just to build the board.

This story illustrates the importance of not only choosing the correct component for the application, but also the critical need for expertise in advance component packaging; without advanced packaging know-how, designers can't understand all the aspects and implications of using a new part. As I said earlier, component selection mistakes can end up being very costly in terms of manufacturing expenses and board failures. Yet as new and increasingly advanced PCB components become available, making these kinds of mistakes becomes more likely. While we would all do well to learn as much about component engineering as possible, it's important to identify resources that can help us understand the latest developments in advanced packaging and how they might affect component selection. One such resource is your circuit board manufacturer, who often has a full-time staff of component engineers to ensure that the best possible part choices are being made for their customers. Also, this edition of *Design007 Magazine* is full of insights from leaders in the PCB component packaging field on new technologies and how to make the best part choices.

The moral of the story is to not be ashamed to admit when you need help, especially when it comes to PCB component selection.

The moral of the story is to not be ashamed to admit when you need help, especially when it comes to PCB component selection. It may very well save you a lot of time, grief, and expense in the end. Today's advanced parts include high-density, fine-pitch BGAs that demand a well-thought-out layer stackup and routing strategy long before they are ever placed on the board. Just as my wife knew exactly what she needed from the craft store before she even got in the car, PCB designers need to know just how much we can and can't do with the parts in our designs—before we go to layout.

Until next time, keep on designing. **DESIGN007**

Tim Haag writes technical, thought-leadership content for First Page Sage on his longtime career as a PCB designer and EDA technologist. To read past columns, click here.

Advanced Packaging Not a Passing Fad

Elementary, Mr. Watson

Feature Column by John Watson, CID, ALTIUM

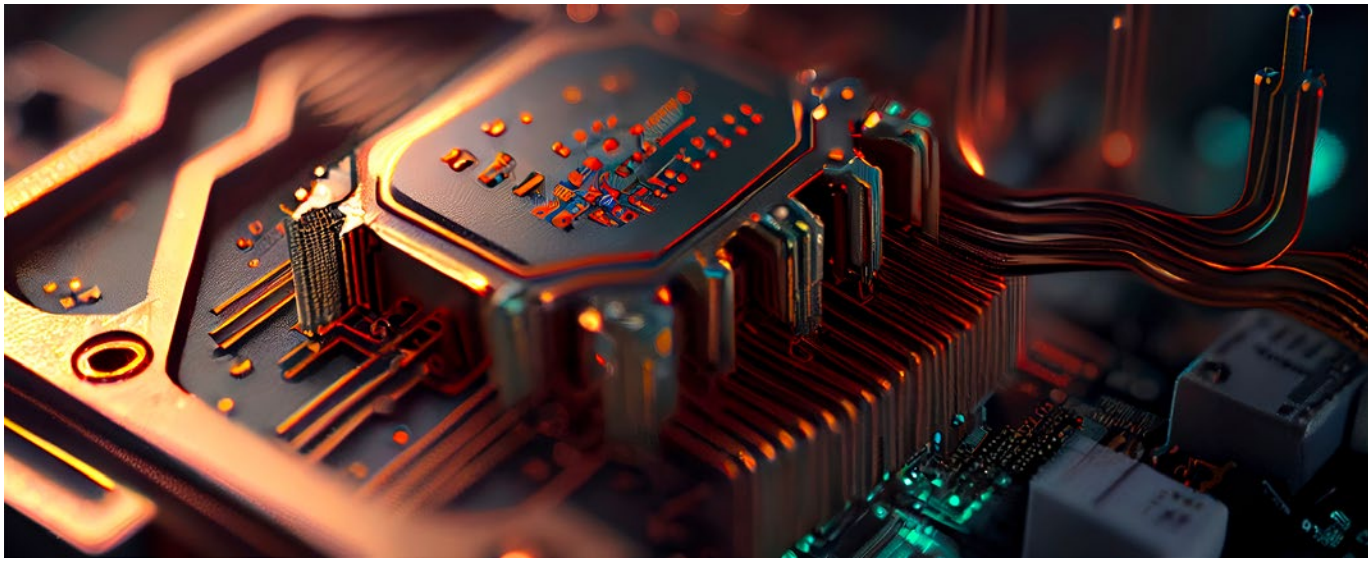
We live in what can only be described as the golden age of electronics. Advancements and innovations grow by leaps and bounds, and never in history has the field of electronics grown at such a fantastic rate. Yet necessity is the mother of invention when discussing the PCB design industry and the advanced integration packages field is one of the fastest-growing and most exciting.

In 2020, the advanced packaging market was worth $24 billion and it's expected to grow as the estimated compound annual growth rate (CAGR) is 8%[1]—phenomenal growth resulting from consumer demand. It's an insatiable appetite for something bigger and better, not only with higher speeds in a smaller package, but to be inexpensive; this is what drives our industry and keeps us employed. This demand is on full display when Apple releases its latest and greatest, and folks are camped out for days waiting for the release. This trend shows no signs of slowing down. One solution to high demand? Advanced packaging. As legislation with the CHIPS Act focuses on domestic semiconductor fabrication, the aim should be to increase the advanced package industry into the mainstream.

Challenges with Advanced Interconnect

Ever since Jack Kilby of Texas Instruments created the first hybrid IC made of germanium in 1958, and Robert Noyce created the first monolithic IC in 1959, the IC has generally remained the same—except for one significant difference in reducing the size of the transistors that make up every IC. When Kilby and Noyce created the first ICs, the size of the transistors was 11 nm. With today's smaller transistors, more nodes, as they are called, are now inside each IC.

By 1965, Gordon Moore estimated that a computer's speed and capability could expect



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to double every two years because of increases in the number of transistors a microchip can contain. It was a shocking statement when Moore announced that a single IC would someday hold 65,000 transistors. The size of IC nodes is now being mass-produced at 5 nm, which was commercially released in the Apple A14 Bionic chip. The transistor count now sits at a staggering 11.8 billion, a 38.8% increase from the A13's transistor count of 8.5 billion.

By 2024, the expectation is to be even smaller at 2 nm. For perspective, that is smaller than human DNA and could hold over 50 billion transistors on a chip the size of a fingernail.

But before we pop the cork on the champagne, I believe we have reached or very close to reaching the limits of our capability to produce chips reasonably and reliably. As things shrink, simply controlling the current flow in such a small area is very difficult. In other words, we are now getting so small that we can no longer control the electrons.

As things shrink, simply controlling the current flow in such a small area is very difficult.

We are simply running out of room. Many believe that Moore's Law is dead, particularly NVIDIA CEO Jensen Huang, who proudly announced his belief in this idea last year. I am not at that point yet, but it does feel like Moore's Law is on life support. Although we call it a law, even Moore agreed it was more of an observation. In his 1965 publication, *Cramming More Components onto Integrated Circuits,* he admitted that "the including micro-assembly techniques for individual components, thin film structures, and semiconductor integrated circuits. Each approached evolved and rapidly and converged." In an interview in April 2005[2], Gordon Moore stated that the projection could not be sustained indefinitely: "It can't continue forever. The nature of exponentials is that you push them out, and eventually disaster happens." He also noted that transistors eventually would reach the limits of miniaturization at atomic levels:

In terms of size [of transistors], you can see that we're approaching the size of atoms which is a fundamental barrier, but it'll be two or three generations before we get that far—but that's as far out as we've ever been able to see. We have another 10 to 20 years before we reach a fundamental limit. By then, they'll be able to make bigger chips and have transistor budgets in the billions.

Another major problem we face is making all the interconnects to a high-density device so that it's a functional item on a PCB design. Conventionally it's done through wire bonds, which have not scaled down at the same pace as the transistor. With 11.8 billion transistors in a single chip, that is more processing power than wires can carry. Getting signals from the silicon out to the real world, which connects to the PCB, is a significant issue.

Frankly, we are reaching the industry limitations in more ways than one.

A Paradigm Shift of Advanced Packaging

Occasionally it's good practice to examine how we do things. Advanced packaging technology (APT) is a paradigm shift for the entire industry. It promises to solve the challenges we face. We can define APT as the aggregation and interconnection of components before traditional electronics packaging. Advanced packaging allows multiple devices (electrical, mechanical, or semiconductor) to be merged and packaged as a single electronic device. They are taking different circuits that were separate chips on the PCB design before and placing them all in a single chip.

Although we are not specifically talking about applications when speaking of APT, we will find

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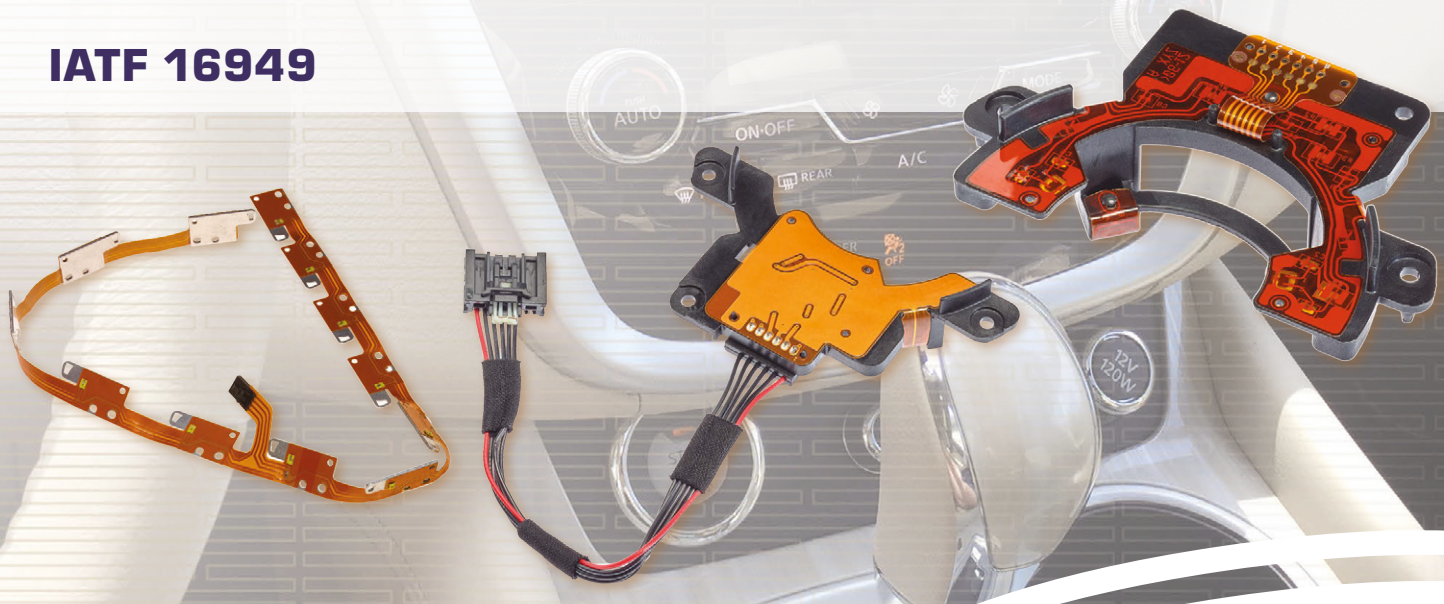

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that particular packaging methods are popular with various industries. For example, high-end AI products such as smartphones and graphic processing units lean more toward 2.5D technology. The industry demands target specific applications and markets with how the various individual circuits are combined with the packaging methods.

The various methods of advanced packaging are listed below.

- Wafer level packaging
- 5D and 3D
- System-in-package
- Bumping and flip-chips
- Chip scale packages
- Redistribution layers
- Embedded die substrate
- MESM and microsystem packaging

Inherent Problems With APT

The APT comes with several inherent problems. First is power dissipation and power use; directly connected to that is the increase and necessity of heat dissipation. Traditionally, silicon generates a lot of heat and is not thermally efficient. It is now seeing a decrease in voltages, but to maintain or increase the power means an increase in current. How is this power migrated through the package and the heat dissipated? Even just a single chip can have problems with power consumption and heat. Now we combine them with other items such as in a system-in-package (SiP) that also holds the microprocessor, the flash, and the SRAM all in a single chip. We've just increased the issue exponentially.

Known Good Die (KGD)

When combining the various individual parts, especially when designing a SiP design package, It is unknown whether an individual circuit works until it is in the final package configuration. Because specific devices cannot be adequately tested beforehand, the failure rate is high and expensive due to lost production time. That is an issue known to the industry as "known good die." How the individual dies are tested and validated must be solved. Usually, one only finds out about these issues after it's too late.

Cost Issues

Most integrated circuit manufacturers' equipment is not ready for the onslaught of advanced packaging. The equipment for such a process is highly specialized and expensive. This specialty requirement is driving up the cost of APT devices on the market. In the future, we should expect that costs should come down.

Conclusion

Advanced packaging technologies have a bright future. The insatiable appetite that the everyday consumer is looking for and expecting from their devices is increasing. It drives this new technology—one that is now mainstream as we finally put to rest Moore's Law and change how we look at the semiconductor industry with a major paradigm shift. Instead of simply looking at increasing node density, we can now customize based on entire sections of circuits for a specific industry and application. It's an exciting time. **DESIGN007**

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John Watson, CID, is customer success manager at Altium, a professor at Palomar College, and an I-Connect007 columnist. To read past columns, click here.

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Celestica Inc., a leader in design, manufacturing, and supply chain solutions, is pleased to announce the appointment of Jill Kale to its Board of Directors effective December 1, 2022.

Lockheed Martin Successfully Hosts Advanced 5G.MIL Capabilities on Flight Ready Hardware ▸

Lockheed Martin, in collaboration with Intel, accomplished an industry first by successfully integrating a 5G Core and Open Radio Access Network into Lockheed Martin's 5G.MIL Hybrid Base Station.

BAE Systems, Purisolve Launch Promoveo Solutions Joint Venture ▸

BAE Systems and IT services company Purisolve, Inc. have combined forces to form a joint venture, Promoveo Solutions.

Collins Aerospace Expands in India ▸

As part of a significant investment to expand its engineering, digital technology, and manufacturing operations in India, Collins Aerospace, a unit of Raytheon Technologies Corp., has officially inaugurated its new Global Engineering and Technology Center and Collins India Operations Center in Bengaluru.

SAIC Awarded Approximately $950M in Space, Intelligence Contracts ▸

Science Applications International Corp. received approximately $950 million in space and intelligence contract awards during the third quarter of fiscal year 2023.

Smiths Detection Opens New UK Biolab ▸

Smiths Detection, a global leader in the development of threat detection and security screening equipment, opened a biolab at its centre of excellence in Hemel Hempstead, UK.

NASA's Europa Clipper Gets Its Wheels for Traveling in Deep Space ▸

Just as NASA's Mars rovers rely on robust wheels to roam the Red Planet and conduct science, some orbiters rely on wheels, too—in this case, reaction wheels—to stay pointed in the right direction.

Momentus Signs Contract with Australian Research Centre ▸

Momentus Inc., a U.S. commercial space company that offers transportation and other in-space infrastructure services, has signed a contract with the CUAVA Training Centre at the University of Sydney to deploy the CUAVA-2 CubeSat in low-Earth orbit in October 2023.

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Inmarsat, a leader in global, mobile satellite communications, has unveiled a major innovation to its maritime safety portfolio: a next-generation terminal that will allow quick and easy access to industry-leading connectivity services.

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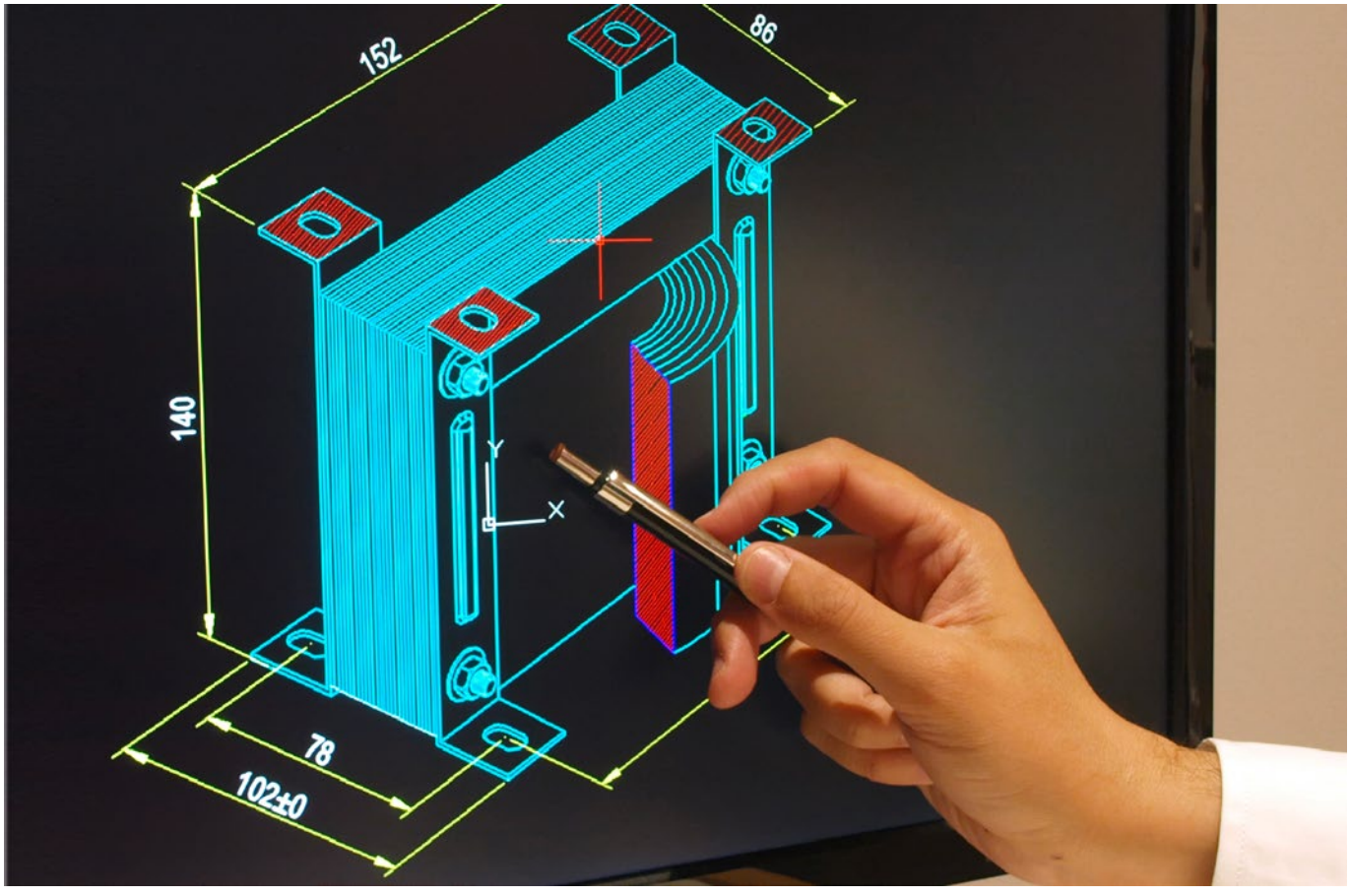

PCB Designers Are Really Product Designers

Article by Zachariah Peterson
ALTIUM

As I look back on 2022, I'm realizing that my company plays multiple roles in client projects beyond just designing circuits and PCBs. Sure, we're primarily a PCB design company, but we also help with things that happen outside the PCB. This includes tasks like enclosure design, defining mechanical constraints, simulating electrical behavior, mating boards into larger assemblies, selecting cabling, and defining test requirements, all of which slowly creep into the standard scope of work for design projects.

The same set of tasks have crept into CAD software features, especially in the PCB design space. Both mechanical design tools and PCB design software have expanded their capabilities beyond enclosure/fixture design and board layout, respectively. Looking at some of the capabilities in a platform like Fusion 360, the MCAD side has significantly outpaced the ECAD side.

In the ECAD/EDA world, we still focus mostly on simulation and fit to enclosure, but there is so much more that goes into full-scale product development, and the ECAD software world should start to move much faster toward the goals I outline below.

What PCB Designers Need for Product Development

As I mentioned in my earlier I-Connect007 article on simulation, designers need much simpler simulation access either inside their

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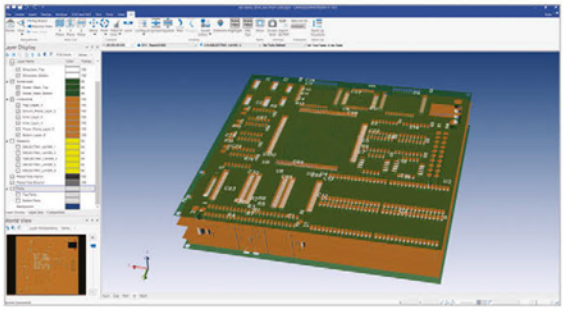

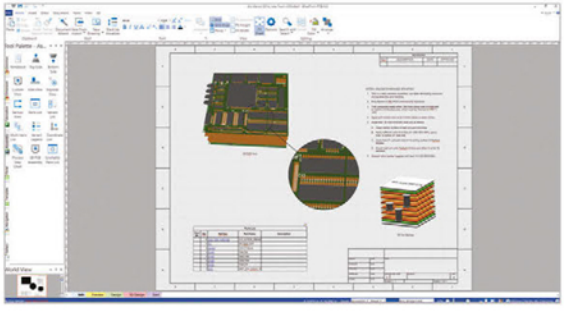

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native PCB design tool or through a direct and seamless integration with another design/simulation program[1]. Now that ECAD/MCAD collaboration has helped bring electrical and mechanical co-design under one roof, designers can instantly pass ECAD data into the MCAD system and vice versa.

What else can the ECAD industry do to support product design? Based on both my personal experience with client projects and current ECAD industry trends, here are some things I'd love to see.

Cable and Harness Design

This area is finally coming to fruition from my preferred EDA vendor, and I expect similar features from others. Many products, whether they are multi-board assemblies or requiring a connection to an external product, may do so with custom cables, custom or standard mated connectors, or flex ribbons.

Harness and cable definition at the logic level, visual integration into the assembly, and even physical design of custom cable assemblies—these are all essential parts of product development. The immediate benefit is in MCAD, where the connector and cable can be viewed in a larger system. However, the broader benefit is in simulation and rules checking, where logical definitions in interconnects are used to examine electrical behavior.

This takes a much higher-level view of systems design and eliminates the phenomenological modeling required in larger assemblies. For example, a harness-plus-cable model extracted from measurement or simulation could be used in SPICE to examine signal and power propagation across the interconnect before creating the PCB layout.

Embedded Development

I continue to be surprised at the lack of support for embedded development by ECAD software vendors. I often make the joke to my ECAD/EDA clients that our industry has totally ignored embedded, and that we've done this at our own peril. The closest we've come to supporting embedded systems development falls into three areas:

- FPGA system-level planning
- Embedded compilers targeting specific chipsets
- Version control

What we don't see is an integrated development environment (IDE) as part of a PCB design application, where users can create and manage libraries, their codebase, vendor libraries and code examples, reference design codebase, and a project's revision history. On the FPGA side, it would be wonderful if designers had the ability to see information a developer would see in the FPGA vendor IDE. We need this type of information to complete schematics for some of our most complex projects; being unable to see how IP can be implemented in our boards has led to redesigns, delays, and of course, cost overruns for the client.

Component Packaging

In the future, I expect to see our industry shift its focus to different types of electronics assemblies, especially as length scales continue to shift smaller into UHDI. Here I'm referring to heterogeneously integrated components on substrates and interposers, where the designer takes control of the component capabilities and footprint.

In particular, I expect the packaging revolution to create a major shift in the way systems design teams approach new products, and especially the role PCB designers have to play in product development. IC substrates are basically just small circuit boards with very fine features; as the packaging market and heterogeneous integration starts to look a lot like the standard PCB market, PCB designers have the skills to immediately fill this product design gap.

It may take several years, or possibly a decade, for the traditional electronics design

process to get mirrored into substrate and packaging design, but I'm confident it will happen. This process is simply too big an enabler of advanced products at smaller scales to be ignored by the semiconductor industry, the big electronics distributors, and ECAD vendors.

Looking to the Future

I expect to see more of the direct electromagnetics simulation integrations and system-level EDA features appear in ECAD software, continuing the trend we've already seen in recent years. Products from vendors like Keysight, Ansys, and others all play well with ECAD software, either through direct integration or a simple file export. The same goes for products like PTC Creo, Solidworks, and Autodesk, all of which have mechanisms to directly pass data with various ECAD platforms.

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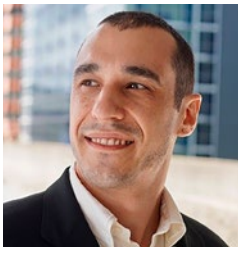


Zachariah Peterson is the founder of Northwest Engineering Systems and a consultant for Altium.

Soft Touch Sensitivity

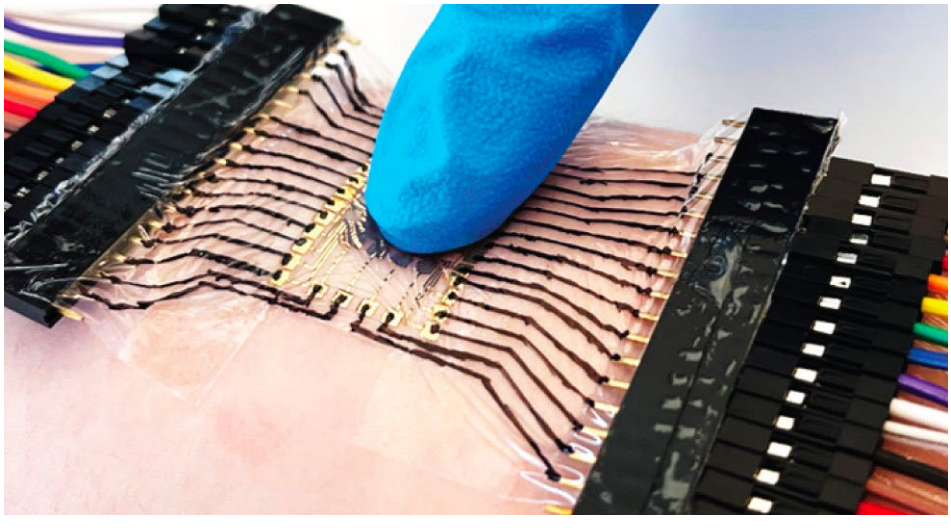
A soft and flexible electronic "e-skin," so sensitive it can detect the minute temperature difference between an inhaled and an exhaled breath, could form the basis of a new form of on-skin biosensor. The ultrathin material is also sensitive to touch and body motion, suggesting a wide array of potential applications.

"The skin plays a vital role in our interactions with the world," says Vincent Tung from KAUST, who led the work. "Recreating its properties in an e-skin could have profound implications for wearable electronics, as well as for sensory prosthetics, soft robotics and human-machine interfaces," he says. Despite considerable research effort, however, it has been very challenging to create suitable materials, which must be strong and highly sensitive, yet imperceptible when applied to the skin.

A carbon nanomaterial called hydrogen-substituted graphdiyne (HsGDY) could be ideal for the task, Tung and his collaborators have shown. This two-dimensional sheet of carbon atoms has similarities to graphene in its strength and electrical conductivity, but also has key differences, Tung notes.

The team were able to show what the theory had predicted: the resulting material was highly twistable, stretchable and mechanically durable. "At around 18 nanometers thick, our e-skin is a fraction of the thickness of human skin, enabling conformal contact and long-term adhesion to the body with maximum flexibility and comfort," Tung says.

The material's island-bridge atomic structure not only contributes to HsGDY's soft and flexible nature but is also key to its electronic properties, Tung adds. (Source: KAUST)



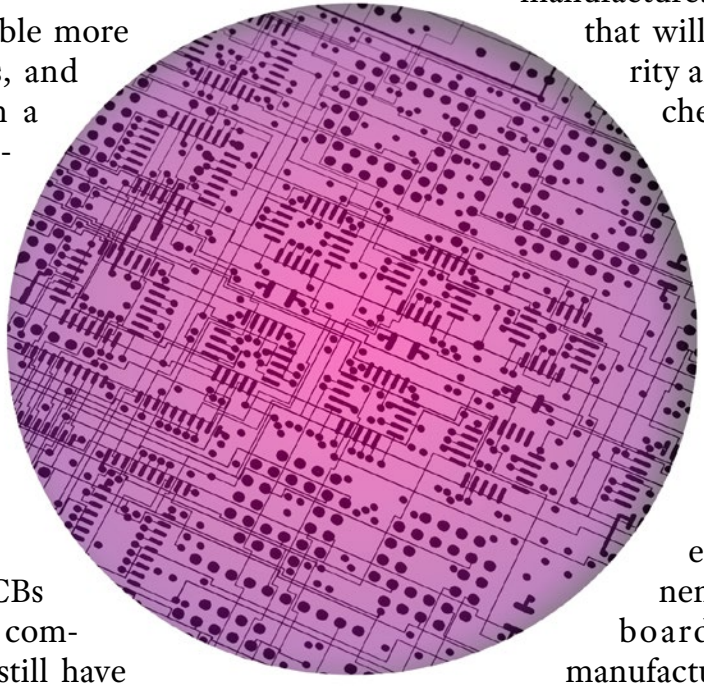
Demystifying Multilayer PCBs

Connect the Dots

by Matt Stevenson, SUNSTONE CIRCUITS

As handheld and wearable technology become vital tools for industries ranging from health services to law enforcement, innovation increasingly coincides with PCBs getting smaller. For these devices, multi-layered PCBs offer requisite functionality for boards occupying a small space.

Multilayer PCBs enable more circuitry, components, and functionality to fit in a smaller space, as compared to single-layer or double-sided PCBs. Without them, miniaturization would be much more challenging and many of our coolest projects would rapidly become too clunky and unwieldy.



Though multilayer PCBs are becoming more common, many designers still have limited experience with multilayer board design. This can make the prospect of attempting such a design seem daunting, but multilayer boards do not have to be a hassle. Just think of them as multiple single-layer boards stacked together.

Sound design processes for multilayer boards mirror that of single-layer PCBs: Choose the right CAD tool to optimize design capabilities and best support the transition from design to manufacture. Look for design tools that will confirm design integrity and perform design rule checks.

Following established best practices for design of multilayer PCBs means becoming familiar with multilayer design tips and guidelines provided by the CAD tool, gaining knowledge about tolerances and components unique to multilayer boards, and knowing the manufacturer's requirements for multilayer designs.

It is also a good idea to understand how multilayer boards are manufactured. The process, though complex, is easy to explain. Let's break

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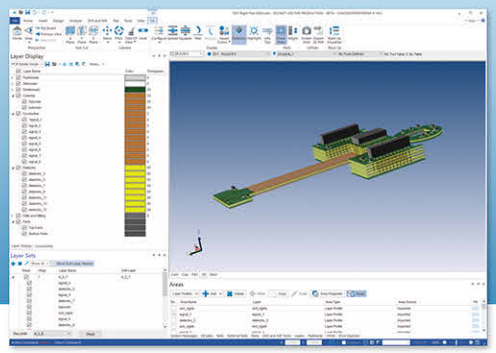

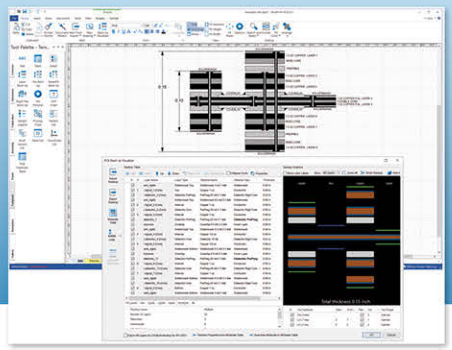

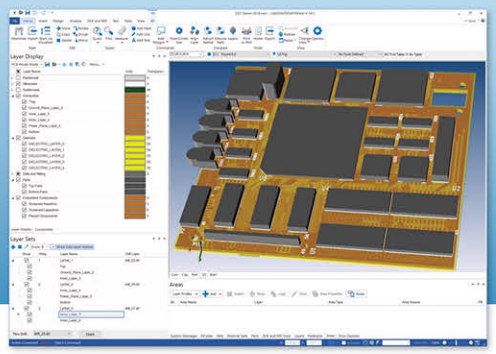

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it down into a series of easy steps by looking at the assembly of an eight-layer PCB.

1. Grouping the Layers

The internal layers are grouped into pairs. For an eight-layer build, layers 2 and 3 are paired together, as are layers 4 and 5, and layers 6 and 7. What about layers 1 and 8? As they are on the outside, they'll be added later.

2. Imaging the Layers

These pairs are imaged together onto both sides of a copper-clad laminate core, creating three distinct double-sided inner layer panels. This image is a representation of the copper image defined by the electronic data for each copper layer.

3. Etching the Images

Once the layers are all imaged, they'll be etched. Etching removes the unwanted copper cladding, which creates spaces while simultaneously defining traces and pads.

4. Inspecting the Etched Layers

After etching is complete, the layers are inspected to ensure that etched images are defect-free.

5. Preparing for Lamination

The defect-free etched layers are then prepared for the lamination process using a chemical process that roughens up the copper to make sure it bonds to the prepreg.

There are several different names for this chemical process, including oxide, black oxide, and alternative oxide, to name a few.

6. Laying Up and Pressing the Layers

Once the oxide process is finished, the inner layers of the PCB are ready to be laid up and pressed into a single panel. A multilayer layup starts with preparing the lamination book. This book contains top and bottom plates made from steel, steel pins for alignment, thermal lagging material, stainless steel shims, PTFE release sheets, and, of course, the manufacturing panels.

7. Creating the Manufacturing Panels

The manufacturing panel is created by placing copper foil onto the alignment pins followed by prepreg layers. Prepreg is short for "preimpregnated," which refers to a partially cured glass-reinforced epoxy resin in sheet form.

The prepreg has two functions. First, it bonds the external foil to the adjacent copper layer and creates the dielectric insulator

6 Layer StackUp (0.062") L06-062-1oz1oz		Thickness (inches)
Layer 1	**1 oz foil plated to approximate* thickness 0.0024"**	0.0024
Prepreg	Bonding ply (2x2116) Average Dielectric Constant 4.5	0.0084
Layer 2	**1 oz foil thickness**	0.0014
Core	Laminate Core Dielectric Constant 4.5 (+/- 0.10)	0.014
Layer 3	**1 oz foil thickness**	0.0014
Prepreg	Bonding ply (2x2116) Average Dielectric Constant 4.5	0.0084
Layer 4	**1 oz foil thickness**	0.0014
Core	Laminate Core Dielectric Constant 4.5 (+/- 0.10)	0.014
Layer 5	**1 oz foil thickness**	0.0014
Prepreg	Bonding ply (2x2116) Average Dielectric Constant 4.5	0.0084
Layer 6	**1 oz foil plated to approximate* thickness 0.0024"**	0.0024
"Thickness does not include soldermask or surface finish"		**0.0636**

between these layers. Prepreg comes in several thicknesses to help match the electrical requirements of the design.

Note that the copper foil in this step becomes the eighth layer in an eight-layer PCB design.

8. Applying the Layers

In this step, each etched and oxidized core is placed on top of the previous core's prepreg until the top layer is reached, where copper foil is applied again.

9. Assembling the Book

Finally, the completed layers are assembled into books. Depending on overall panel thickness, multiple panels can be contained within a single book. Separator sheets are placed between the panels to keep them from sticking together. In addition, shims can be added to evenly distribute pressure and maintain a consistent flatness across panels.

Thermal lagging material is generally placed between the steel plates on either end of the book and the first panel. This helps control the heat flow at a predictable rate into the manufacturing panels during lamination.

10. Pressing the Book

Finally, using heat and mechanical pressure under vacuum, the prepreg is heated up and the epoxy liquefied in order to distribute it evenly. The epoxy then cools and hardens, bonding all the layers into a single panel.

The PCB is now ready to have holes drilled into and through it, creating a finished multilayer PCB.

Designing multilayer boards will become increasingly common, and it makes sense for designers of every experience level to become more familiar with best practices. **DESIGN007**

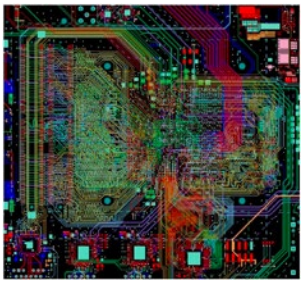
Matt Stevenson is vice president at Sunstone Circuits. To read past columns, click here.

Elementary, Mr. Watson

The Art of the PCB

by John Watson

After finishing the statue of David, Michelangelo—Italian sculptor, painter, architect, and poet of the High Renaissance—was asked how he had created such a beautiful work of art. He said, "The sculpture was already complete within the marble block before I started my work. I merely had to chisel away the superfluous material."



After decades of being in the industry and seeing countless designs, it's still amazing to see the exceptional beauty of a well-done PCB design. For designers, each PCB begins as a blank canvas; not knowing what the final product will look like, we walk a fine line between engineering and artistry, often producing fascinating results.

There is a uniqueness to every PCB design. If I gave the same schematic to 10 individuals and asked them to complete the design, I can guarantee that each designer would come up with something different. This is a result of blending each person's understanding of engineering requirements with their own touch of artistry. From the very start of a project, there is a "flow" to the circuit in the schematic. With signals, best practice is to go from left to right, from inputs to outputs. With the powers and grounds, we move from the top down to the bottom. Seeing how different people interpret this process always makes me geek out a little, because in a PCB, we can clearly see evidence of the artistic tendency. There is a stunning beauty to the multi-layered colors and the various details of connections and features, such as length tuning, impedance matching, etc. It indeed can only be described as art.

To read the rest of this column, click here.

Interview by Nolan Johnson
I-CONNECT007

Nolan Johnson recently met with Alun Morgan, technology ambassador at Ventec, and Ventec COO Mark Goodwin to discusses the industry's determination to cling to outdated processes and standards, and some potential consequences. To maintain efficiency and keep pace with the market's newest entries in Asia, Alun and Mark believe that legacy companies in the West must be open to challenging conversations that will require questioning old practices and revising those practices toward sustainability.

As Alun points out, everyone says they want change, but no one wants to lead the way.

Nolan Johnson: Would you say that there's an opportunity for innovation right now? Your options are to either stay inside old niches with low margins, or to start looking for new ways to do things. In another conversation, for example, you alluded to thermal management coatings as potential replacements for heat sinks. What other ways can you see this done differently?

Mark Goodwin: I don't have a clear answer to that, but I think we will start seeing management of scarce resources enter the supply chain discussion. People need to consider what they truly need for the performance they're looking for; there is no doubt in my mind there's a huge amount of unnecessary over-engineering happening. For example, you must start considering the scope for using a half-ounce copper foil when you're currently using one ounce, or one ounce where you're using two-ounce—those are the shifts in scope we need to be anticipating.

Alun Morgan: That's right. This is an opportunity to return to the point we've made before. It's critical to understand the end use. You need a clear understanding of both what the customers need and what they really want, then you need to link it all together. Mark, you and I have spent our careers with companies who often don't share information with us, which makes it impossible to offer them anything substantial; on the other hand, when companies share information with us, we can get them access to a fantastic supply chain offering.

Goodwin: Yes, and we've done lots of business over many years. By way of example, let's talk about an issue that's been a bugbear of ours for years. Why is laminate 1.6 mm thick? It's a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waste of glass fabric and of resin. In the old days, it had to be 1.6 mm because it needed to fit into an edge connector. When was the last time you saw an edge connector? Why is it still 1.6 mm thick? A double-sided plated through-hole board of 1.0 mm is rigid enough to support the components. Why not take out two, three, even four pieces of glass fabric?


Alun Morgan

Morgan: It comes to the need. What is the requirement? The user doesn't always know what he needs or what he can get away with. He just says, "Well, it's always been that way." You see this mindset all the time in so many different industries. The first step in designing a solution for someone is understanding what they need. Don't ask them what they need—most of the time, they don't know. They really don't, so you must ask the right questions.

My son's involved in UX—user experience—and so much of that is relevant here. He walks through that process with users. He calls it a "design safari"—pretend you're going on a safari where you must stop at each new thing, think it through, and ask, "Why do we do that?" Until you've done that, you don't know what the customer needs, and they don't know either. You must go through each stage. Once you've identified the real need, you can develop an efficient method to deliver that need.

We've seen so much waste in pursuing this, haven't we, Mark? On a few occasions, we've nailed it down and saved huge amounts of resources. If you can get everyone to be open and have that discussion, get them to genuinely share with you, you can make big gains.

Goodwin: There must be a willingness and openness to move forward, but all too often we've discovered there are too many closed minds in this business.

Morgan: Some people will design something and never change it. The design might have been right when they first did it, but then they don't change or review it, in some cases, for 20 years. This is crazy.

Johnson: We've come to a place where pricing and sustainability are such important factors because we're using copper which is in tremendous demand.

Morgan: Cost—not price—is the issue, though. We can work on the cost.

Johnson: But isn't that the motivating factor? Isn't that where you can turn around and say, "You know, we can save you money if you modify the spec to reduce the resource?"

Morgan: You would have thought so.

Goodwin: I usually hear something like, "That's great, Mark. We'll take the price, but we don't want to do the work involved with the change."

I've been in the circuit board industry since 1983 and in laminates since 1990. In my experience, there is a resistance to change. They want the savings, but they don't want to do the work. They don't want to commit to making changes. The automotive business is particularly focused on cost reduction, but also highly resistant to change. We are running out of road to get one without the other.

Morgan: We all have to work together to make this happen.

Goodwin: I'm not pointing the finger at the printed circuit board market here, either. Usually, they're constrained by somebody upstream or downstream of them. The folks telling them what to do are so far removed from how a printed circuit board or laminate is made. They have no idea what they are or aren't restricting.

Johnson: How do we get out of this?

Morgan: I want to say "education," but as important as that is, the reality is we're operating within the market. The market seems to be self-regulating, so those who are inefficient will end up being uncompetitive and will lose their business. That's the reality.


Mark Goodwin

Goodwin: What's that great presentation slide you always show about change, where people are standing on edge of the cliff?

Morgan: That slide is quite interesting. You've got a guy on a platform saying, "Who wants change?" All the hands go up, but then he asks, "Who wants to change?" Only one hand goes up. The guy presses on: "Who wants to lead the change?" At that point, the audience runs off, and that's the reality. Someone says, "We need to pay more tax," and the answer is always, "Yeah, everybody else but me should pay more tax." That's not going to cut it. We all have to do our part if we want things to change.

Sometimes I step back and reflect on how our business has evolved over the years. Back in the '50s, we had every kind of sheet size imaginable. We had all kinds of stuff going on. We were efficient because there was no other choice in those days. The reality is, in the West, we've continued with a lot of these old practices even though so many new options are available.

For example, Western laminators probably have 10 or 20 standard laminate sizes, three or four different widths of glass fabric. You go to Asia, what have you got, Mark?

Goodwin: A 50-inch width.

Morgan: And two sheet sizes. In Asia, they're efficient from the beginning. We still hold onto the inefficiencies of the old days, and we have yet to fix them.

Goodwin: The old U.S. sheet size was 36" x 48". Depending on which way around or which glass width you use to produce your prepreg, you can have 20% more or 20% less square meter output from your treater.

Morgan: Even more than 20%, by the way—as much as 30%. It's a massive change, and that leads to a better market.

Goodwin: The equipment costs are the same, the processing running costs are the same. It's just more output through better equipment utilization, so real cost benefit.

Morgan: The only reason it's done that way is because in those days, you couldn't buy glass wider than 37 inches. That was it. There was nothing available. Now, you can easily and reliably buy 50-inch.

Goodwin: For the United States, we still have to make narrow widths. We do still treat narrow width fabric because some people will not change the warp direction on their 18" x 24" polyimide panels. This, by the way, is a story that's over 30 years old.

We were trying to drive this change in 1990, swapping warp and weft around, to maximize machine utilization for us and the glass weavers, and that job is still not 100% done.

Johnson: This is something that really goes to the OEM designer, doesn't it?

Morgan: Yes, but it depends where you are in the chain. Commoditization has occurred in a lot of our sectors over the years, and if you're in a commodity business, you need to be efficient. You need to fix these things. You can get away with this for years when you're specialized, but over time, everything becomes commoditized. Even products that you feel were "specialty"

at the time end up commoditized. If you don't make those changes fast enough, you lose out to somebody who will make those changes.

We're asking people to think about these things, to look for and actually consider the most efficient solution.

Goodwin: We know that change takes time—it never happens as fast as you'd like. But if you don't start, it never happens at all.

Morgan: The solution is not to say to people at Ventec, "Please hold more stock for me because of the ongoing logistics problem." That's not a solution—that's a stop-gap measure. We need to understand the demand pattern properly. I've reached this step many times with many different customers; it's a big step for many. Some commit, and do it, and do it very successfully.

If they're like, "Just put it on the table and we'll discuss it properly," then we can get somewhere, but this is a conversation we need to keep having. Who makes these changes? Asian producers—because they think fresh and they are fresh. That kind of thinking leads to proper solutions.

Johnson: What would Ventec's portfolio of products look like if you could solve this conundrum; if you could make changes to materials, and get people to specify?

Goodwin: Starting with the scarcity of raw materials, I won't provide two-,three-, and even six-ounce copper foil on a commodity FR-4 when I've got high demand for high-end IMS materials, and high demand for military and aerospace polyimide that requires heavy coppers. I will put those raw materials on my niche specialty products.

Morgan: We'd reserve those for flagship products. Our operations in Asia are pretty optimized because we're supplying a market that understands that. The issue occurs when we're working with legacy businesses. It's very hard to find folks willing to change.

Goodwin: Interestingly, the world thinks that polyimide is a U.S. business. Yes, polyimide in circuit boards is still a very big business in the U.S., but of the five major suppliers of polyimide in the world—Ventec, AGC Nelco, Isola, EMC/Arlon and Hitachi, whichever way you want to call it—four of those five are Taiwanese- or Japanese-owned. The other is American-owned, but its most recent U.S. factory has no treaters, because you can't get environmental permits for treaters—no dirty processes in America anymore.

Morgan: That's a big Asian footprint.

Goodwin: What's American about the polyimide business, if only one of the five suppliers is American-owned—but has no treaters in its newest U.S. factory? It's predominantly an Asian owned business now, and one in that group of five became Taiwanese-owned recently; it just started production of its polyimide in Taiwan.

Morgan: It's very surprising.

Goodwin: They have a product running on a treater in Taiwan. Well, that's great; it's good for the business. But the production has got to be qualified by PCB manufacturers and OEMs, and if the doors are opening for qualification of a new production, they should be open to changing to a more cost- and resource-efficient warp direction and exchange 24" x 18" for 18" x 24".

Johnson: This industry will need to ask itself some hard questions, and we covered quite a few of them here. Gentlemen, always a pleasure speaking with you.

Morgan: Any time at all, Nolan. Great talking with you. **DESIGN007**

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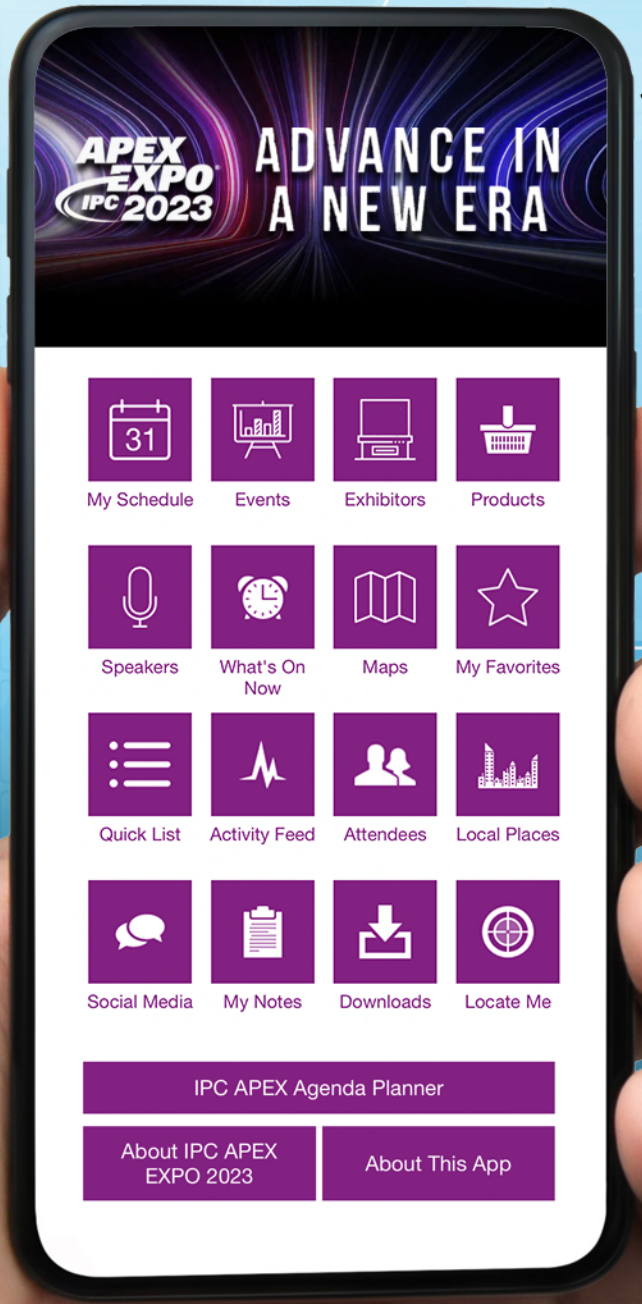

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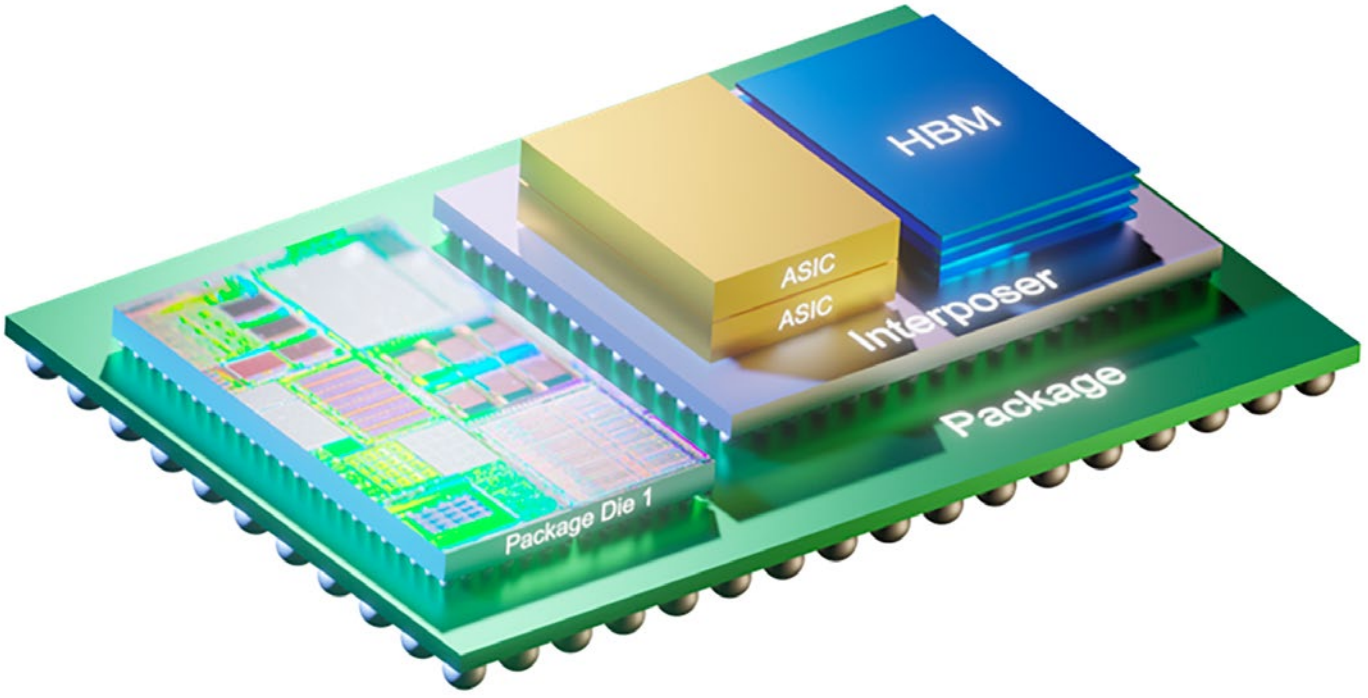

Scaling Beyond Silicon

Feature Article by Ashutosh Mauskar
CADENCE DESIGN SYSTEMS

Technology has always invoked radical changes, but unlike today, there used to be one major revolutionizing technology trend at a time. The world is becoming increasingly connected, more automated and more intelligent, driven by generational drivers—hyperscale computing, 5G, artificial intelligence and machine learning (AI/ML), industrial IoT (IIoT), and autonomous vehicles—which are invoking disruptive technological forces on vertical markets, unfolding varied levels of microelectronics and digital transformation across the globe. The increasing demand for miniaturization and higher speed is changing the dynamics of the semiconductor components needed to store and process data.

With this augmented digital effect on our lives, the electronics market opportunities—and challenges—have also accelerated. As a primary catalyst for this breakthrough, the semiconductor industry is the most vital growing segment, with a significant impact on business and society, and drawing attention from the public and government. Unlike investing the typical 10% of their revenues into CapEx, semiconductor companies are now investing more than 16%, which is higher than ever.

Governments are now focusing on the strategic significance and supply chain resilience of semiconductors, investing billions to ensure economic competitiveness and affirm their positions across the semiconductor value chain. Commercial best practices are increasingly adopted, including digital twins and co-design/co-optimization of hardware and software to ensure that systems sophistication is on par with technological advances.

The rising trend of innovative products, both household and consumer electronics that are intelligent, connected and voice-enabled, sup-

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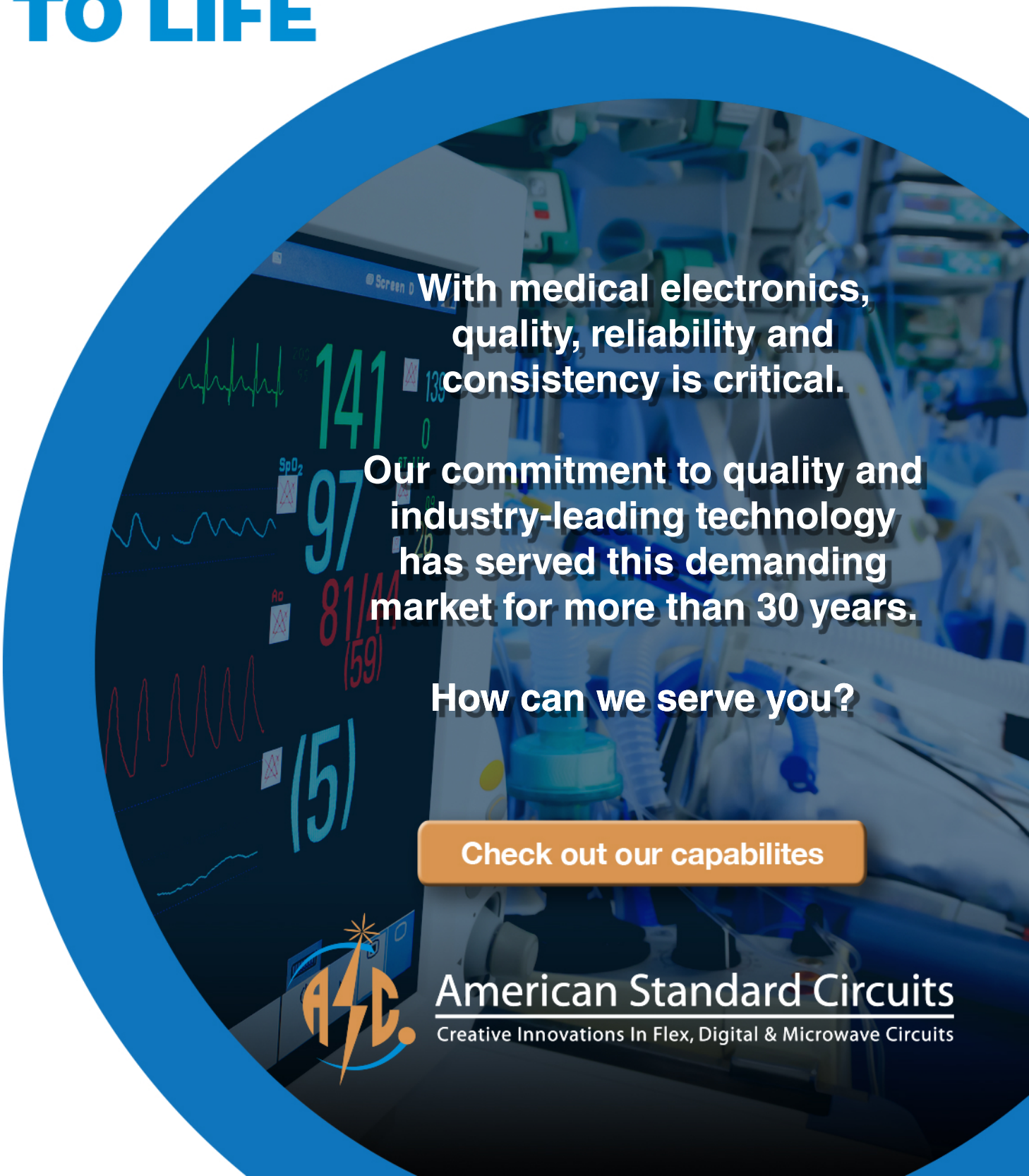

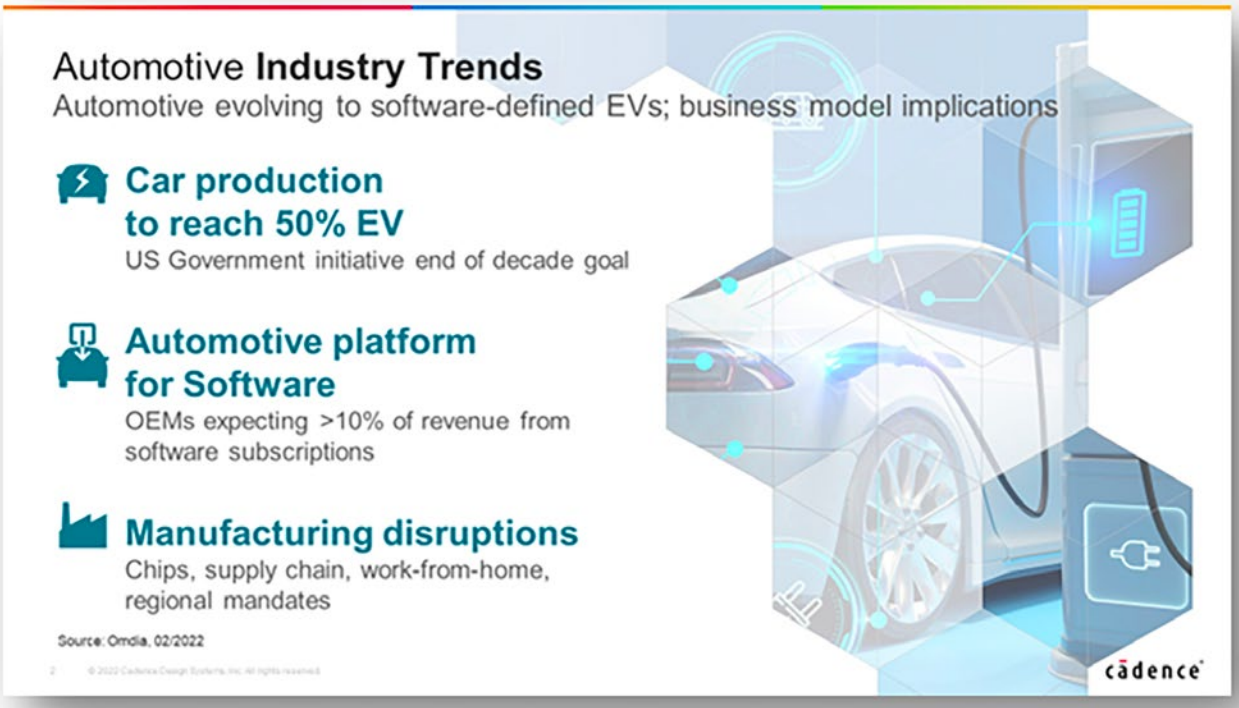

Figure 1: Automotive industry trends.

ports the proliferation globally due to its higher usage, convenience, and usability. Electronic product design companies now realize that the survival of consumer electronics depends on differentiated hardware developed simultaneously with excellent software and the ability to achieve first-pass success with advanced design solutions and methodologies. This cognizance is encouraging system companies to build their silicon.

Changing automotive trends, including the increased popularity of electric vehicles and supply chain concerns, are reshaping the industry, driving chip companies to look for system-on-chip (SoC) design efficiency and scalability. Connected cars, sensors, electrification, and new business models require integrated hardware and software to optimize cost. According to Deloitte, it is not unusual for electronics to account for 40% of the cost of a new vehicle—in 2000 it was about 15%. Internal combustion vehicles use anywhere from $500 to $700 worth of semiconductors, but electric vehicles (EVs) and hybrid vehicles use semiconductors worth thousands of dollars. To meet these rising costs, companies need to identify overlap within their automotive systems. By doing this, they can optimize product designs to handle multiple functions, reducing the overall number of chiplets in a vehicle and bringing down costs.

Moore's Law continues to advance. It provides tremendous performance, power, and area (PPA) advantages to early movers but is no longer on the equation's technological and economic side. The future holds heterogeneous architecture—the world of "more than Moore" and a new wave of expansion to embrace multi-die packaging to accommodate the changing landscape of micro- and nanoelectronics. As die size reaches the reticle limit of lithography, designing chips at the latest nodes is difficult and expensive. Low-volume businesses cannot manage the unsustainable design rate at the latest node. Also, the newest node designs need a team of specialists that are challenging to find.

The complexity and cost of advanced node design and manufacture impelled the industry to seek substitutes for the traditional mono-

Figure 2: Automotive semiconductor market trends.

lithic system-on-chip. Semiconductor packaging emerged from a conventional mechanical protective structure to a packaging that adds value and differentiation from competitors. New logical partitioning methods, manufacturing capabilities, and ecosystem dynamics are needed to target the latest advanced packaging technologies. The driving forces are heterogeneous integration, disaggregated modularized SoC, and chiplet-based design. The through-silicon vias (TSVs), fanout wafer-level packaging (FOWLP), and system-in-package (SiP) approaches as alternatives to SoCs are driving more silicon content in packages.

The transformation from monolithic silicon to multiple functional reusable chiplets (e.g., analog blocks, I/O blocks, memory, CPUs, and other IP) that can be integrated using advanced heterogeneous integration packaging technology provides a cost-effective alternative with a robust reuse model. This approach allows mixing into the design die from processes incompatible with the basic logic process, such as DRAM or RF. The yield of a given silicon area built as a huge chip was much lower than the same silicon made from several separate dies and put together with 3D packaging.

Advanced packaging has several such advantages but also presents challenges of planning, managing, and optimizing top-level design and connectivity. Moreover, the needs of IC and systems designers are converging, and the 3D ecosystem, design flow, and implementation also pose several challenges. The world of 3D-IC packaging is still maturing, and the application of chiplets is ongoing. The standards, a unified interface and toolchains are still evolving to support the design and implementation of heterogeneous packaging. Traditionally, process design kit (PDK)-based silicon design is standard in the industry. In contrast, package designs were executed with limited datasets available from the outsourced semiconductor assembly and test vendors (OSATs).

Now, as silicon becomes a system-in-heterogeneous integration, foundries are helping to drive the concept of PDKs in both silicon and the packaging world. A multi-chiplet 3D design flow is complex, and it is necessary to

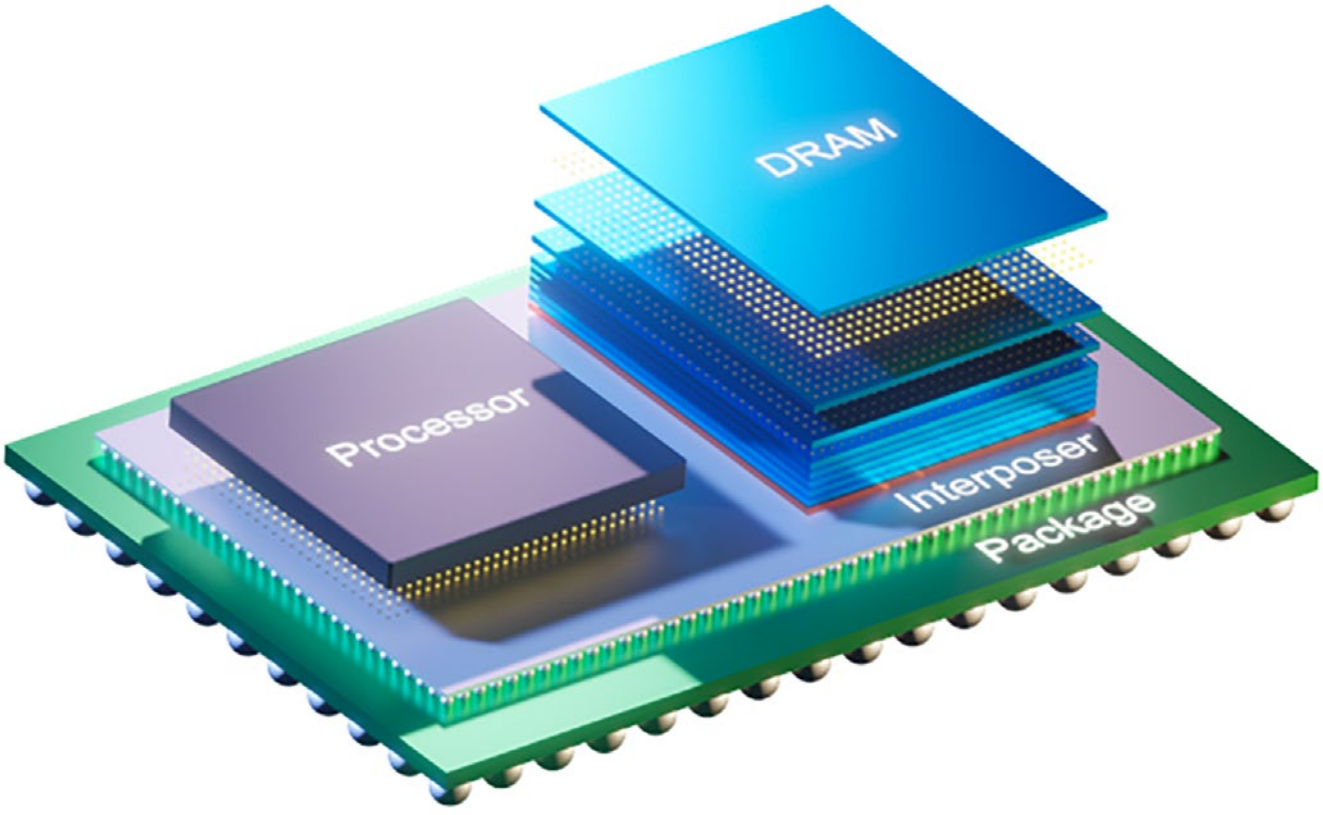

Figure 3: 3D-IC Interposer and chiplets.

improve legacy tool support in 3D integration. Design portioning between chiplets, including die-to-die (D2D) connections and managing thermal and off-package I/Os, are complex challenges. High interconnect densities are driving the transition from laminate design to silicon interposer design, making formal signoff of design rule check (DRC) and layout vs. schematic (LVS) a new requirement for package designers.

Chiplet-based systems require that the interposer and the package be designed correctly. Interposers have high-speed signals, clocks, address lanes, and data buses, which require signal and power-integrity analysis. When they are tightly packed systems, power and ground impedances impact the signal reflections, crosstalk, and simultaneous switching noise. This makes critical our integrated analysis technology, with design technology.

The industry is facing many significant challenges: technology acceleration, pandemics changing work patterns, and climate issues. However, there has never been a better time to work in the electronics industry, especially now that every segment is fusing in a metaverse. Cadence aims to strengthen its partners with more vibrant design and analysis solutions to enhance productivity and disperse creativity. We are aggressively developing new 3D-IC capabilities, molecular modeling, RF and mmWave, automotive and aero defense solutions, multiphysics analysis from IP to chip to package to board to innovative electromechanical products, and now even data centers. You can expect that AI and ML will be very much at the forefront. **DESIGN007**

Ashutosh Mauskar is vice president of product management and business development, custom IC, PCB and MSA products at Cadence Design Systems.

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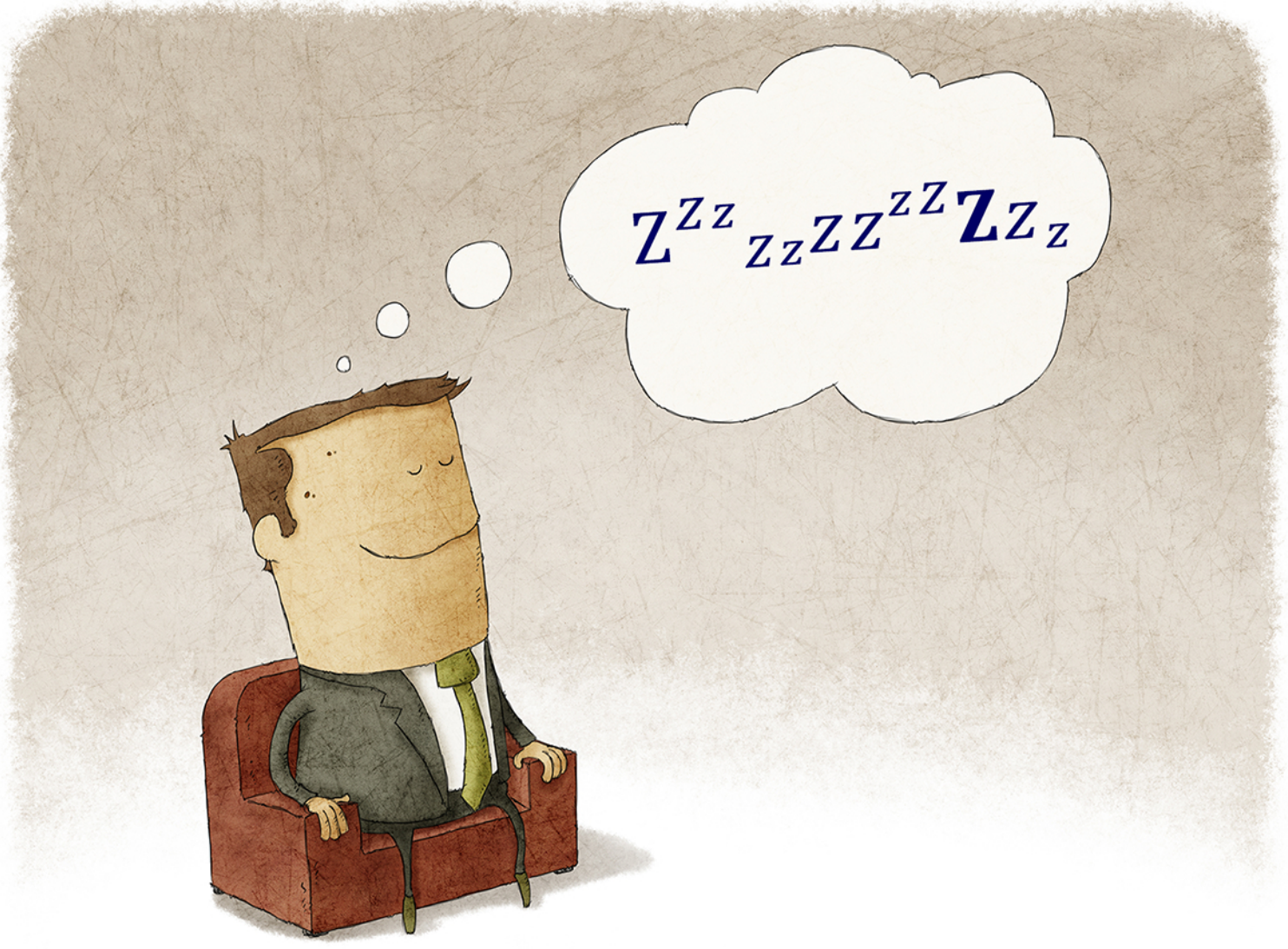

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Automotive Conformal Coating Applications

Sensible Design

by Saskia Hogan, ELECTROLUBE

Conformal coatings are all around us. The benefits they offer are discreet but intensely purposeful, as they protect electronic circuitry against harsh environments and help to extend the reliability and lifetime of our devices. We can find conformal coatings in household appliances, white goods, and other electronics in and around our homes, as well as in our workspaces, in manufacturing, and other industrial applications.

With a surge in connectivity adoption via IoT, smart cities, and smart infrastructure networks, the need to protect electronics in different devices is becoming increasingly important. As dependence on devices increases, protecting the security and physicality of electronics is of significant interest to many. This is where conformal coatings can make such a big difference. Protection of electronics is particularly important in the the automotive industry, with the range of advanced driver assistance systems (ADAS) and electric vehicles currently available.

In this column, I will discuss how conformal coatings can make a difference in electric and hybrid vehicles, as well as other automotive applications, areas where we have seen a vast increase in demand for conformal coatings.

A Need for Coatings

Coatings are used extensively in diesel and petrol vehicles. Will there be as much of a need for coatings in hybrid or electric vehicles?

The rapid adoption of EVs and ADAS, autonomous driving, and the vast increase in infotainment solutions in vehicles has created enormous demands on the electronics involved in these vehicles. At the same time, the requirements for conformal coatings are rising. One target, to increase the range per charge of an

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electric vehicle, is to make the vehicle as light as possible. Electronic design engineers are feeling the pressure to minimize their electronics through a finer pitch on the board. In ADAS, as well as other applications, the tolerance to failures is extremely low, which means the electronics on the board will require a high level of protection against environmental influences like humidity, condensation, thermal changes, corrosive gases, and other contaminants. But not only is it important to protect the electronics against the environment, it is also necessary to insulate the different components on the board from each other. A high dielectric strength material, capable of resisting a greater voltage before it breaks down, is of crucial importance.

A high dielectric strength material, capable of resisting a greater voltage before it breaks down, is of crucial importance.

Conformal coatings can deliver on these challenges. Not only do they provide a strong protective barrier to the outside world, but they also deliver on the insulation resistance that is required to allow a finer component pitch on the board. All this provides a high level of protection in a lightweight solution.

There is a huge need for conformal coatings in hybrid and electric vehicles, but these applications also have very strict requirements, which means there is also much more pressure to get things right.

Typical Applications

What are some of the typical applications for coatings within the automotive industry?

The potential applications for conformal coatings are almost limitless. Wherever there's an electronic circuit board that needs lightweight protection, a conformal coating can be an ideal solution. Coating applications in automotive can be in sensors used in ADAS and other supporting applications. Examples of this include the ADAS control unit PCB or powertrain applications, like the battery management system PCB, charger PCB, inverter, DC/DC converter, and transmission switches, just to name a few. Also, there's a requirement for coatings to protect electronics in the vehicle infotainment system, alongside external and interior lighting, climate control systems, and other electric controls. There are many more applications for electronics in vehicles; the list seems endless

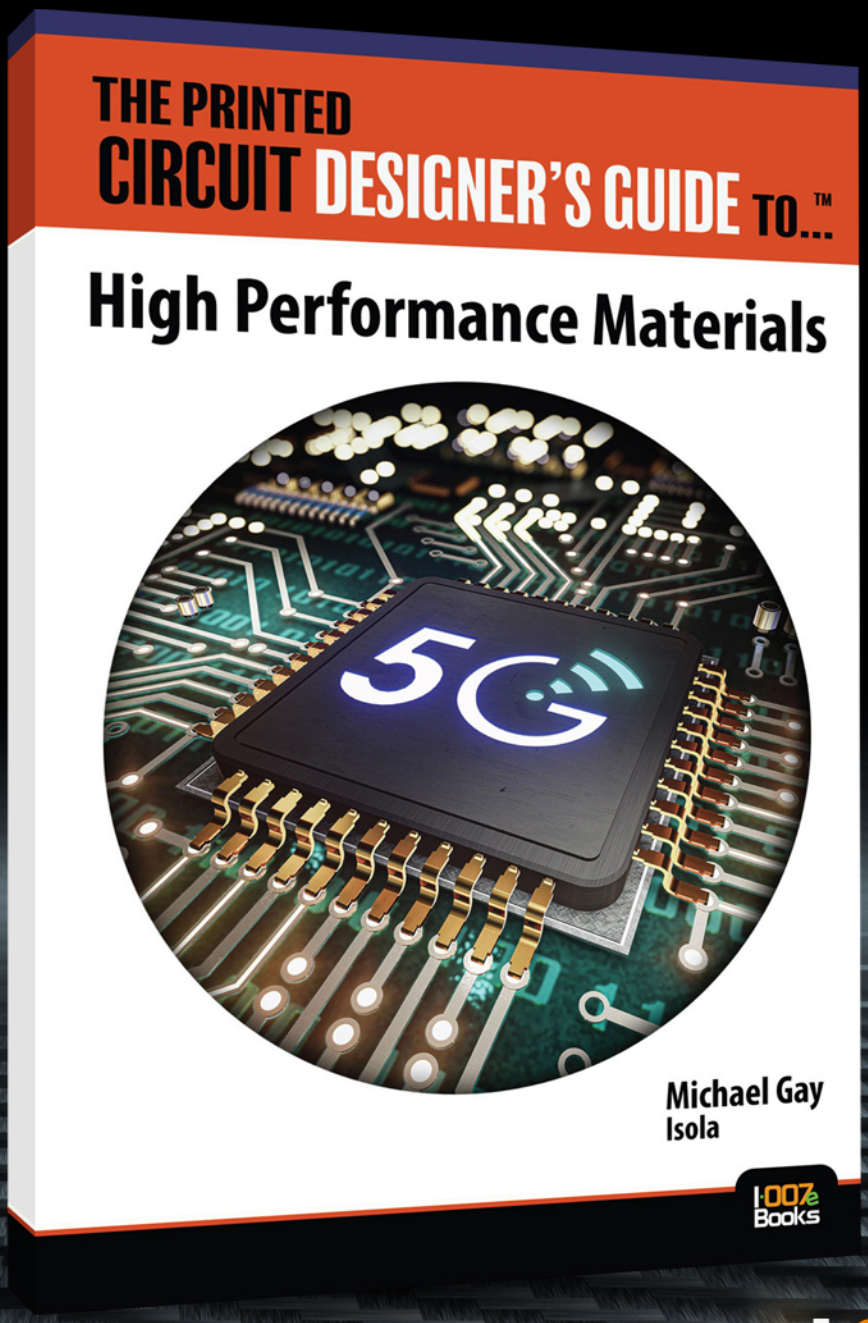
For instance, if we move away from the vehicle itself to the charging infrastructure, we are faced with charging stations that are exposed to all weathers: heat, cold, humidity, and corrosive environments—especially near coastlines. If we look at the need for a reliable network of charging points that enables EV drivers to charge their vehicles, we must include the electronics in the charging point in our list of potential applications for conformal coatings.

Bio-based coatings, especially those with a higher content of raw materials from sustainable sources, have shown to perform well in future-proofing the conformal coatings process in EV and automotive applications. Lighter-weight coatings that meet the sustainability requirements of manufacturers and end users have shown improved condensation resistance, thermal stability, flexibility, and adhesion compared to many petrochemical-derived polymers. **DESIGN007**

Saskia Hogan is global product manager, conformal coatings, at Electrolube. To read past columns from Electrolube, click here. Download your free copy of Electrolube's book, *The Printed Circuit Assembler's Guide to... Conformal Coatings for Harsh Environments,* and watch the micro webinar series "Coatings Uncoated!"

Choose wisely.

With today's material performance requirements, it's more important than ever to understand and choose your materials wisely.



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DFM 101
Final Finishes: HASL

Article by Anaya Vardya
AMERICAN STANDARD CIRCUITS

Introduction

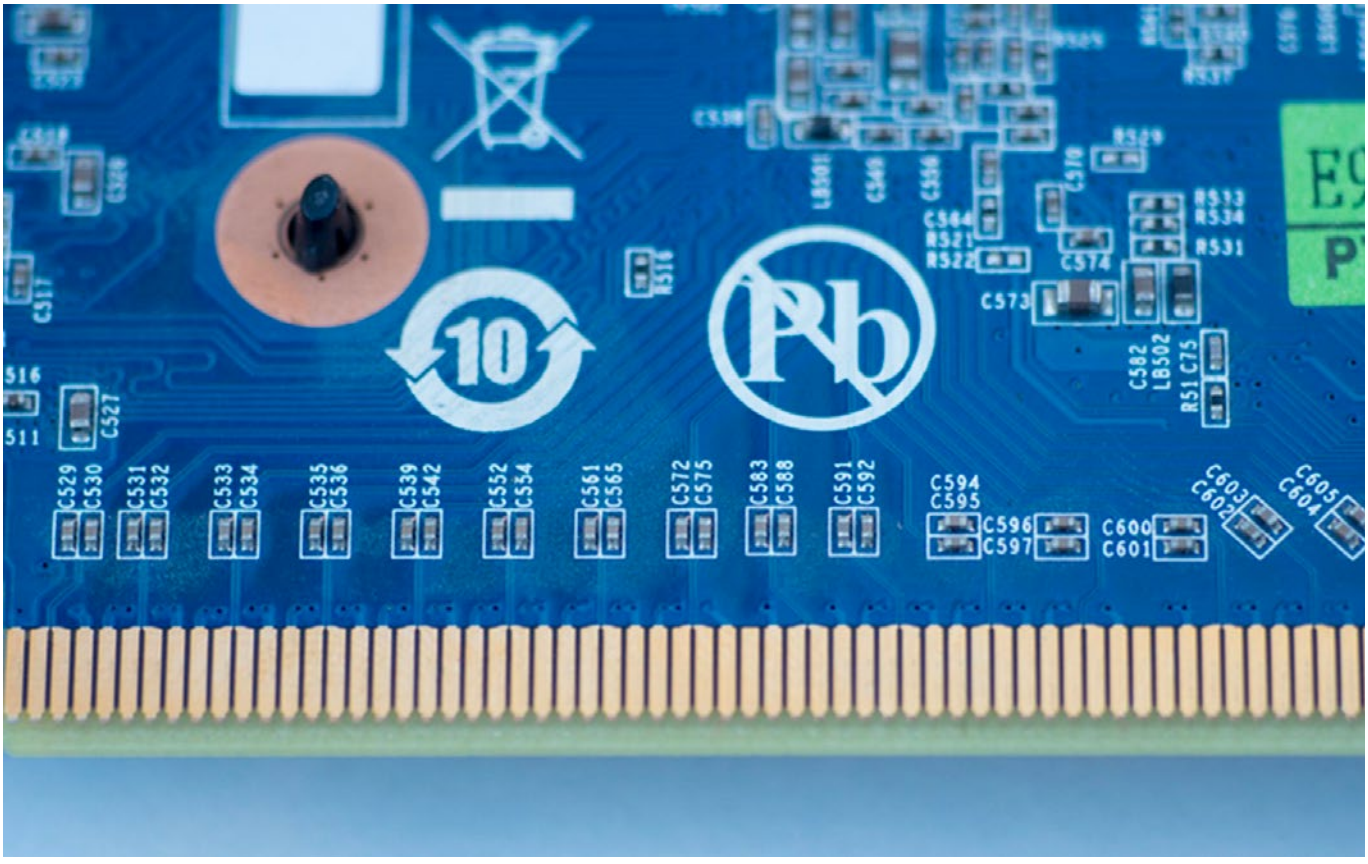
One of the biggest challenges facing PCB designers is not understanding the cost drivers in the PCB manufacturing process. This article is the latest in a series that will discuss these cost drivers (from the PCB manufacturer's perspective) and the design decisions that will impact product reliability.

Final Finishes

Final finishes provide a surface for the component assembler to solder, wire bond, or conductively attach a component pad or lead to a pad, hole, or area of a PCB. The other use for a final finish is to provide a known contact resistance and life cycle for connectors, keys, or switches. The primary purpose of a final finish is to create electrical and thermal continuity with a surface of the PCB.

HASL (Hot Air Solder Leveling)

The next finish to discuss in this series is HASL. Choosing a surface finish means weighing the pros and cons associated with each, typically a combination of application, cost, and the properties of the finish. For example,



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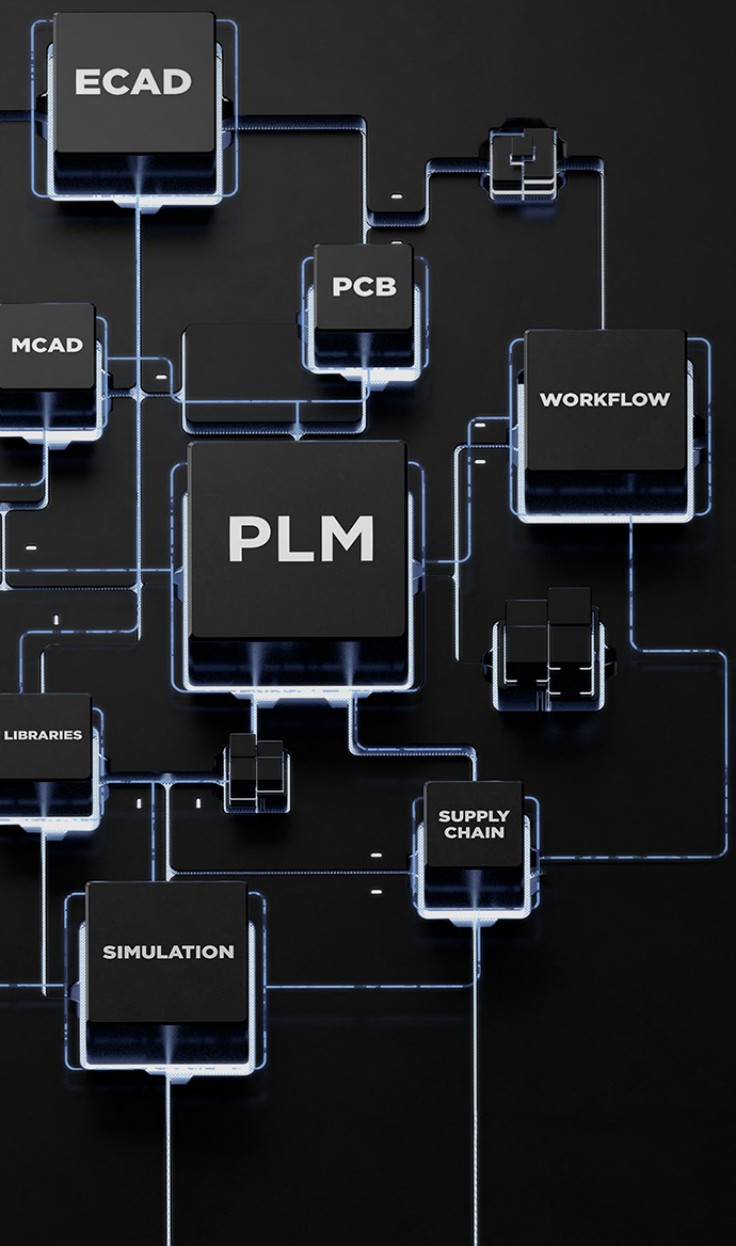

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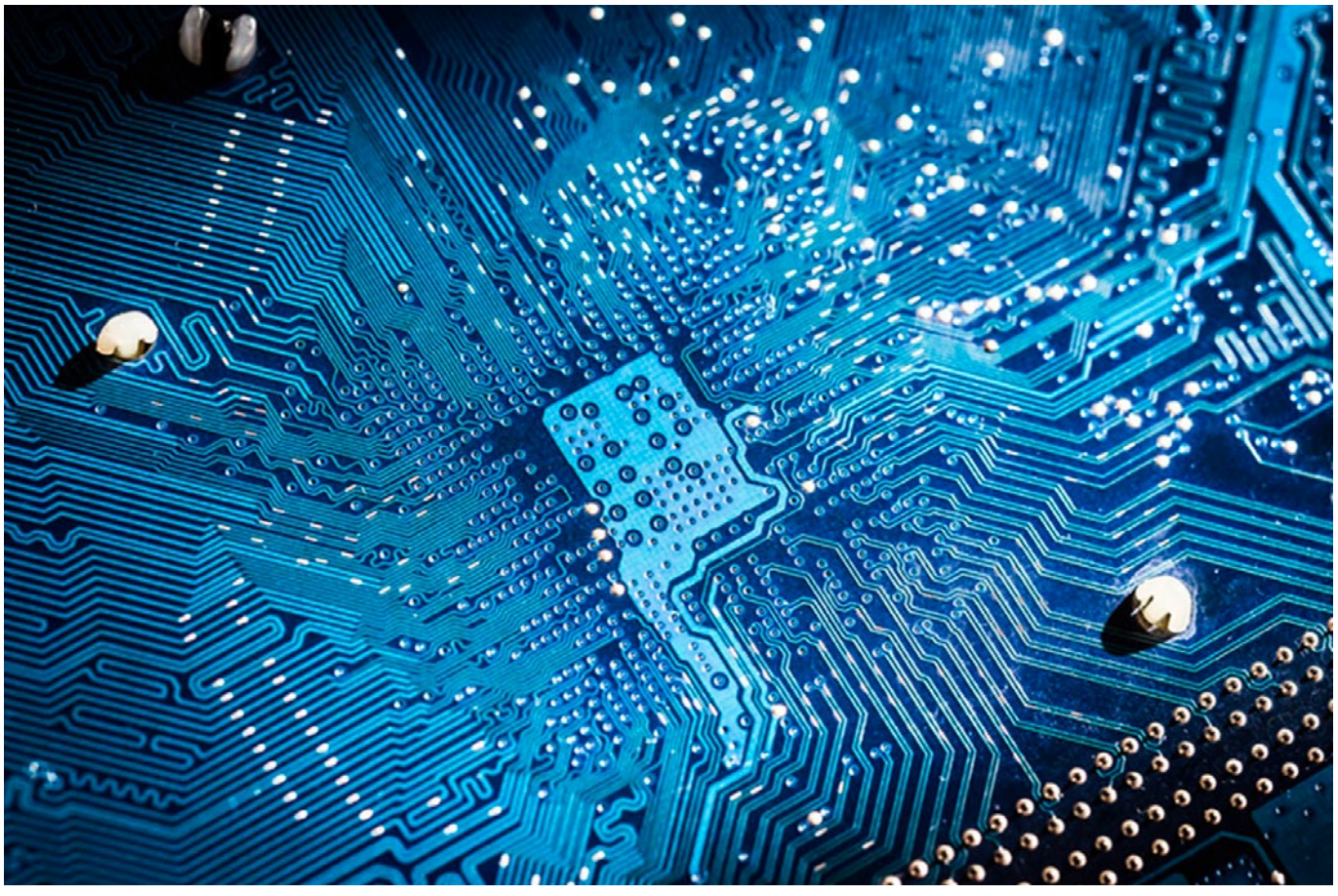


Lead-free HASL is considered "RoHS" compliant (< 0.1% BW of finish, for Pb, Hg or Cd), while SnPb (tin/lead) HASL is not.

HASL is available in two versions: a tin/lead alloy and a lead-free option. HASL is a variable thickness metal alloy coating, typically 25 to 2000 µin [0.65 to 50 µm] thick, designed to create a solderable surface and to maintain solderability over an extended period. Using specialized equipment, panels with exposed copper (pads and/or traces) are inserted into a vat of molten solder. A series of compressed hot-air knives then remove excess solder and "level" the surface before the solder solidifies and cools. HASL is the most prevalent and most solderable finish. Boards that have been HASL leveled will have a bright, silvery pad coloration. Solder thickness and uniformity on SMD pads is a function of pad size, pad orientation during processing, and HASL equipment. As pad size increases, thickness and uniformity decrease. This is caused by the high surface tension of solder and the airflow over pads that remove excess solder. Small pads (0.025" pitch SMD) will have a more uniform solder coating than large pads (0.050" x 0.050"). Large pads may be partially covered with a mound of solder while the rest of the pad is thin eutectic solder. Small pads may have the same condition depending on pad orientation during processing.

Pad orientation also contributes to solder thickness and uniformity. Fine-pitch SMD pads perpendicular to the direction of processing will have a uniform solder coating covering the entire pad. Fine-pitch SMD pads that are parallel to the direction of processing will have the leading half reduced to the thin eutectic solder with a mound of solder on the trailing half (eutectic solder is the optimum metal alloy to maximize solderability). Angled processing exposes both pad directions to similar air blasts resulting in more consistent pad thickness for similar pad sizes. 45-degree angle pro-

cessing minimizes the pad orientation difference. HASL is not used for fine pitch components. This is because it increases fabrication and assembly rework for boards that have fine-pitch SMT devices with lead centers below 0.020" and presents coplanarity issues.

Pros and Cons of HASL

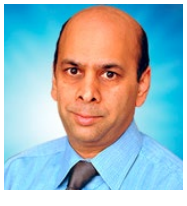
Pros

- Economical and widely available
- Excellent solderability
- Can be reworked at the fabricator
- Presents a very flat solder deposit

Cons

- Limited assembly reflow cycles, as the HASL process introduces a thermal shock before it gets to assembly
- Not suited for fine pitch (due to uneven surface height) or high aspect through-holes
- Standard SnPb HASL is not RoHS compliant
- Lead-free HASL requires different assembly soldering parameters

Understanding the cost drivers in PCB fabrication and early engagement between the designer and the fabricator are crucial elements that lead to cost-effective design success. Following your fabricator's DFM guidelines is the first place to start. **DESIGN007**



Anaya Vardya is president and CEO of American Standard Circuits; co-author of *The Printed Circuit Designer's Guide to... Fundamentals of RF/Microwave PCBs* and *The Printed Circuit Designer's Guide to... Flex and Rigid-Flex Fundamentals;* and author of *The Printed Circuit Designer's Guide to... Thermal Management: A Fabricator's Perspective.* Visit I-007eBooks.com to download these and other educational titles. He also co-authored "Fundamentals of Printed Circuit Board Technologies" and provides a discussion of flex and rigid flex PCBs at Real Time with... American Standard Circuits.

PCB Designer Dave Graves Passes Away

David N. Graves, 65, passed away December 22, 2022. He worked with several firms, starting in 1974, and helped found UltraCAD Design Inc. in 1992. Twenty years later he joined Monsoon Solutions, Inc. where he spent the rest of his career before retiring in 2021.

Dave was a superb designer, a patient mentor to colleagues and customers alike, and was well respected by everyone. He was inducted into the Top Gun Hall of Fame in March 2001, during the PCB Design Conference, West.

(Source: Douglas G. Brooks, PhD)

Flex007 Highlights

Web vs. Direct Imaging ▸

As flexible printed circuits continue making waves in PCB manufacturing, the Altix team looks at today's use cases for FPCs and explores trending topics and what it means for PCB manufacturers.

PCB Technologies Acquires Galil Microwaves & Microelectronics Ltd. ▸

PCB Technologies is proud to announce that the company has acquired the technology and the business activity of Galil Microwaves & Microelectronics Ltd.

Global Flexible PCB Market Report 2022: Rising Use in the Aerospace and Aviation Sector Boosts Growth ▸

According to official industrial sources, around 1.5 billion smartphones were sold in the year 2019, due to the rise in disposable income and increasing mobile data connectivity.

Compeq October Revenue Jumps 30.6% ▸

Compeq Manufacturing Co. Ltd, a Taiwan-based manufacturer of HDI, rigid-flex PCBs, and flex PCBs, has posted unaudited net sales of NT$7.8 billion ($253.1 million at $1:NT$30.96) for October 2022, up by 30.6% year-on-year (YoY) and by 2.9% month-on-month.

NextFlex Announces Over $8 Million in Funding for Flexible Hybrid Electronics Innovations ▸

NextFlex, America's Flexible Hybrid Electronics Manufacturing Institute, announced $8.45 million in funding (including $4.25M in cost-share contribution from participants) for nine new projects as part of its Project Call 7.0 to further promote FHE development and adoption throughout the U.S. advanced manufacturing sector.

IDTechEx Asks, What 2023 Holds for Printed/Flexible Electronics ▸

With applications ranging from energy harvesting to sensing, and applicability to sectors being as varied as healthcare and automotive, printed/flexible electronics are set to change expectations of what electronics can provide and where they can be utilized.

Zhen Ding October Revenue Up 30% YoY ▸

Taiwan-based Zhen Ding Technology Holding Ltd has posted sales of NT$21.19 billion ($691.87 million at $1:NT$30.63) for October 2022, up by 29.9% year-on-year (YoY) and by 4.5% from the previous month.

Flexible PCB Market to Record $15.76 Billion Growth ▸

The Flexible Printed Circuit Board market will register an incremental spend of about US$15.76 billion, growing at a CAGR of 10.32% during the five-year forecast period.

Flexible Electronics Spark PhD Student's Interest ▸

A Binghamton University doctoral student aims to make innovative technology more accessible through the use of flexible hybrid electronics.

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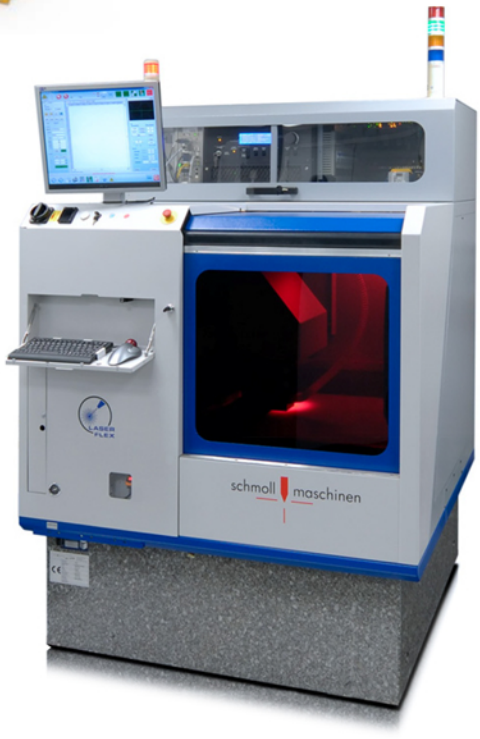

Typical applications:

- Polymer cover foil
- Covered polymer laminates
- Thin, rigid-flex materials
- Inner layers and prepregs
- Separation or decap from tracks
- Structuring cavities
- Microvia and through-hole drilling

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A Patently Innovative Revolution

Flexible Thinking

by Joe Fjelstad, VERDANT ELECTRONICS

The month of January is named for the Roman god Janus, a two-faced deity whose role is to watch over doorways, the comings and goings of individuals, and the passage of time. In January, individuals often make resolutions to themselves; though following through on these resolutions may be short-lived, a new year often prompts us to be mindful of the need to make some improvements in our lives—whether personal or professional. One of the best ways to look forward is, like Janus, to simultaneously look backward. For technologists of every stripe, one of the best places to look back on is the U.S. Patent and Trademark Office (USPTO).

The patent office is a great place to get an understanding of the kinds of useful ideas that may shape our technological future. We generally think of patents as a means to protect intellectual property, but patents can be a valuable tool in divining what's to come. As many of us lack a full appreciation of the history of patents, this article aims to provide a brief history and some personal comments and observations on this important topic.

In the broadest terms, the patent office has been the nation's repository for millions of inspirations, insights, and all our inventors' "Eureka!" and "A-ha!" moments since the founding of the United States of America. The USPTO records and memorializes all the inventions born from those special moments of discovery, allowing everyone in the world to see and learn from them.

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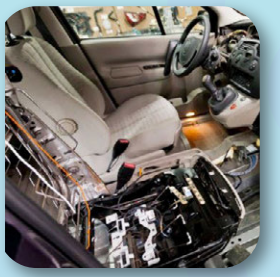
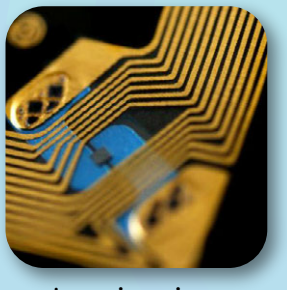


Automotive Electronics



Lamination

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The patent system is among the most important gifts that the Founding Fathers left us in the U.S. Constitution, specifically in Article 1 Section 8, which contains the deceptively simple Clause 8: "[The Congress shall have Power] To promote the Progress of Science and useful Arts, by securing for limited Times to Authors and Inventors the exclusive Right to their respective Writings and Discoveries."

From those few words enshrined in the Constitution, it is evident that they understood the importance of innovation to the success of the nation. Note that the statement does not use the term "patent" but instead uses the term "*right* to their respective writings and discoveries." The idea of issuing patents came to America by way of the Old World; the term traces its roots back to England's Statute of Monopolies of 1624, which endowed inventors with the sole rights to their inventions for a period of 14 years.

The Founders clearly knew that granting such rights would be important to the growth and improvement of the nation; they also recognized that by granting inventors limited monopoly over their ideas for a period, inventors would be more open to sharing ideas and discoveries that would help build that nation. Since its founding, the United States and its laws have protected and encouraged innovation.

Since its founding, the United States and its laws have protected and encouraged innovation.

The concept of the patent is now universally embraced at every level of business, at least intellectually if not always in practice. Today, while a great many countries have their own patent systems, the international Patent Cooperation Treaty (PCT) of 1970 provides a unified procedure for filing patent applications to protect inventions from member countries. A patent application filed under the PCT is referred to as an "international application," though PCT filing does not lead to the granting of an international patent, as one must still file separately for a patent in each nation where protection is sought.

When it comes to patents, there has been an effort to "make things simpler," but as we all know implementing such policies in bureaucracies can be challenging. Moreover, the "Rule of Law" is not always equally applied. In recent years, illegal expropriation of intellectual property has become a major concern, which is very unfortunate and undermines the intention and purpose of patent grants.

It is a sad reality that the global patent system is not in great shape. Many countries have attempted to collaborate to make a more useful and enforceable system, but concerns over commerce and competitiveness have caused many business leaders to turn a blind eye to patents—especially among newer members of the international business community, where the idea of intellectual property is not given much weight.

The more cynical folks in most industries commonly assume that a patent is of no value until it is tested in court and backed by the weight and force of governments that have the power to restrict trade. This must delight litigators around the globe, since they seem to make their greatest personal gains from conflict; they are always assured a "win," no matter what the outcome is for their client. As many haggard veteran inventors have observed: If you think getting a patent is expensive, try defending one.

Lest the reader be left in a dark mood at the beginning of a new year, it is important to remember that at a fundamental level, the basic idea of the patent is still a good one. If a patent causes one new good idea to enter circulation, then the process is worth it. There will never be a need to shut down the patent

office as it was reportedly suggested by U.S. Commissioner of Patents, Charles H. Duell, in 1899, because "everything that can be invented has been invented." At the time, about 700,000 patents had been issued; today, roughly 11.5 million patents exist, and the number of applications is growing. We will collectively negotiate our way through the current controversy, but even if patents were to disappear, inventors would continue to invent, as it is an integral part of our human nature.

Enjoy the new year; get out there and invent.

DESIGN007

Joe Fjelstad is founder and CEO of Verdant Electronics and an international authority and innovator in the field of electronic interconnection and packaging technologies with more than 185 patents issued or pending. To read past columns or contact Fjelstad, click here. Download your copy of Fjelstad's book *Flexible Circuit Technology, 4th Edition,* and watch his in-depth workshop series "Flexible Circuit Technology."

A Greener Internet of Things With No Wires Attached

Emerging forms of thin-film device technologies that rely on alternative semiconductor materials, such as printable organics, nanocarbon allotropes and metal oxides, could contribute to a more economically and environmentally sustainable internet of things (IoT), a KAUST-led international team suggests.

The IoT is set to have a major impact on daily life and many industries. It connects and facilitates data exchange between a multitude of smart objects of various shape and size—such as remote-controlled home security systems, self-driving cars equipped with sensors that detect obstacles on the road, and temperature-controlled factory equipment—over the internet and other sensing and communications networks. Also, the current global production of lithium for battery materials may not keep up with the increasing energy demand from the swelling number of sensors.

Wirelessly powered sensor nodes could help achieve a sustainable IoT by drawing energy from the environment using so-called energy harvesters, such as photovoltaic cells and radio-frequency (RF) energy harvesters, among other technologies. Large-area electronics could be key in enabling these power sources.

KAUST alumni Kalaivanan Loganathan, with Thomas Anthopoulos and coworkers, assessed the viability of various large-area electronic technologies and their potential to deliver ecofriendly, wirelessly powered IoT sensors.

Over the years, Anthopoulos' team has developed a range of RF electronic components, including metal-oxide and organic polymer-based semiconductor devices known as Schottky diodes. "These devices are crucial components in wireless energy harvesters and ultimately dictate the performance and cost of the sensor nodes," Loganathan says.

Key contributions from the KAUST team include scalable methods for manufacturing RF diodes to harvest energy reaching the 5G/6G frequency range. "Such technologies provide the needed building blocks toward a more sustainable way to power the billions of sensor nodes in the near future," Anthopoulos says. (Source: KAUST)

TOP TEN EDITOR'S PICKS

Sensible Design: Encapsulation Resins—PU vs. Epoxy

Most resin systems in use today are extremely complex products with elaborate chemical formulations. Process characteristics and final properties are usually adjusted by the manufacturer to suit the customer's requirements, yet resin technology is often overlooked.

Digital Transformation: Leveraging Digital Automation to Accelerate PCB Design

I see digital automation as the simplification of manual tasks that have been optimized in the digital world to a point where they require the least amount of effort to successfully do what they are required to do in the real world.

Beyond Design: Forget What You Were Taught

Ralph Morrison was a physicist who promoted the belief that electromagnetic energy flows in spaces, not the traces. That energy does not flow in the copper traces of a PCB, but rather the energy follows the traces acting as a waveguide and propagates through the dielectric material.

The Test Connection: Spreading the Word About DFT

Bert Horner

As signal speeds continue to increase and feature sizes decrease, PCB designers are beginning to pay greater attention to test and design for test (DFT) strategies. Bert Horner, president of The Test Connection in Hunt Valley, Maryland, is spearheading this drive to show designers the benefits of a solid DFT plan, as well as the downside of not having a test strategy.

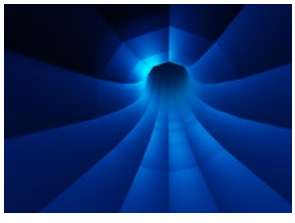
Dana on Data: PCB Data Transfer Non-evolution

The PCB industry still sends scanned copies of paper documents, which I have termed "ePaper," back and forth to each other; this process requires humans to interpret the information on the electronic copy of a document before manually entering it into a computer. So much for the concept of continuous improvement.

Physics, Electrical Engineering, and PCB Design

When I was a sophomore in college, I had an amazing professor for Physics II: Electricity and Magnetism. He made a series of complex topics fun to learn, and his personality and way of teaching were almost tailor-made for the way I like to learn. However, I did find myself wondering, "Will I ever use any physics in real life?" It turns out that the answer to the question was yes.

Electronics vs. Physics: Why Vias Don't Get Hot



The resistance of a copper trace is mostly determined by its geometry (cross-sectional area), and there are lots of studies trying to look at the relationship between the current down a trace (of known size) and the resulting temperature of the trace. But the situation is much more complicated than this.

Connect the Dots: Managing Solder for Fewer Heat Sink Failures

Heat sink failures can be difficult to detect, especially when the failure rates are low. But even if the volume of failures is low, those costs quickly run into thousands of dollars.

A New Gathering Place for Designers

IPC APEX EXPO started out as a show for the PCB manufacturing community, but it's grown beyond that. This year, there's more design curriculum at the show than ever before. IPC instructor Kris Moyer has been instrumental in leading the organization's efforts around PCB design and design engineering curriculum. So, I asked him the million-dollar question.

E-mobility a Driver of Topics at IPC APEX EXPO

E-mobility is a challenging new paradigm for electronics design. Regardless of industry, automotive, two-wheeler, vertical takeoff, and landing (VTOL), rail, or marine, e-mobility presents new challenges that the electronics supply chain is working together to resolve.

Career Opportunities

Find industry-experienced candidates at jobConnect007.

For just $750, your 200-word, full-column ad will appear in the Career Opportunities section of all three of our monthly magazines, reaching circuit board designers, fabricators, assemblers, OEMs, suppliers and the academic community.

In addition, your ad will:

- be featured in at least one of our newsletters
- appear on our jobConnect007.com board, which is promoted in every newsletter
- appear in our monthly Careers Guide, emailed to 26,000 potential candidates

Potential candidates can click on your ad and submit a resume directly to the email address you provide, or be directed to the URL of your choice.

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Career Opportunities

CHEMCUT

Technical Sales Manager

Objectives

Provide sales leadership and management for a regional sales territory. Responsible for retaining current customers as well as developing and attracting new customers and markets. Responsible for selling current and new products, keeping abreast of new technologies, market trends, and customer product needs.

Essential Functions and Responsibilities

- Develop and service assigned geographic region
- Actively and consistently seek new customers
- Visit customers and potential customers to develop relationships, deliver sales presentations, follow up on leads, and close sales
- Provide technical support and product recommendations in person, by email, and phone
- Manage major accounts; establish long-term, ongoing relationships with key individuals
- Provide feedback to Chemcut as well as sales peers regarding competition, pricing, and marketing opportunities

Qualifications

- Bachelor's degree in mechanical, electrical, chemical engineering or related fields
- 3-5 years of field sales experience with technology driven industrial products
- Well-developed sales and customer relations skills
- Ability to make decisions and evaluations to determine customer needs
- Ability to travel up to 50% of the time
- Excellent oral and written communication skills
- Knowledge of target market industries

To apply, please submit a cover letter and resume to hr@chemcut.net.

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Prototron Circuits

Sales Representatives

Prototron Circuits, a market-leading, quick-turn PCB manufacturer located in Tucson, AZ, is looking for sales representatives for the Utah/Colorado, and Northern California territories. With 35+ years of experience, our PCB manufacturing capabilities reach far beyond that of your typical fabricator.

Reasons you should work with Prototron:

- Solid reputation for on-time delivery (98+% on-time)
- Capacity for growth
- Excellent quality
- Production quality quick-turn services in as little as 24 hours
- 5-day standard lead time
- RF/microwave and special materials
- AS9100D
- MIL-PRF- 31032
- ITAR
- Global sourcing option (Taiwan)
- Engineering consultation, impedance modeling
- Completely customer focused team

Interested? Please contact Russ Adams at (206) 351-0281 or russa@prototron.com.

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Career Opportunities

Test Engineer, Electronics Engineer

Keytronic is a dynamic, team-based contract manufacturer with facilities worldwide. Innovation defines us. Come join us in Spokane, Washington! We invite you to bring your engineering expertise and passion for excellence. In turn, we provide meaningful opportunities for you to implement these attributes to their fullest while working together to bring our customer's high-tech automotive, aerospace, medical and commercial products to full production.

We encourage you to apply to one of our open positions below if you enjoy being challenged, working in a dynamic work setting and being a part of a team creating products to improve our world.

- **Test Engineer**—You will assist in conducting electrical test engineering support involving automation, assembly, maintenance, and data collection.

- **Electronics Engineer**—You will work on a team creating electronic circuitry, writing firmware for microprocessors and interfacing with customer development teams producing a wide array of products.

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Regional Manager
Midwest Region

General Summary: Manages sales of the company's products and services, Electronics and Industrial, within the Carolinas and Mid-Atlantic Region. Reports directly to Americas Manager. Collaborates with the Americas Manager to ensure consistent, profitable growth in sales revenues through positive planning, deployment and management of sales reps. Identifies objectives, strategies and action plans to improve short- and long-term sales and earnings for all product lines.

DETAILS OF FUNCTION:
- Develops and maintains strategic partner relationships
- Manages and develops sales reps:
  - Reviews progress of sales performance
  - Provides quarterly results assessments of sales reps' performance
  - Works with sales reps to identify and contact decision-makers
  - Setting growth targets for sales reps
  - Educates sales reps by conducting programs/seminars in the needed areas of knowledge
- Collects customer feedback and market research (products and competitors)
- Coordinates with other company departments to provide superior customer service

QUALIFICATIONS:
- 5-7+ years of related experience in the manufacturing sector or equivalent combination of formal education and experience
- Excellent oral and written communication skills
- Business-to-business sales experience a plus
- Good working knowledge of Microsoft Office Suite and common smart phone apps
- Valid driver's license
- 75-80% regional travel required

To apply, please submit a COVER LETTER and RESUME to: Fernando Rueda, Americas Manager

fernando_rueda@kyzen.com

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Career Opportunities

TAIYO AMERICA

Formulating Chemist

Taiyo is the world leader in solder mask products and has extensive worldwide R&D resources to further offerings that include the latest in inkjet technology, specialty dielectric inks and via filling inks for use with microvia and build-up technologies, as well as thermal-cure and UV-cure solder masks.

PRIMARY FUNCTION

Formulate, develop new products, and modify existing products as identified by the sales staff and company management. Conduct laboratory evaluations and tests of the industry's products and processes. Prepare detailed written reports regarding chemical characteristics. The Formulator will also have supervisory responsibility for R&D Technicians.

ESSENTIAL DUTIES

1. Prepare design of experiments (DOE) to aid in the development of new products related to the solar energy industry, printed electronics, ink jet technologies, specialty coatings and additives, nanotechnologies, and applications.
2. Compile feasibility studies for bringing new products and emerging technologies through manufacturing to the marketplace.
3. Provide product and manufacturing support.
4. Provide product quality control and support.
5. Participate in multifunctional teams.

REQUIRED EDUCATION/EXPERIENCE

1. Minimum 4-year college degree in engineering or chemistry.
2. Preferred: Minimum 4-years' experience in chemical technologies and polymer science.
3. Knowledge of ink jet technologies, advanced materials and emerging technologies, including nano technologies.

Email: BobW@Taiyo-america.com with a subject line of [Application for Formulating Chemist]

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FLEXIBLE CIRCUIT Technologies

Application Engineer

Flexible Circuit Technologies (FCT) is a global supplier providing design, prototyping and production of flexible circuits, rigid flex circuits, flexible heaters and full assembly services.

Responsibilities

- Gain understanding for customer/specific project requirements
- Review customer files, analyze - application, design, stack up, materials, mechanical requirements; develop cost-effective design to meet requirements
- Quote and follow-up to secure business
- Work with CAD: finalize files, attain customer approval prior to build
- Track timeline/provide customers with updates
- Follow up on prototype, assist with design changes (if needed), and push forward to production
- Work as the lead technician/program manager or as part of FCT team working with an assigned application engineer
- Help customer understand FCT's assembly, testing, and box build services
- Understand manufacturing and build process for flexible and rigid-flex circuits

Qualifications

- Demonstrated experience: flex circuit/rigid-flex design including design rules, IPC; flex heater design +
- Ability to work in fast-paced environment, broad range of projects, maintain sense of urgency
- Ability to work as a team player
- Excellent written and verbal communication skills
- Willing to travel for sales support and customer support activities if needed

Competitive salary, bonus program, and benefits package. Preferred location Minneapolis, MN area.

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Career Opportunities

EMA Design Automation®

Technical Marketing Engineer

EMA Design Automation, a leader in product development solutions, is in search of a detail-oriented individual who can apply their knowledge of electrical design and CAD software to assist marketing in the creation of videos, training materials, blog posts, and more. This Technical Marketing Engineer role is ideal for analytical problem-solvers who enjoy educating and teaching others.

Requirements:

- Bachelor's degree in electrical engineering or related field with a basic understanding of engineering theories and terminology required
- Basic knowledge of schematic design, PCB design, and simulation with experience in OrCAD or Allegro preferred
- Candidates must possess excellent writing skills with an understanding of sentence structure and grammar
- Basic knowledge of video editing and experience using Camtasia or Adobe Premiere Pro is preferred but not required
- Must be able to collaborate well with others and have excellent written and verbal communication skills for this remote position

EMA Design Automation is a small, family-owned company that fosters a flexible, collaborative environment and promotes professional growth.

Send Resumes to: resumes@ema-eda.com

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pluritec®

MACHINES FOR PRINTED CIRCUIT BOARDS

Field Service Engineer

Location: West Coast, Midwest

Pluritec North America, ltd., an innovative leader in drilling, routing, and automated inspection in the printed circuit board industry, is seeking a full-time field service engineer.

This individual will support service for North America in printed circuit board drill/routing and X-ray inspection equipment.

Duties included: Installation, training, maintenance, and repair. Must be able to troubleshoot electrical and mechanical issues in the field as well as calibrate products, perform modifications and retrofits. Diagnose effectively with customer via telephone support. Assist in optimization of machine operations.

A technical degree is preferred, along with strong verbal and written communication skills. Read and interpret schematics, collect data, write technical reports.

Valid driver's license is required, as well as a passport, and major credit card for travel.

Must be able to travel extensively.

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Career Opportunities

European Product Manager
Taiyo Inks, Germany

We are looking for a European product manager to serve as the primary point of contact for product technical sales activities specifically for Taiyo Inks in Europe.

Duties include:
- Business development & sales growth in Europe
- Subject matter expert for Taiyo ink solutions
- Frequent travel to targeted strategic customers/OEMs in Europe
- Technical support to customers to solve application issues
- Liaising with operational and supply chain teams to support customer service

Skills and abilities required:
- Extensive sales, product management, product application experience
- European citizenship (or authorization to work in Europe/Germany)
- Fluency in English language (spoken & written)
- Good written & verbal communications skills
- Printed circuit board industry experience an advantage
- Ability to work well both independently and as part of a team
- Good user knowledge of common Microsoft Office programs
- Full driving license essential

What's on offer:
- Salary & sales commission--competitive and commensurate with experience
- Pension and health insurance following satisfactory probation
- Company car or car allowance

This is a fantastic opportunity to become part of a successful brand and leading team with excellent benefits. Please forward your resume to **jobs@ventec-europe.com.**

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Technical Service & Applications Engineer
Full-Time — Midwest (WI, IL, MI)

Koh Young Technology, founded in 2002 in Seoul, South Korea, is the world leader in 3D measurement-based inspection technology for electronics manufacturing. Located in Duluth, GA, Koh Young America has been serving its partners since 2010 and is expanding the team with an Applications Engineer to provide helpdesk support by delivering guidance on operation, maintenance, and programming remotely or on-site.

Responsibilities
- Provide support, preventive and corrective maintenance, process audits, and related services
- Train users on proper operation, maintenance, programming, and best practices
- Recommend and oversee operational, process, or other performance improvements
- Effectively troubleshoot and resolve machine, system, and process issues

Skills and Qualifications
- Bachelor's in a technical discipline, relevant Associate's, or equivalent vocational or military training
- Knowledge of electronics manufacturing, robotics, PCB assembly, and/or AI; 2-4 years of experience
- SPI/AOI programming, operation, and maintenance experience preferred
- 75% domestic and international travel (valid U.S. or Canadian passport, required)
- Able to work effectively and independently with minimal supervision
- Able to readily understand and interpret detailed documents, drawings, and specifications

Benefits
- Health/Dental/Vision/Life Insurance with no employee premium (including dependent coverage)
- 401K retirement plan
- Generous PTO and paid holidays

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Career Opportunities

ARLON ELECTRONIC MATERIALS

Arlon EMD, located in Rancho Cucamonga, California, is currently interviewing candidates for open positions in:

- **Engineering**
- **Quality**
- **Various Manufacturing**

All interested candidates should contact Arlon's HR department at 909-987-9533 or email resumes to careers.ranch@arlonemd.com.

Arlon is a major manufacturer of specialty high-performance laminate and prepreg materials for use in a wide variety of printed circuit board applications. Arlon specializes in thermoset resin technology, including polyimide, high Tg multifunctional epoxy, and low loss thermoset laminate and prepreg systems. These resin systems are available on a variety of substrates, including woven glass and non-woven aramid. Typical applications for these materials include advanced commercial and military electronics such as avionics, semiconductor testing, heat sink bonding, High Density Interconnect (HDI) and microvia PCBs (i.e. in mobile communication products).

Our facility employs state of the art production equipment engineered to provide cost-effective and flexible manufacturing capacity allowing us to respond quickly to customer requirements while meeting the most stringent quality and tolerance demands. Our manufacturing site is ISO 9001: 2015 registered, and through rigorous quality control practices and commitment to continual improvement, we are dedicated to meeting and exceeding our customers' requirements.

For additional information please visit our website at www.arlonemd.com

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INSULECTRO

Are You Our Next Superstar?!

Insulectro, the largest national distributor of printed circuit board materials, is looking to add superstars to our dynamic technical and sales teams. We are always looking for good talent to enhance our service level to our customers and drive our purpose to enable our customers build better boards faster. Our nationwide network provides many opportunities for a rewarding career within our company.

We are looking for talent with solid background in the PCB or PE industry and proven sales experience with a drive and attitude that match our company culture. This is a great opportunity to join an industry leader in the PCB and PE world and work with a terrific team driven to be vital in the design and manufacture of future circuits.

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Career Opportunities

MivaTek Global

Field Service Technician

MivaTek Global is focused on providing a quality customer service experience to our current and future customers in the printed circuit board and microelectronic industries. We are looking for bright and talented people who share that mindset and are energized by hard work who are looking to be part of our continued growth.

Do you enjoy diagnosing machines and processes to determine how to solve our customers' challenges? Your 5 years working with direct imaging machinery, capital equipment, or PCBs will be leveraged as you support our customers in the field and from your home office. Each day is different, you may be:

- Installing a direct imaging machine
- Diagnosing customer issues from both your home office and customer site
- Upgrading a used machine
- Performing preventive maintenance
- Providing virtual and on-site training
- Updating documentation

Do you have 3 years' experience working with direct imaging or capital equipment? Enjoy travel? Want to make a difference to our customers? Send your resume to N.Hogan@MivaTek.Global for consideration.

More About Us

MivaTek Global is a distributor of Miva Technologies' imaging systems. We currently have 55 installations in the Americas and have machine installations in China, Singapore, Korea, and India.

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TRAIN. WORK SMARTER. SUCCEED.

Become a Certified IPC Master Instructor

Opportunities are available in Canada, New England, California, and Chicago. If you love teaching people, choosing the classes and times you want to work, and basically being your own boss, this may be the career for you. EPTAC Corporation is the leading provider of electronics training and IPC certification and we are looking for instructors that have a passion for working with people to develop their skills and knowledge. If you have a background in electronics manufacturing and enthusiasm for education, drop us a line or send us your resume. We would love to chat with you. Ability to travel required. IPC-7711/7721 or IPC-A-620 CIT certification a big plus.

Qualifications and skills

- A love of teaching and enthusiasm to help others learn
- Background in electronics manufacturing
- Soldering and/or electronics/cable assembly experience
- IPC certification a plus, but will certify the right candidate

Benefits

- Ability to operate from home. No required in-office schedule
- Flexible schedule. Control your own schedule
- IRA retirement matching contributions after one year of service
- Training and certifications provided and maintained by EPTAC

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Career Opportunities

The Test Connection, Inc.

Rewarding Careers

Take advantage of the opportunities we are offering for careers with a growing test engineering firm. We currently have several openings at every stage of our operation.

The Test Connection, Inc. is a test engineering firm. We are family owned and operated with solid growth goals and strategies. We have an established workforce with seasoned professionals who are committed to meeting the demands of high-quality, low-cost and fast delivery.

TTCI is an Equal Opportunity Employer. We offer careers that include skills-based compensation. We are always looking for talented, experienced test engineers, test technicians, quote technicians, electronics interns, and front office staff to further our customer-oriented mission.

Associate Electronics Technician/ Engineer (ATE-MD)

TTCI is adding electronics technician/engineer to our team for production test support.

- Candidates would operate the test systems and inspect circuit card assemblies (CCA) and will work under the direction of engineering staff, following established procedures to accomplish assigned tasks.
- Test, troubleshoot, repair, and modify developmental and production electronics.
- Working knowledge of theories of electronics, electrical circuitry, engineering mathematics, electronic and electrical testing desired.
- Advancement opportunities available.
- Must be a US citizen or resident.

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Test Engineer (TE-MD)

In this role, you will specialize in the development of in-circuit test (ICT) sets for Keysight 3070 (formerly HP) and/or Teradyne (formerly GenRad) TestStation/228X test systems.

- Candidates must have at least three years of experience with in-circuit test equipment. A candidate would develop and debug our test systems and install in-circuit test sets remotely online or at customer's manufacturing locations nationwide.
- Candidates would also help support production testing and implement Engineering Change Orders and program enhancements, library model generation, perform testing and failure analysis of assembled boards, and other related tasks.
- Some travel required and these positions are available in the Hunt Valley, Md., office.

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Sr. Test Engineer (STE-MD)

- Candidate would specialize in the development of in-circuit test (ICT) sets for Keysight 3070 (formerly Agilent & HP), Teradyne/ GenRad, and Flying Probe test systems.
- Strong candidates will have more than five years of experience with in-circuit test equipment. Some experience with flying probe test equipment is preferred. A candidate would develop, and debug on our test systems and install in-circuit test sets remotely online or at customer's manufacturing locations nationwide.
- Proficient working knowledge of Flash/ISP programming, MAC Address and Boundary Scan required. The candidate would also help support production testing implementing Engineering Change Orders and program enhancements, library model generation, perform testing and failure analysis of assembled boards, and other related tasks. An understanding of stand-alone boundary scan and flying probe desired.
- Some travel required. Positions are available in the Hunt Valley, Md., office.

Contact us today to learn about the rewarding careers we are offering. Please email resumes with a short message describing your relevant experience and any questions to careers@ttci.com. Please, no phone calls.

We proudly serve customers nationwide and around the world.

TTCI is an ITAR registered and JCP DD2345 certified company that is NIST 800-171 compliant.

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Career Opportunities

BLACKFOX
Premier Training & Certification

IPC Instructor

Longmont, CO; Phoenix, AZ; U.S.-based remote

Independent contractor, possible full-time employment

Job Description

This position is responsible for delivering effective electronics manufacturing training, including IPC Certification, to students from the electronics manufacturing industry. IPC instructors primarily train and certify operators, inspectors, engineers, and other trainers to one of six IPC Certification Programs: IPC-A-600, IPC-A-610, IPC/WHMA-A-620, IPC J-STD-001, IPC 7711/7721, and IPC-6012.

IPC instructors will conduct training at one of our public training centers or will travel directly to the customer's facility. A candidate's close proximity to Longmont, CO, or Phoenix, AZ, is a plus. Several IPC Certification Courses can be taught remotely and require no travel.

Qualifications

Candidates must have a minimum of five years of electronics manufacturing experience. This experience can include printed circuit board fabrication, circuit board assembly, and/or wire and cable harness assembly. Soldering experience of through-hole and/or surface-mount components is highly preferred.

Candidate must have IPC training experience, either currently or in the past. A current and valid certified IPC trainer certificate holder is highly preferred.

Applicants must have the ability to work with little to no supervision and make appropriate and professional decisions.

Send resumes to Sharon Montana-Beard at sharonm@blackfox.com.

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American Standard Circuits
Creative Innovations In Flex, Digital & Microwave Circuits

CAD/CAM Engineer

Summary of Functions

The CAD/CAM engineer is responsible for reviewing customer supplied data and drawings, performing design rule checks and creating manufacturing data, programs, and tools required for the manufacture of PCB.

Essential Duties and Responsibilities

- Import customer data into various CAM systems.
- Perform design rule checks and edit data to comply with manufacturing guidelines.
- Create array configurations, route, and test programs, panalization and output data for production use.
- Work with process engineers to evaluate and provide strategy for advanced processing as needed.
- Itemize and correspond to design issues with customers.
- Other duties as assigned.

Organizational Relationship

Reports to the engineering manager. Coordinates activities with all departments, especially manufacturing.

Qualifications

- A college degree or 5 years' experience is required. Good communication skills and the ability to work well with people is essential.
- Printed circuit board manufacturing knowledge.
- Experience using CAM tooling software, Orbotech GenFlex®.

Physical Demands

Ability to communicate verbally with management and coworkers is crucial. Regular use of the telephone and e-mail for communication is essential. Sitting for extended periods is common. Hearing and vision within normal ranges is helpful for normal conversations, to receive ordinary information and to prepare documents.

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Career Opportunities

U.S. CIRCUIT

Plating Supervisor

Escondido, California-based PCB fabricator U.S. Circuit is now hiring for the position of plating supervisor. Candidate must have a minimum of five years' experience working in a wet process environment. Must have good communication skills, bilingual is a plus. Must have working knowledge of a plating lab and hands-on experience running an electrolytic plating line. Responsibilities include, but are not limited to, scheduling work, enforcing safety rules, scheduling/maintaining equipment and maintenance of records.

Competitive benefits package.
Pay will be commensurate
with experience.

Mail to:
mfariba@uscircuit.com

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APCT
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APCT, a leading manufacturer of printed circuit boards, has experienced rapid growth over the past year and has multiple opportunities for highly skilled individuals looking to join a progressive and growing company. APCT is always eager to speak with professionals who understand the value of hard work, quality craftsmanship, and being part of a culture that not only serves the customer but one another.

APCT currently has opportunities in Santa Clara, CA; Orange County, CA; Anaheim, CA; Wallingford, CT; and Austin, TX. Positions available range from manufacturing to quality control, sales, and finance.

We invite you to read about APCT at APCT.com and encourage you to understand our core values of passion, commitment, and trust. If you can embrace these principles and what they entail, then you may be a great match to join our team! Peruse the opportunities by clicking the link below.

Thank you, and we look forward to
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I-007eBooks The Printed Circuit Designer's Guide to...

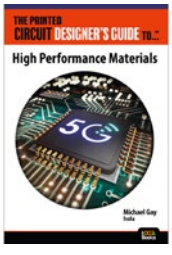
Designing for Reality by Matt Stevenson, Sunstone Circuits

Based on the wisdom of 50 years of PCB manufacturing at Sunstone Circuits, this book is a must-have reference for designers seeking to understand the PCB manufacturing process as it relates to their design. Designing for manufacturability requires understanding the production process fundamentals and factors within the process that often lead to variations in manufacturability, reliability, and cost of the board. Speaking of making better decisions, **read it now!**

Thermal Management with Insulated Metal Substrates, Vol. 2

by Didier Mauve and Robert Art, Ventec International Group

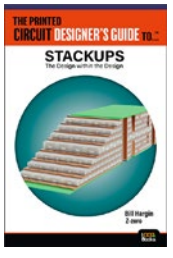
This book covers the latest developments in the field of thermal management, particularly in insulated metal substrates, using state-of-the-art products as examples and focusing on specific solutions and enhanced properties of IMS. **Add this essential book to your library.**



High Performance Materials

by Michael Gay, Isola

This book provides the reader with a clearer picture of what to know when selecting which material is most desirable for their upcoming products and a solid base for making material selection decisions. **Get your copy now!**



Stackups: The Design within the Design

by Bill Hargin, Z-zero

Finally, a book about stackups! From material selection and understanding laminate datasheets, to impedance planning, glass weave skew and rigid-flex materials, topic expert Bill Hargin has written a unique book on PCB stackups. **Get yours now!**

THE ELECTRONICS INDUSTRY'S GUIDE TO... *The Evolving PCB NPI Process*

by Mark Laing and Jeremy Schitter, Siemens Digital Industries Software

The authors of this book take a look at how market changes in the past 15 years, coupled with the current slowdown of production and delivery of materials and components, has affected the process for new product introduction (NPI) in the global marketplace. As a result, companies may need to adapt and take a new direction to navigate and thrive in an uncertain and rapidly evolving future. Learn how to streamline the NPI process and better manage the supply chain. ***Get it Now!***

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