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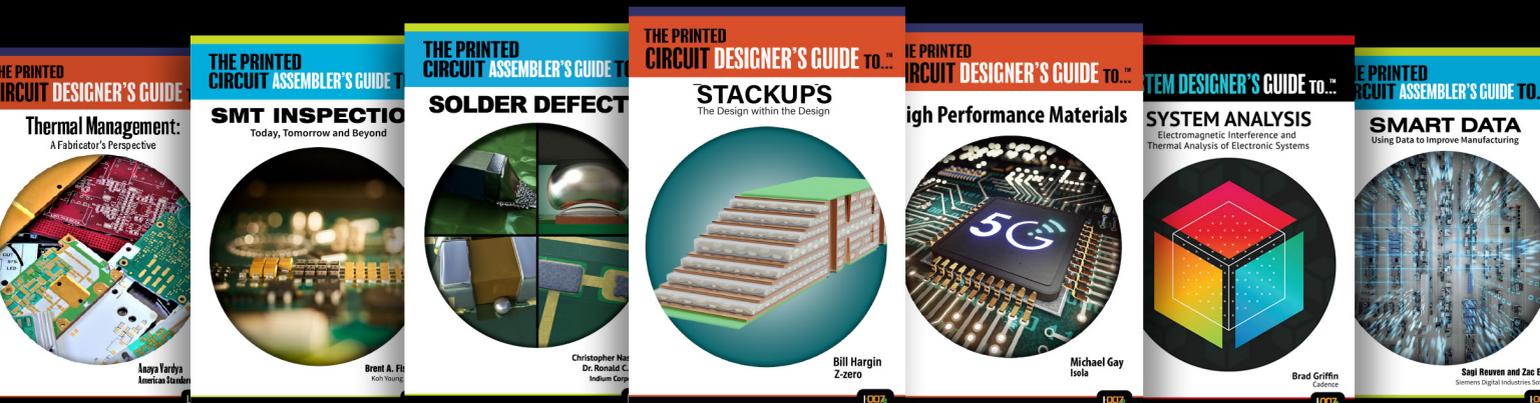
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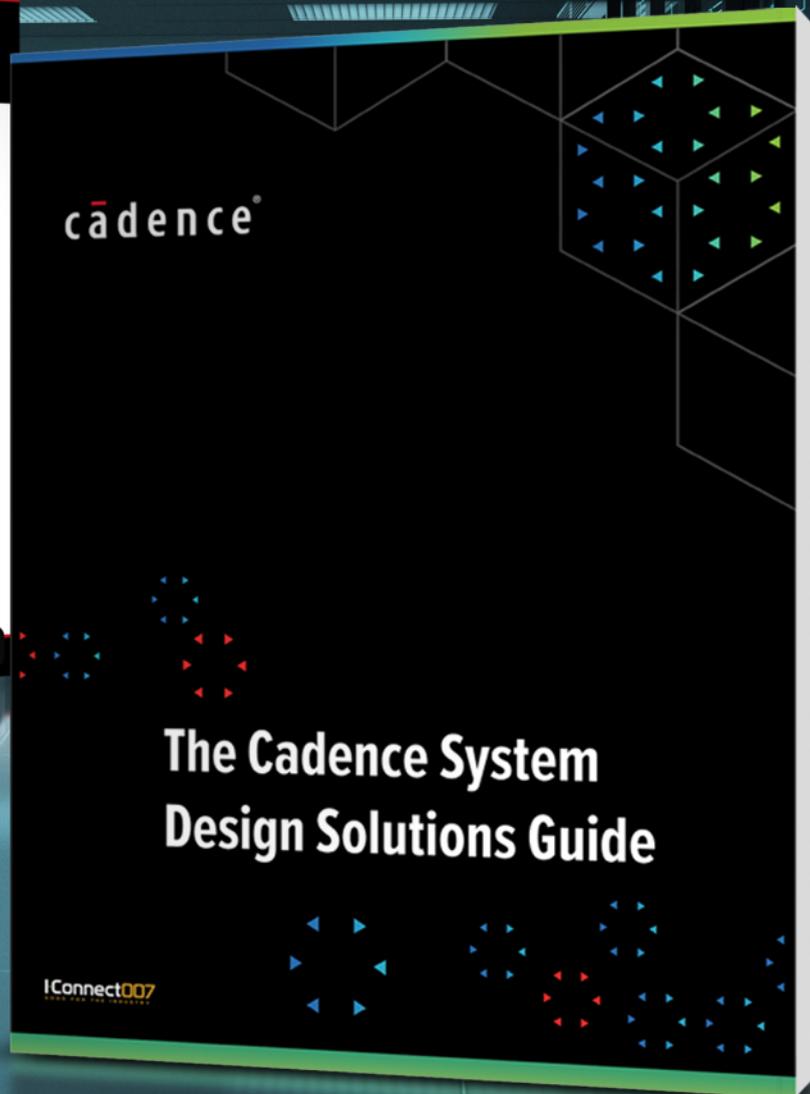
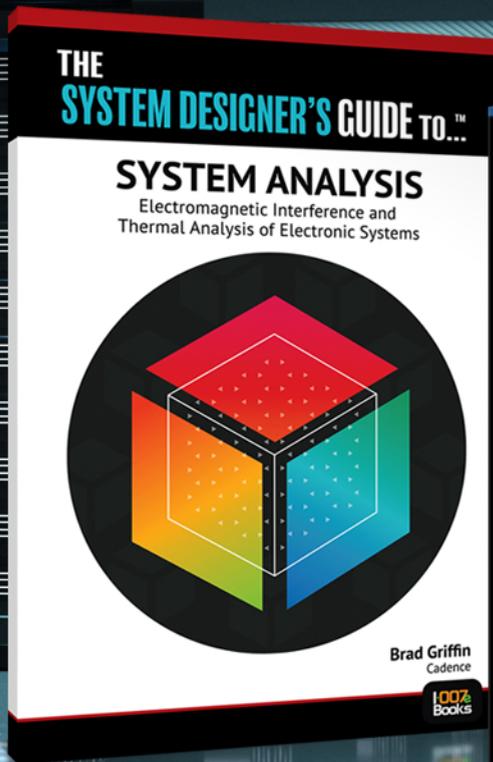
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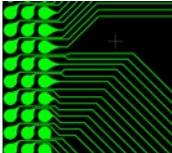
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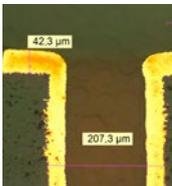
Additive Design: The Same, but Different

As today's shrinking geometries push the limits of traditional fab methods, you need an ace up your sleeve more than ever. Additive processes may be your best bet. This month's issue of *Design007 Magazine* focuses on how readers can get started designing additive and semi-additive PCBs, and how the design process for additive technology differs from that of traditional subtractive processes.

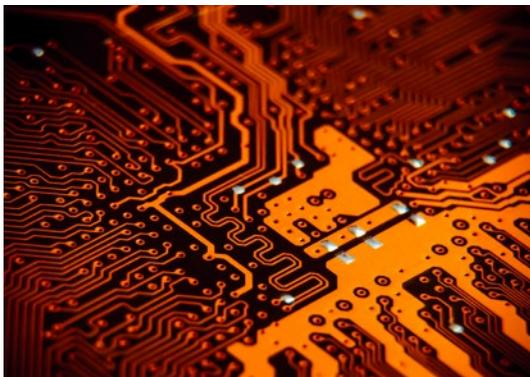
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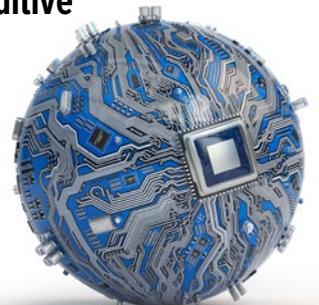
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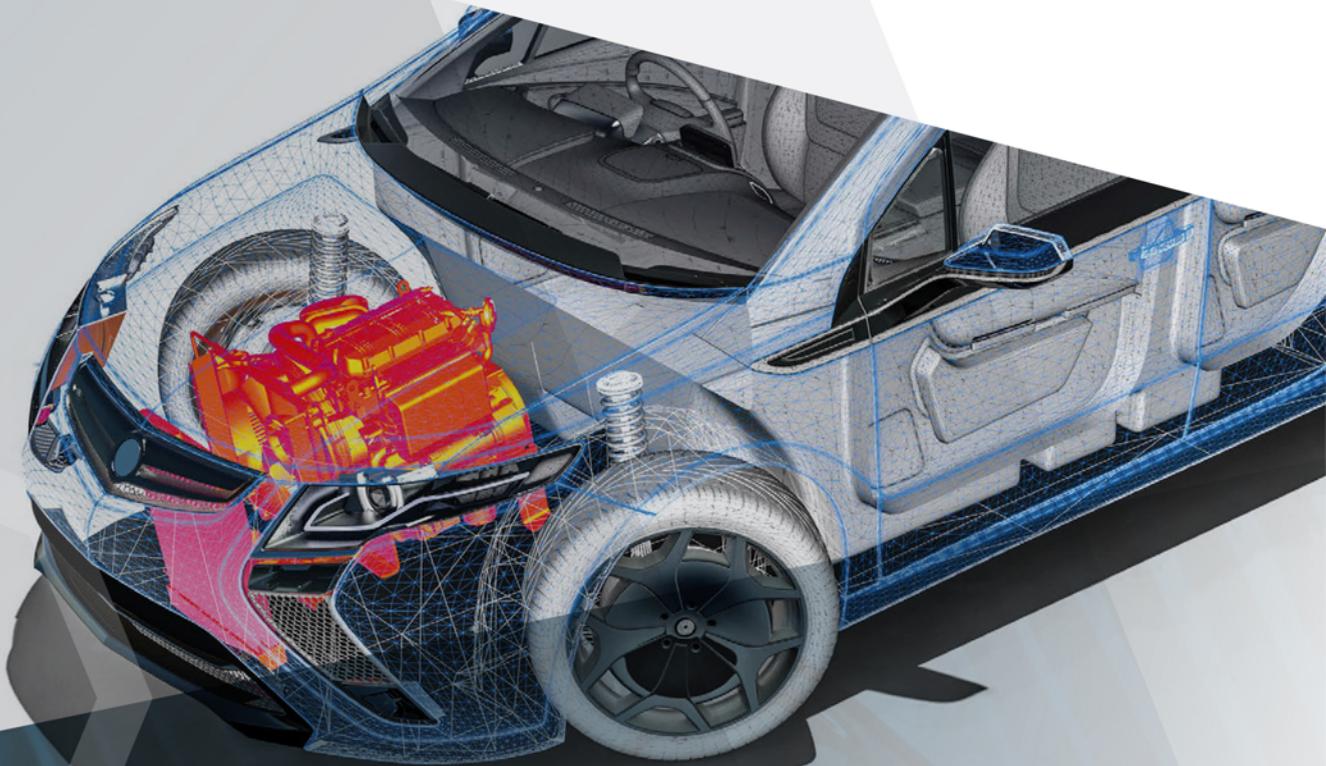
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FLEX007

This Month in Flex

Flexible and rigid-flex circuits continue to evolve at a constant pace. Of all of the innovative “twists” on flex circuits, wearable electronics may wind up being the most ubiquitous of all someday. This month, we bring you a column by Joe Fjelstad that delves into the possibilities afforded by wearable electronics.

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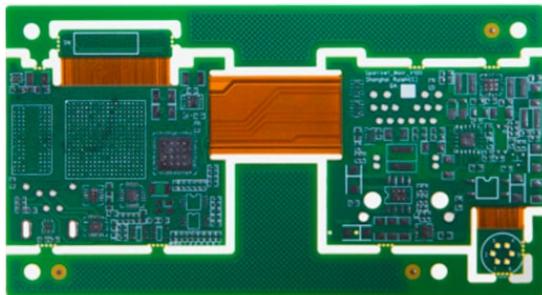
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Additive Design: The Same, but Different

The Shaughnessy Report

by Andy Shaughnessy, I-CONNECT007

When we decided to focus on designing for additive and semi-additive processes this month, we ran into a challenge much like the one we faced with the February issue of *PCB007 Magazine*: There aren't too many experts on this subject, not to mention educational resources or agreed-upon best practices.

Additive and semi-additive design and manufacturing are in flux, and PCB designers in the additive world are basically making the

rules as they go. As instructor Cherie Litson says in her feature article this month, when it comes to additive processes, there are far more questions than answers. Cherie is currently working on an additive design curriculum which she hopes to have ready to go this year. The industry certainly needs more additive design resources.

At recent trade shows, there was plenty of chatter about additive and semi-additive design techniques. Much of it is speculation,



but the interest is there. If your company's high-density boards have pushed traditional subtractive etch fabrication to its practical limits, you're probably already researching additive and semi-additive processes.

Defense and aerospace contractors are very interested in additive. NASA is doing an additive happy dance, and so are consumer device makers who are on the leading edge of miniaturization, in the arena of ultra-HDI. If you need spaces and traces below 1 mil, additive is an attractive option.

It's not that subtractive etch can't go below 1 mil spaces and traces. Traditional fabrication processes can go below 1 mil, but the boards become burdensomely complex, which is going to cost you—in extra routing and via layers, and increased lamination cycles, which drive up cost and drive down reliability and yield.

Additive and semi-additive processes seem to be a better way, at least so far. Additive can produce spaces and traces 0.5 mils wide and smaller, and the laminate itself can be thinner, too. And the additive traces are beautiful, with straight walls—not trapezoidal. For 60 years, fabricators and designers have wondered what it would be like to have perfectly straight-walled traces, and now we can find out.

But there are plenty of potential pitfalls. In fact, we don't even know what we don't know, as Pentagon spokesmen like to say. How does a designer get involved in designing additive PCBs? What resources are available? When does it make sense to use additive or semi-additive vs. traditional? How are signal integrity, crosstalk, and impedance affected by these new constructions? Where is the sweet spot? Do today's EDA tools support additive and semi-additive?

This month's issue of *Design007 Magazine* will focus on how readers can get started designing additive and semi-additive PCBs, and how the design process for additive technology differs from that of traditional subtractive processes.

In a conversation with Dave Torp, he discusses additive design techniques and why the design cycle is similar to traditional design, but in a different order. Cherie Litson walks us through the steps in additive and semi-additive design, including DFM and signal integrity considerations. Luca Gautero explains how solder mask is applied during additive processes, and how this affects the design rule check guidelines. Columnist Tara Dunn answers some of the many questions designers have about designing boards made with semi-additive (SAP) processes. Tomas Chester addresses designing PCBs with additive traces.

Columnist Barry Olney discusses a typical SAP design process, its benefits and challenges, and why SAP may be part of a natural manufacturing evolution as lines and spaces grow increasingly denser. Dave Wiens explains how today's EDA tools will have to adapt to optimize the design cycle for additive and semi-additive PCBs, and Calumet's Todd Brassard and Meredith LaBeau detail some of the hurdles facing designers who move into additive PCBs, and why a little competition here would help get this technology standardized.

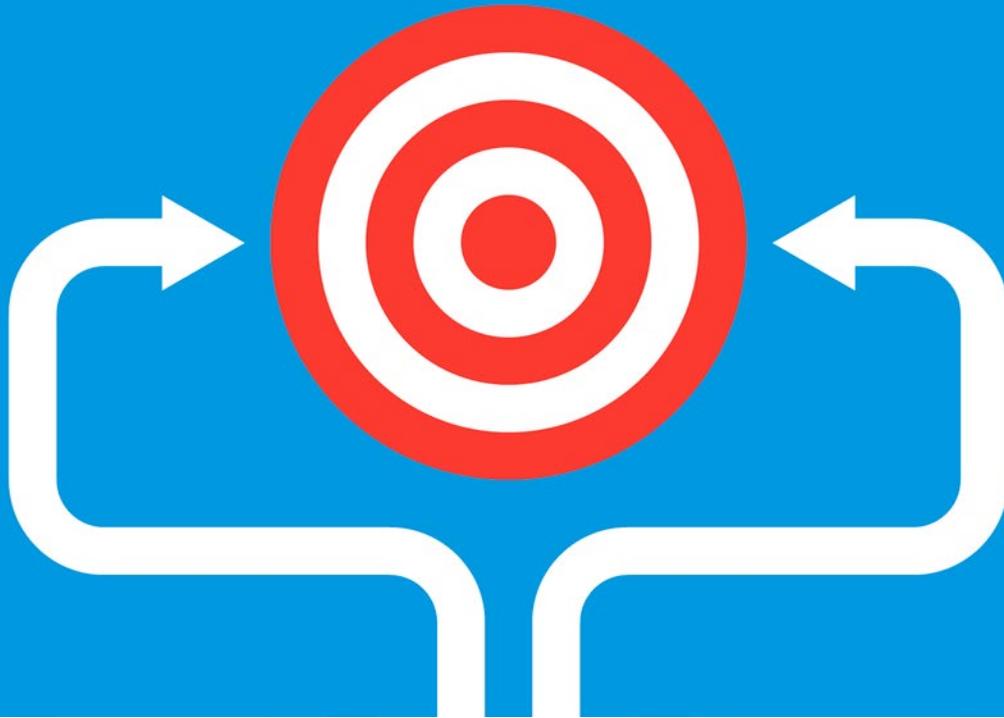
We also have columns from our regular contributors Matt Stevenson, Martyn Gaudion, John Coonrod, Vern Solberg, Kelly Dack, Beth Turner, and Joe Fjelstad. Finally, we have a review of *The Printed Circuit Designer's Guide to... Stackups: The Design within the Design* by Skyler Sopp, and an article by Anaya Vardya.

Additive and semi-additive processes are microcosms of the industry—there's a lot of innovation going on. And we'll keep bringing you the design information you need to know. See you next month! **DESIGN007**



Andy Shaughnessy is managing editor of *Design007 Magazine*. He has been covering PCB design for 20 years. He can be reached by [clicking here](#).

ADDITIVE DESIGN: Same Steps, Different Order



Feature Interview by the I-Connect007
Editorial Team

We recently spoke with Dave Torp, CEO of Winonics, about the company's additive and semi-additive processes and what PCB designers need to know if they're considering designing boards with these new technologies. As Dave explains, additive design is not much different from traditional design, but the steps in the design cycle are out of order, and additive designers must communicate with their fabricators because so much of the new processes are still proprietary.

Andy Shaughnessy: Dave, give us some background on Winonics and your focus on additive and semi-additive processes.

Dave Torp: Additive Circuits Technologies is the parent company, which owns two com-

panies. One is Winonics, a rigid circuit board company. The other is a flexible circuit board company called Bench 2 Bench Technologies. Winonics is ISO-9001, AS9100, and ITAR-registered. We have a 52,000 square-foot facility in Brea, California. Bench 2 Bench has a 25,000 square-foot facility, located about 10 minutes away in Fullerton.

From the holistic view, our focus is in the high-reliability electronics market. We focus on the aerospace, defense, and the medical device electronics. Our competitive anchor is providing great service. We don't really put too many boundaries on what we do. Simply put, we're a technology realization company.

We have process patents for applying circuitry and metallization in an additive technology. We also have some trade secrets that



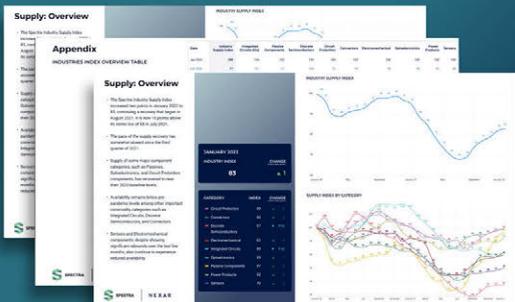
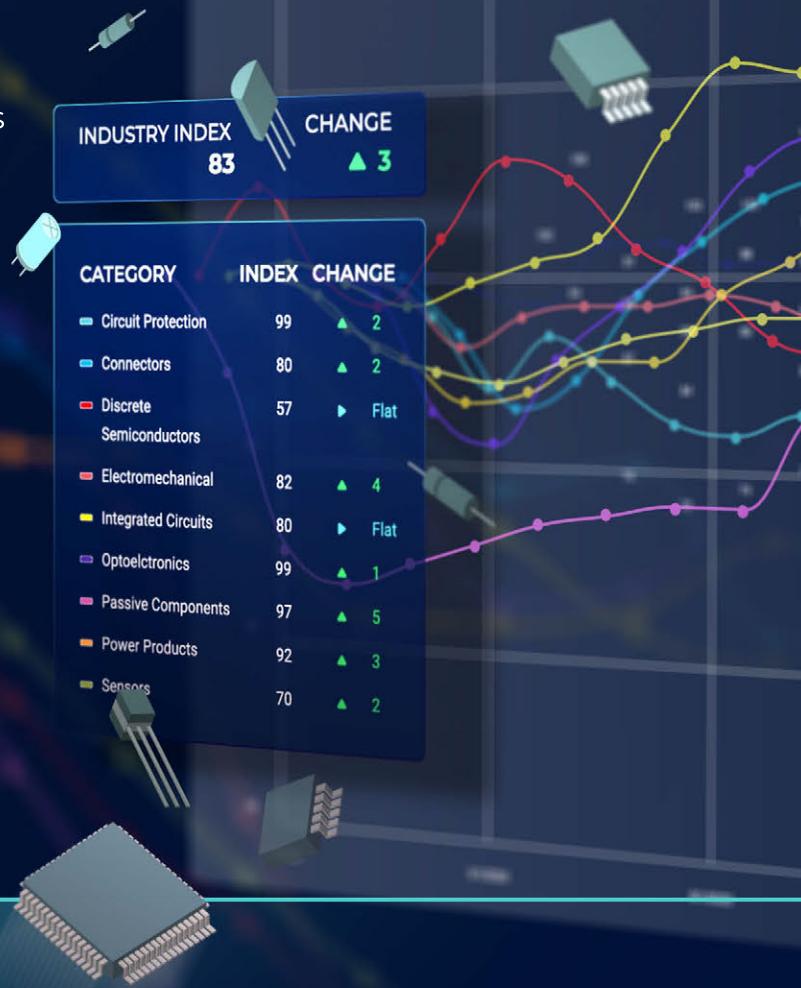
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we keep behind the vest with respect to our manufacturing operations. What the additive technology enables is ultra-fine features and ultra-high definition. The enabling technology provides metallization in very high-density configurations to make high-density interconnects. We have demonstrated the technology down to 15-micron lines and spaces, which was, at the time, the limit of the laser technology that we had.

As the LDI technology becomes more precise, we'll have the ability to go further down that pathway. So, we look to being capable of doing 8-micron lines and spaces and below by 2023.

The real drivers for the technology are miniaturization and the need for greater speed. If you look at some of the frequencies that are required to enable a communication, you are getting up into the 5G-plus mindset. The layer counts within the circuit boards aren't increasing, but the number of interconnects between those layers is increasing. You can have a lot of fun with respect to the layers that are being interconnected and how the microvias are being stacked and racked upon each other. Sometimes you stack them right on top of each other. Other times, you stagger them out a little bit, depending on the signal integrity that you want.

With respect to the additive processes, first we have semi-additive technology, which is a fairly new process. In a lot of cases, you take the ultra-thin copper foils, or the plating applied to the substrate. You hit it with photo-sensitive materials, etch away that ultra-thin part of the copper, and then start to plate back up. That's the semi-additive process.

The fully additive process is the newest technology, where you print the pattern that you want on the substrate without copper foil, using a palladium or platinum-based chemistry, and expose it with a laser or a UV source of radiation. Then you allow the electroless copper plating to be deposited, followed by electrolytic plating



Dave Torp

This allows us to create ultra-fine traces down to sub-15-micron type technology. We're excited about the opportunities, especially in the in-betweens, where you're using hybrid interposer layers to try to connect this heterogeneous integrated package together.

Barry Matties: I'm curious about what the challenges are for designers. Are you offering design services, or are you working with designers to help them understand how to efficiently design for additive or semi-additive?

Torp: We work with the designers. A lot of the tried-and-true design technologies are based upon the subtractive methodology, whereas the additive methodology is a little bit different. Your sequence of operations and how you build the structures is different. If you want to build a house, are you going to hog it out, or are you going to machine it out of a tree? You've got a big tree and you're going to machine a

house out of it. That's the way the subtractive process works.

With the additive process, you're building from the bottom up, so it's a little bit different methodology as far as how you put the layers together. We work with the designers, and a lot of the military and aerospace guys are looking to get finer and finer features which, within the U.S. footprint, are increasingly difficult to come by. There are very few circuit board shops that can get down to the lines and spaces that we're capable of achieving with the additive process.

Shaughnessy: Talk a little bit more about that, Dave. How else is the design process different?

Torp: It's different in some respects. You'll find with the ultra-thin foils, if you're familiar with traditional laminate structure, is that it's required to have a tooth on one side, and then you laminate the foil onto the substrate, whether it be the FR-4 or some of the BT or the PTFE-based substrate. You required a little bit of a tooth that acts as a nail, so when you make your copper-clad laminate, you've got to bite into the laminate. With the technology that we're using, it's a chemistry that's applied to the substrate or the prepreg, at that time. It conforms to the contour of the surface, so you wind up with a better bite than you do with these ultra-thin foils, because they just don't have much of a tooth.

If you think of the tooth as a nail that gets driven into the substrate, the adhesion there is minimal at best because you just don't have the length of nail being driven into the substrate. With the capabilities that additive circuits bring, it can conform to every nook and cranny. You wind up with this very, very good adhesion on all layers of the substrates that you're applying it to, and specifically the outside layers of the multilayer, where you need really good adhesion strength. The inner layers are laminated together. You can get away with some minimal adhesion, but on those outer

layers, you must have good peel strength, sheer strength, and strength in connection with the substrate.

Then there's the trick of making the microvias between the layers because, typically, you're building the layers up. You're going through plating the vias and the same plating technologies used, but the order of operations to get the via into contact with the capture pad below is a little bit tricky, a little bit different than what people are used to. But we've done the reliability testing. We've sent the assemblies to cap for thermal cycling resistance testing. We're doing very well with respect to the performance of that thermal cycling testing.

As I'm sure you're familiar, that type of testing is meant to shred the microvia into pieces. We were able to survive their -55°C to $+205^{\circ}\text{C}$ thermal cycling without too many issues. We have a few defense electronics-related customers very interested in that technology, particularly on the stuff that's really hard to stick to, which is typically the PTFE-based laminate material. We can get pretty good adhesion onto some substrates that are very difficult to work with. In a nutshell, that's what differentiates us from some of the other processes out there.

Shaughnessy: A lot of it sounds like different steps for a designer.

Torp: The order of the steps is a little bit different. You're not trying to do it in a subtractive methodology. You're building from the inside out, rather than the outside in. Our website covers a little bit of it, but it's a very proprietary process. Many of our customers are keeping a tight lid on what they do, so it's tough to find information on exactly how to do this. Typically, we work with the designers one-on-one. They have their requirements with respect to impedance and signal-to-noise ratios. They have some ideas of what the end functionality needs to have. Then, we work with them on what's capable. What is stretching it? We invite

the designers to work with us on their specific opportunities and processes.

Then we build prototypes for them, and later they come out and do the thermal cycling and environmental stress testing. They say, “Wow, this is pretty interesting stuff. We didn’t quite think about it the way you guys think about it.” It’s an alternative type of process. Normally, it’s in the areas where people struggle with the material set, the low Dk, high-frequency materials set is one that we’ve had the greatest amount of interest in, especially, from the defense electronics guys.

Matties: When you say it’s proprietary, is that referring to the design process?

Torp: It’s the fabrication process. The order of the process is a little bit different than what they’re used to, but we’re using all the same set of materials that they’re used to. From a reliability standpoint, you have similar outcomes; it’s just not the same order of operation. You’re still using the same electroless copper and electrolytic copper, but the way you’re connecting the dots, so to speak, is a little out of sequence.

Matties: So, if a traditional PCB designer wants to learn how to do additive design, is it important that they talk to the manufacturer building the board?

Torp: Yes, you really need to talk to the fabricators building the boards. That’s where the reality, the product realization, comes in. There are not many board fabricators in the world actually doing this, and they’re keeping much of their processes under lock and key.

Matties: Do you see a growing market for additive and semi-additive?

Torp: Yes, there’s very big market growth area because the complexity and the number of connections on the board is increasing, especially with the laser-drilling of microvias.

Matties: When should the designer consider using additive? What’s the trigger point for that decision being made?

Torp: I would say the lines and spaces are the triggers. Once you start to get below, let’s say, one mil or 25-micron lines and spaces, you start to see an increased desire to move toward the additive process, rather than to try to do it in the semi-additive process. It comes down to being able to control plating within the process, and especially your registration at that point. It’s a very difficult thing to go below 25-micron lines and spaces.

That’s where the designers must tell us what their requirements are, particularly for signal-to-noise ratio impedance. The dielectrics are getting

more like glass in terms of trying to get to the operating frequencies where the HF/RF guys operate. This is where additive comes in.

It’s just a spooky environment. The high-speed digital stuff is not as bad as the high-frequency designs. I know Happy can expound upon that. The high-frequency engineers are very knowledgeable folks, and they light up when you start to talk about the high-frequency space.



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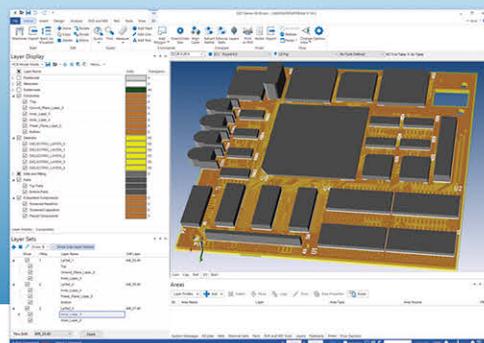
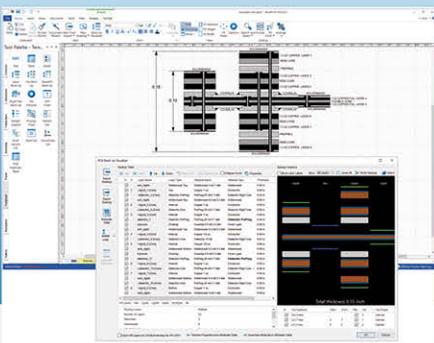
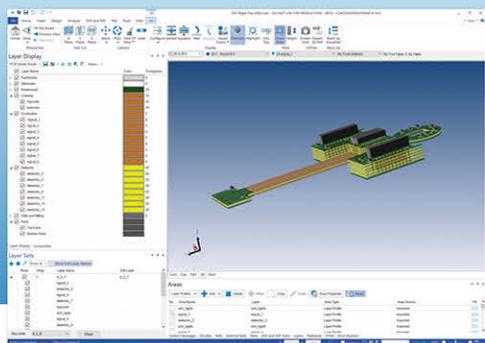


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Happy Holden: You're balancing the losses between the dielectric losses and the copper losses, and the fields that they produce. As things get smaller, with the fields that are active, everything becomes infinitely more complex.

Torp: Yes, the high-speed digital is a little bit easier than the high-frequency stuff. I was recently at the IMAPS Device Packaging Conference, and they're really going down in lines and spaces, headed toward glass interposers. They were talking about going down to 2-micron lines and spaces on glass, which is an extremely challenging thing. It's not the revenue center of gravity, at this point. But that's leaning toward the cutting edge, depending on how close you want to be to it.

Matties: Now, with the designers working with an additive design, what material selections or considerations should they have in mind? How does that vary?

Torp: We're working with a lot of high-frequency materials. We try to stay copper-clad laminate supplier-independent. We like to work with them all. But you start to see more of the higher-temperature, higher-frequency materials—the PTFE and the ceramic-filled type materials. Then, we also do a lot of work on the FR-4 traditional epoxy materials.

Then you start to look at some of the polyimide materials, which have their own set of issues. They move around a little bit. They tend to be a little bit more hydroscopic and create some dimensional issues that you must compensate for. That's the biggest thing with some of the material selections.

There are quite a few things happening with additive before we standardize on a process; a lot of the standards are rear-view mirror kinds of things.

Shaughnessy: Are there currently IPC standards for additive or semi-additive?

Torp: There are some standards and standards committees coming online for additive. There's the Ultra High-Definition Committee that's recently been formed. The Sintering Materials Committee just finished its first publication of a standard, so they're looking at alternative material types with respect to putting metallization down onto the substrates. They're looking at a lot of nano-sintering materials, and copper-based materials to get a copper-to-copper interconnect.

Then there are also committees dedicated to textiles and alternative substrates as well, because people are trying to put this on quite a variety of materials. The IPC does have quite a few new standards committees working on the additive technology; much of it is around the conductive inks that are being supplied to the industry.

Shaughnessy: Can you use a regular field solver to model additive and semi-additive designs?

Torp: Yes. We've engaged a few designers to help us with signal attenuation. That's not necessarily our core competency. But we do have a couple of folks very good at modeling capabilities who help the designers model the circuitry.

Shaughnessy: Very cool. If someone is using any of the main EDA tools, do they have to



do certain workarounds for this, or is it fairly intuitive?

Torp: I'd say it's fairly intuitive. The same laws of physics apply, and they just get more accentuated when you start to get into finer lines and spaces. Eventually, you reach a signal integrity barrier that is hard to design around, especially when everything gets tighter and tighter together. You start to look at the edge effects, or the skin effects, that the copper has. You can't have any imperfections in the side walls of the copper, and the surface topography of the copper must be pretty consistent in order to get the signal integrity right, and to be able to model it.

Shaughnessy: I know the designers will like the straight walls of the traces. But is there any downside to the straight walls. I'm sure it has an effect on impedance, right?

Torp: Yes. Obviously, the conductor has a significant influence on the impedance and the signal integrity. You don't want variations in that conductor width as you move the signal through the conductors. The surface roughness also has some influence over the high-frequency applications.

Matties: What advice are you giving designers who are considering additive or moving into additive?

Torp: From the design perspective, my words of wisdom are to look at what's realistic in terms of registration. As you go through the lamination process, materials move. Each layer moves in relationship to each other so getting your registration right and making sure that you can

actually align layer to layer to layer, the way you intended it to. It has to do with the signal integrity. Registration, at least with the manufacturing piece of it, is one of the biggest challenges to overcome. Make sure the board fabricator, or the substrate fabricator, can achieve those levels of registration.

Matties: You say this market is growing. What year-on-year percentage increase are you seeing in additive?

Torp: At this point, the percentage increase is in the double digits CAGR on year-on-year. I think we will reach an inflection point, probably in 2023-24, where it really sets up in significant volume. Right now, very few manufacturers are capable of the types of technology that the industry would like to move forward into as more fabricators and more manufacturing capabilities exist, particularly within the U.S. footprint. You're going to see an inflection point that goes from what is state-of-art to what is a revenue center of gravity. I anticipate that occurring sometime between the end of 2023 and end of 2024.

Matties: For designers who are doing high-speed and RF, over the next several years they will probably need learn additive designs, correct?

Torp: Yes, I would say within the next two and a half years, they must be a step toward additive and semi-additive processes, and a step away from that fully subtractive technology.

Matties: Aside from spacing and finer features, are there any other reasons somebody would go to additive?

Torp: There are some interconnect reliability features and functions that start to get involved in the whole design of the assembly itself, of what you're trying to connect. From a design standpoint, especially in the heterogeneous integration piece of it, it all starts with the design because you're now designing a system that will work together. It's not just designing the substrates or the boards. You're trying to marry it up into the shortest distance between the connections. You don't want to necessarily go through long transmission lines between the connections; you're trying to rack and stack things on top of each other.

From a design standpoint, especially in the heterogeneous integration piece of it, it all starts with the design because you're now designing a system that will work together.

You're trying to minimize the losses within the transmission lines that are either in the board or the interposer layers. You want to minimize the number of connections between the dots.

Matties: Dave, do you do rigid-flex with additive?

Torp: Yes. We look to put additive on polyimide substrates, the backbone of a flexible circuit. While trying to get adhesion to some of the polyimides, we are doing some plasma prep work to rough it up just a little bit, so we get better bite into the polyimides. But we are deploying and employing the additive technology into the polyimides to get that finer line and space.

Holden: Is the chemical a lot like the E Surface? Is it a nano technology?

Torp: The chemical is a palladium base. It's very similar to the old E Surface technology. There have been some twists and turns along the way to get better adhesion, but it's very similar. The patents for E Surface technology are owned by Additive Circuits Technologies and it's similar to what we were doing five to seven years ago. Now, it's just a matter of taking the technology and realizing it in a product, which was missing from the E Surface technology.

With the additive technologies, that Z-dimension starts to become available to you. That wasn't available to designers working with subtractive methods. You can build a construct that follows a certain topography, and that follows a certain geometry or a certain contour around a 3D geometrical design that is different than the traditional laminated flat structure that we're used to. There are some military and defense companies who are interested in putting material into unusual configurations.

Shaughnessy: What do you think it's going to take to get additive more into the mainstream?

Torp: It's a niche, right now. So, as far as the additive into the mainstream, you need more manufacturers and fabricators capable of deploying the technology and putting it in. It's somewhat like what HDI was in the early days—nobody really wanted to share how they did it. You're all competing for a competitive advantage early on, and then you start to get it into this standardization mode.

The standards committees will be vital in trying to get a set of standards, not only design guidelines, but a set of tolerances for manufacturability of it before it really starts coming into the mainstream. But, if you look at some of the technology that goes into such things as the Apple Watch, and the number of interconnects and sensors inside a relatively complicated device, it's phenomenal the amount of integra-

tion they're doing, in a very, very small space. There are not a lot of folks who can deliver that type of technology.

Until that level of technology gets embedded into the mainstream, it will be very difficult. Most of the technology, as Happy knows, is coming out of Asia Pacific, with some coming out of Europe. In the U.S., we're a little behind the curve from a manufacturing standpoint.

Holden: It's interesting to see that Nan Ya is going to invest something like \$600 million to

expand for ABF substrate. Are you working with the ABF film?

Torp: Yes, we're playing around with it and having some success, but we have more to do before we build a construct completely on the ABF film. It's similar to what we're doing on the polyimide.

Matties: Dave, this has been great. Thank you.

Torp: Thank you all. DESIGN007

It's Only Common Sense

How to Develop Great Leaders



by Dan Beaulieu

Editor's note: I-Connect007 columnist Dan Beaulieu focuses his weekly column on helping electronics companies enhance their professional and technical image.

In this column, he takes an inward look at how companies can upskill their employees into leadership positions.

As we know, the biggest challenge facing any business today, no matter the industry, is the lack of good, qualified people. An even bigger challenge than that is finding people to lead those we already have on board.

There are just not enough good leaders today. Notice I did not say managers; I expressly said "leaders" because there is a huge difference. Managers manage people while leaders not only manage people but inspire them as well.

A great leader creates a clear and concise vision of where the company and her team are headed. They spend a lot of time, in fact most of their time, with their team helping them to see the vision and then inspiring them to do their best to achieve that mission. Here's what I see about great leaders.

- Great leaders inspire
- Great leaders create visions
- Great leaders motivate their team to go the extra mile
- Great leaders show the way step by step
- Great leaders are great teachers and mentors

- Great leaders create a circle of trust with their team
- Great leaders have high values and pass those values on to their team
- Great leaders create passion in their teams
- Great leaders attract the best people
- Great leaders bring out the best in the people they lead
- Great leaders create great leaders

That's the thing I want to talk about today: developing great leaders.

Just as it has become more difficult to find good people, it is that much more difficult to find good leaders. To meet that challenge, companies have been forced to develop their own, to develop them organically. In my opinion, this is the best way to go.

As I have mentioned several times in this column, I have been looking for ways to help companies with their labor challenges. I have been watching webinars and reading books about creating great teams through great leadership by people much smarter than me.

I read at least six books about leadership and then came across a very good book the subject by famous industry guru John Maxwell. His book titled Great Leaders Ask Great Questions: Your Foundation for Successful Leadership, has this excellent section on how to develop leaders.

The following guidelines (in my own words) were inspired by John Maxwell's book.

To read the rest of this column, [click here](#).

Designing Additive and Semi-Additive PCBs

Feature Article by Cherie Litson
LITSON1 CONSULTING

With components getting smaller and electronic devices becoming more compact, we are reaching the physical limits of the typical etched fabrication processes. To address these limits, new additive and semi-additive processes are being developed to fit into the current fabricators' production lines without too much disruption or extra cost.

That leaves the design engineer with a few questions: Will additive and semi-additive processes really reduce layer count and sizes? Are there signal integrity and impedance advantages and disadvantages? When does it make sense to switch to additive or semi-additive? Are my DFMs going to be any different?

Answers to these questions and many more are still being developed. However, I've found a few answers that I'm happy to share with you.

First, let's look at liquid metal ink. LMI is ultra-thin and ultra-dense, conforms to any 3D

surface, works with different pure metals and their alloys (copper, gold, silver, palladium, platinum, etc.), and is non-aqueous, which enables low-cost manufacturing.

Here are some fundamentals for these very small features. Figure 1 depicts some examples of the additive processes used to create fine copper traces on a printed circuit board. One of the first things you'll notice are the shapes of the traces: They are not trapezoidal. Figure 2 shows close-ups of traces created with additive processes.

Will they really help to reduce layers? Yes, and you still need a good plan for your layer stackup and routing schemes. Everything is just a little different. When the traces get smaller, your dielectric gets thinner. So, it's best to use these either on the outerlayers (foil top designs) or on an inner core pair. They're great for breakout of fine-pitch parts. Just be

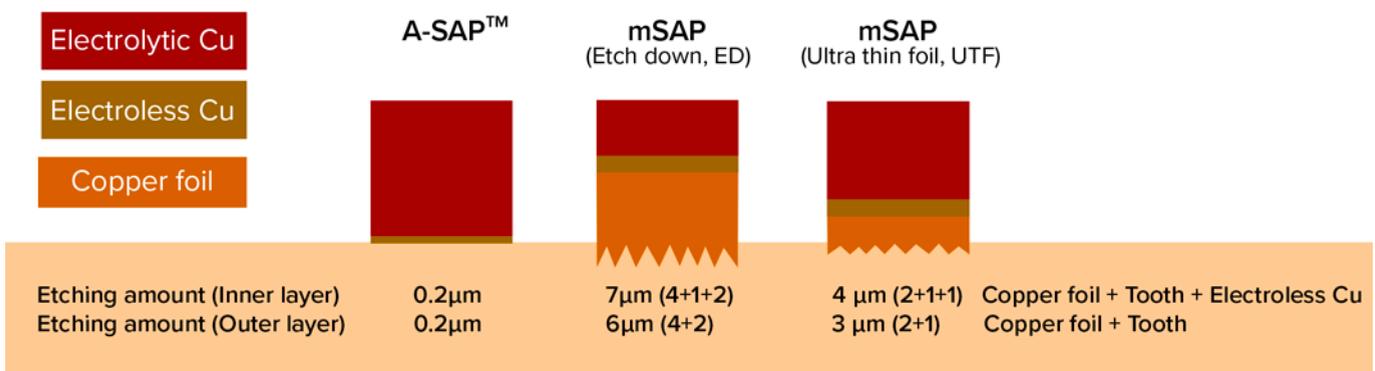
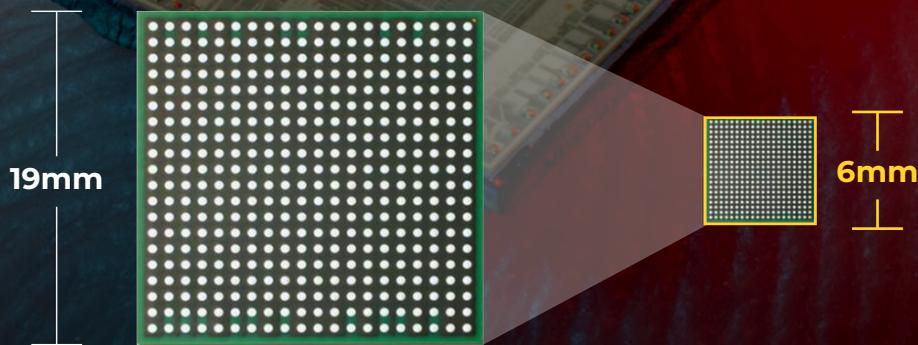


Figure 1: A variety of examples of additive processes.

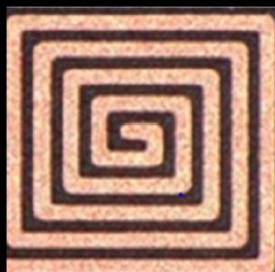
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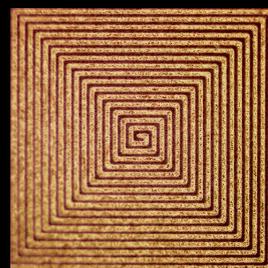
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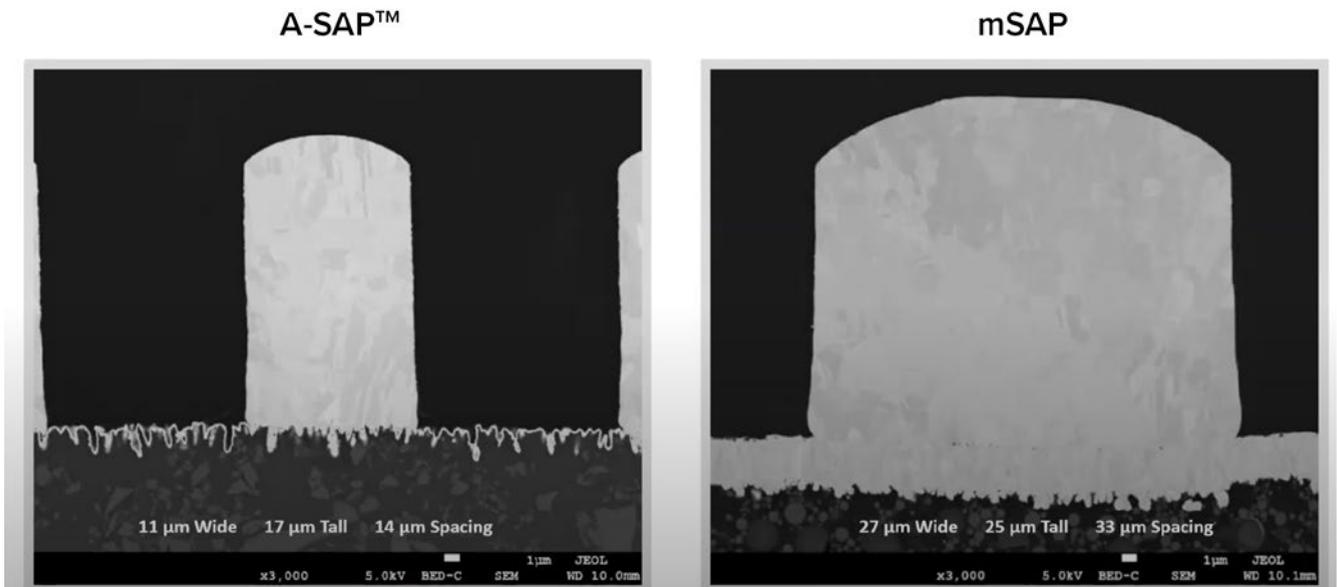


Figure 2: While traditional subtractive traces are trapezoidal, additive traces have straight walls.

sure you leave enough room away from the component pin to allow the solder mask to cover the trace and not your pin. That's usually about a 1.6–2 mil (40-50 micron) space to the trace. Then you can place the traces down to 1 mil apart (25 micron), impedance depending (Figure 3).

Are there signal integrity or impedance advantages and disadvantages with additive? Yes, but it depends on how you look at it. Thinner dielectrics mean thinner boards. This

could be positive or negative, depending on your mechanical needs. Current SI calculators don't want to work with a trace width that is smaller than the thickness of the copper.

Speculations are that the high aspect ratio can reduce insertion loss and improve coupling of differential lines, as there is less friction to the material surface. The narrow spacing can improve inductive and capacitive coupling—the only thing between the traces is resin, no glass. The process itself allows very precise

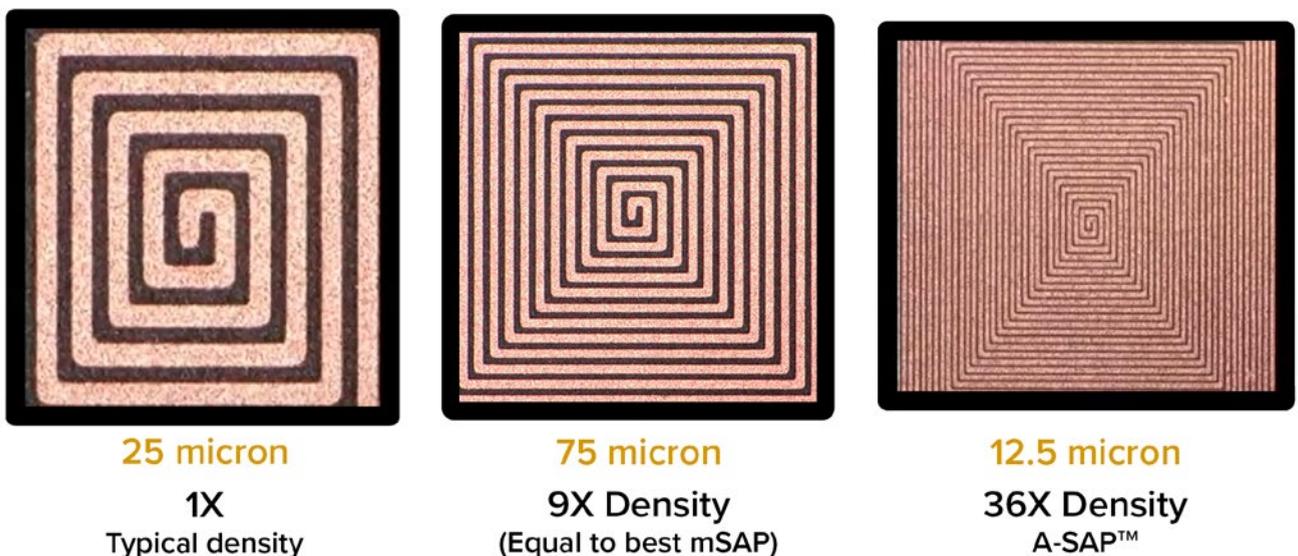


Figure 3: Additive and semi-additive processes permit line and space densities up to 36X that of typical subtractive PCBs.

control of the trace/space and can offer tighter control of impedance variations. Now we just need the calculators out there to tackle these new geometries.

When does it make sense to switch to additive or semi-additive? When you can't get the signal trace density with the current process, or when you can't break out from that 3.5-mm or 3-mm pitch BGA. Don't go there if you only have one component at that pitch. Get a bigger component package instead. For DFM's sake, don't mix small-pitch parts with large power parts on the same side of the board. That will give any assembler nightmares and cost you extra. Also, consider switching when you have very flexible products, need a circuit on a different type of material (like aluminum), if you need to add copper onto a 3D-printed surface, or create an ultra-smooth conduction surface.

Are my DFMs any different? Yes and no. There are a few things that need to be considered. Normal DFMs still apply. All the typical output files can be generated the same as you would for a subtractive process. You will need

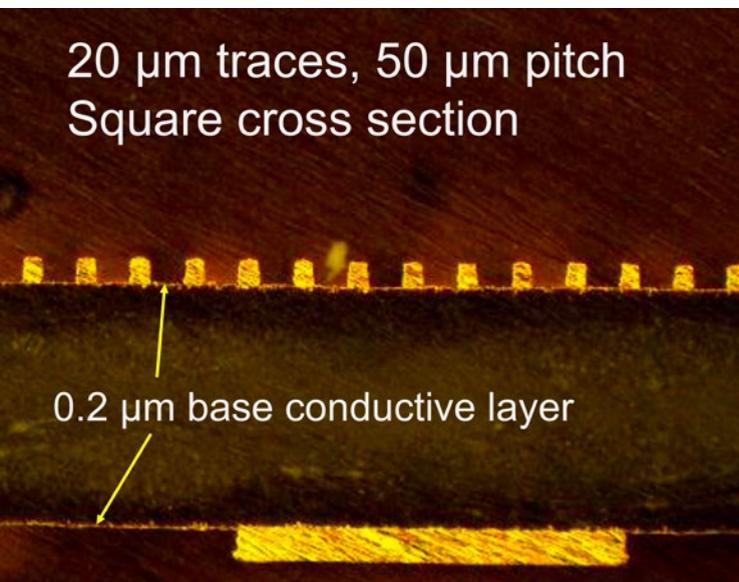


Figure 4: A -section of an additive PCB.

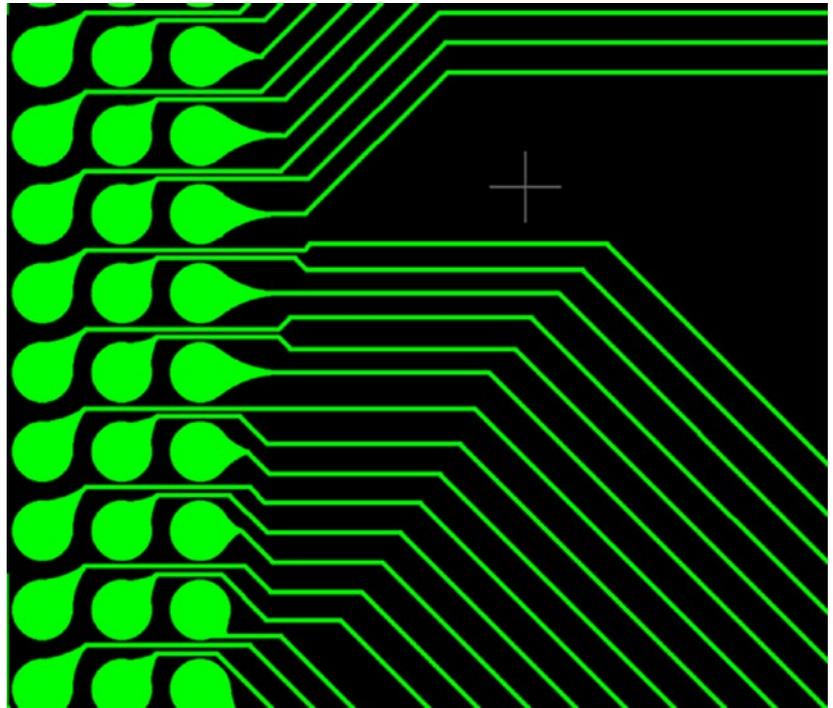


Figure 5: Designing additive and semi-additive PCBs is much like designing traditional PCBs, but with a few important twists.

more notes and direction to your fabricator. You will need to work with a fabricator who has experience with additive or semi-additive processes, and you will need to look deeper at the layer stackup and component placement planning.

I'm compiling a set of DFM guidelines now, and it's not quite done yet. I'll have more information about additive processes in my next article for *Design007 Magazine*.

Get involved with additive design. As miniaturization continues past the practical limits of subtractive etch, additive and semi-additive processes are likely to become more mainstream. **DESIGN007**

All images used in this article courtesy of Averatek.



Cherie Litson, CID+, is the founder of Litson1 Consulting and an instructor at EPTAC and Everett Community College. Cherie has more than 30 years of design experience, and has been an instructor since 2003.

Additive Manufacturing Requires Additive Design Techniques

Feature Article by Luca Gautero
SUSS MICROTEC

Although I am not a designer by trade, I want to share my thoughts on what additive manufacturing means for designers, especially how it relates to solder mask. The following are the topics I feel are most important to address.

1. Definition of Solder Mask

By its nature, the definition provided by any EDA tool is a negative one; the CAM vector files specify what goes away from an assumed continuous surface. Until now, solder mask has always presented itself as subtractive. SUSS MicroTec developed a front end, JETxSMFE, that can operate at the CAM station to smooth out manufacturing. The software understands

all of this, managing the details correctly on the incoming files.

2. The Advantage of Inkjet Solder Mask

One advantage of inkjet solder mask is to avoid any filling of holes or vias. Another way, maybe an annoyance to some, is to say that “tenting” is not possible. Still, the consensus is that solder mask-free vias improve a board’s reliability (Figure 1). The JETxSMFE removes solder mask at declared holes. Undeclared drills, which might still exist depending on the manufacturing convention on the production floor, will result in ink on the print table. This is not a big issue as a scraper easily removes excess solder mask, and alternatively, replacing the table or its liner (if present) gets the job done. However, both solutions lead to a small downtime. Long story short, if you want friends on the shop floor, be sure to have all the drills in your design.

3. The Dam Dogma

These small solder mask traces on laminate are supposed to separate two nearby copper pads. Such a pattern indicates the non-solder mask defined (NSMD) pad design choice. However, this choice involves several constraints, and these create an artificial need for narrow dams. From my earlier example, this time with numbers: Imagine two pads, 200 μm apart, nothing extreme.

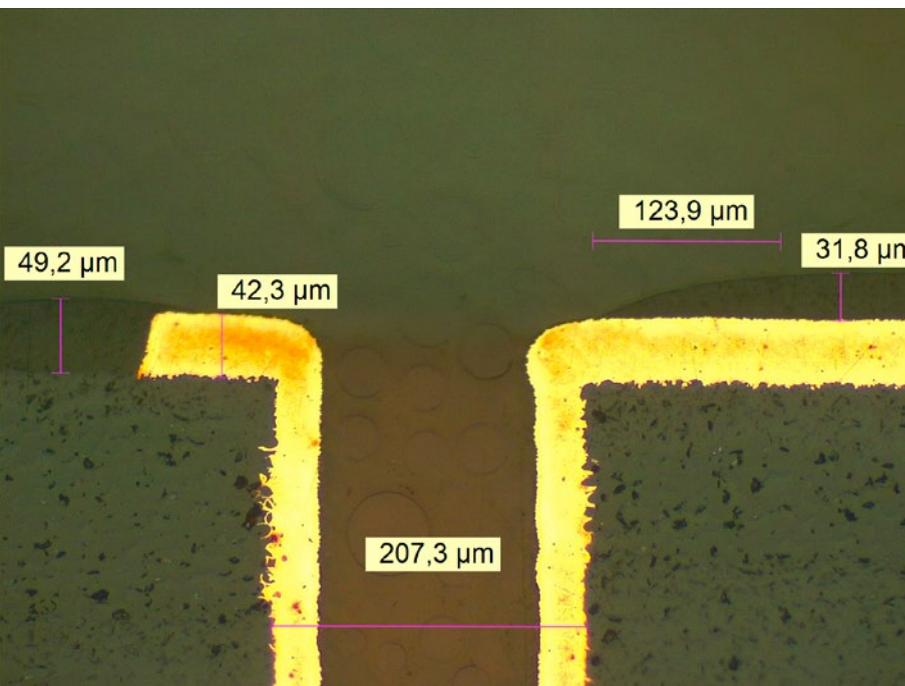


Figure 1: A cross-section of a via after solder mask coating. The trace connecting the pad extends further on the right side and is covered by solder mask. (Source: ACB-Atlantec SAS)

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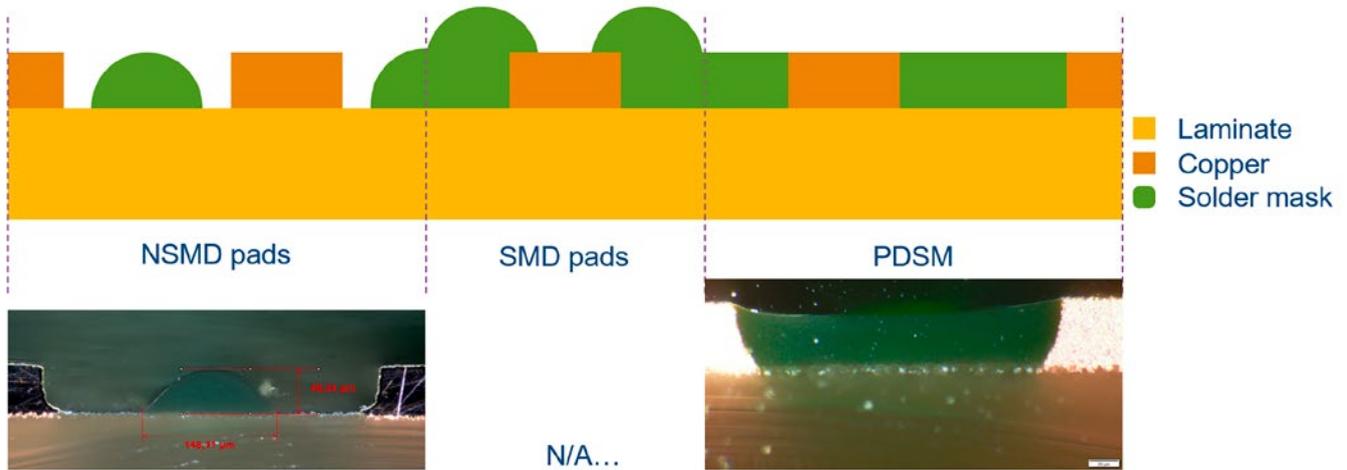


Figure 2: The choices are depicted here as a sketch and as its resulting cross-section.

What is the maximum size of a dam between these two? Assuming that LDI technology is used, the dam size results from applying the state-of-the-art constraint of the technology. This 200 μm pitch decreases by the laser beam width plus the registration accuracy twice—one for each pad. Therefore, it quickly comes down to 100 μm . Any more challenging a pad distance will also make it harder to define a dam.

From this reasoning, the many requests to create 50 μm dams or less with traditional technology seem legitimate. So, what do we do with inkjet printing? Does it join the race to the last micrometer? No, instead it challenges the initial design choice, which already spurs debate¹: Will it be solder mask defined (SMD) pad or NSMD pad? Neither of the two. Instead, it will be pad-defined solder mask (PDSM). Unfortunately, this acronym is not a thing yet, so there is no point in googling it. Inkjet is a volume-driven coating technology, which means that filling gaps is possible and, in this case, even encouraged.

4. Defining the Thickness

The definition of thickness means that the spectrum between coating conformality (Figure 3) and topography-

independent flatness can be seen (Figure 4). What is the best choice? What solution of thickness design would better fit the solder mask requirements? PCB designers know exactly what the tasks of the solder mask are². Still, the “inkjet upgrade” reviews the basics: While copper without solder mask can oxidize, laminate does not. Copper traces with high voltage without solder mask could create short circuits while bare laminate does not. Therefore, laminate does not need solder mask. The reasons for the solder

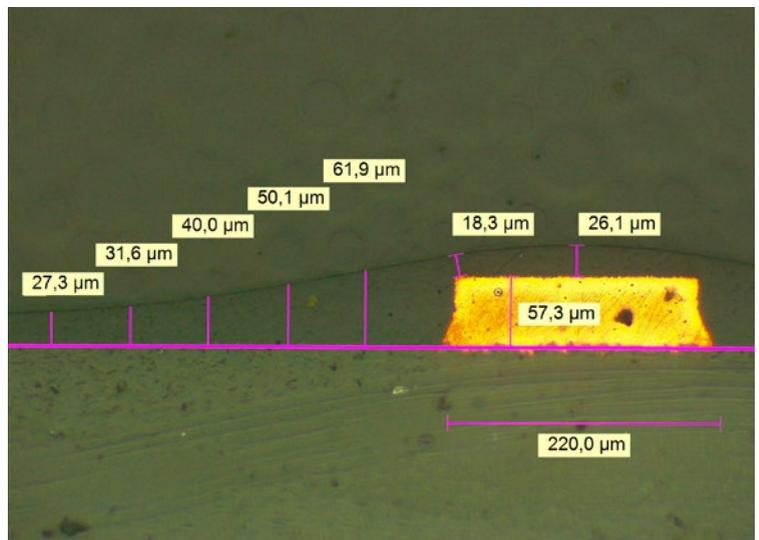


Figure 3: Laminate and copper coating meet the target thickness of 23 $\mu\text{m} \pm 5 \mu\text{m}$. The thickness transition between the two levels is chosen to exceed the target thickness to ensure mechanical stability. (Source: ACB-Atlantec SAS)

When combining the idea of constant coating thickness and the PDSM proposed earlier, a novel level of compactness can open for ball grid array (BGA) structures.

5. Design Rule Check

Here is a mélange of considerations which fall under the category of design rule check, where the CAM software will eventually implement them. However, their description here might avoid misunderstandings in the future. The designer will have to know that:

- Solder mask will have a minimum radius. Such radius depends strongly on the inkjet machine chosen.
- The smallest feasible gap between solder mask features is smaller than the smallest feasible printed solder mask feature.
- Thinner solder mask allows for smaller feature size; vice versa, thicker copper or a requirement of thick solder mask will increase the minimum feature size.

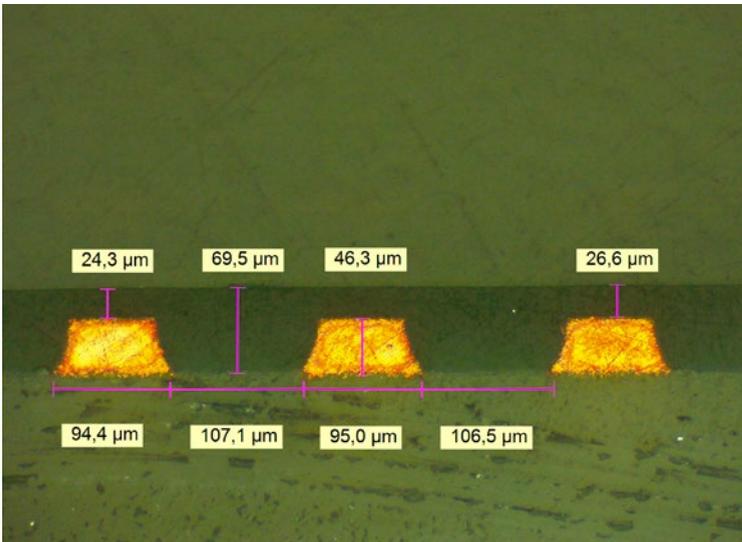


Figure 4: An example of a solder mask profile independent of the copper traces.
(Source: ACB-Atlantec SAS)

mask coating are convenience (less developer chemistry use) and the need to support any stencil frames. The first is no longer a problem, since inkjet does not use developing chemistry; the second has an elegant design solution: meshes or arrays of shapes to provide the same support with significantly less material coated.

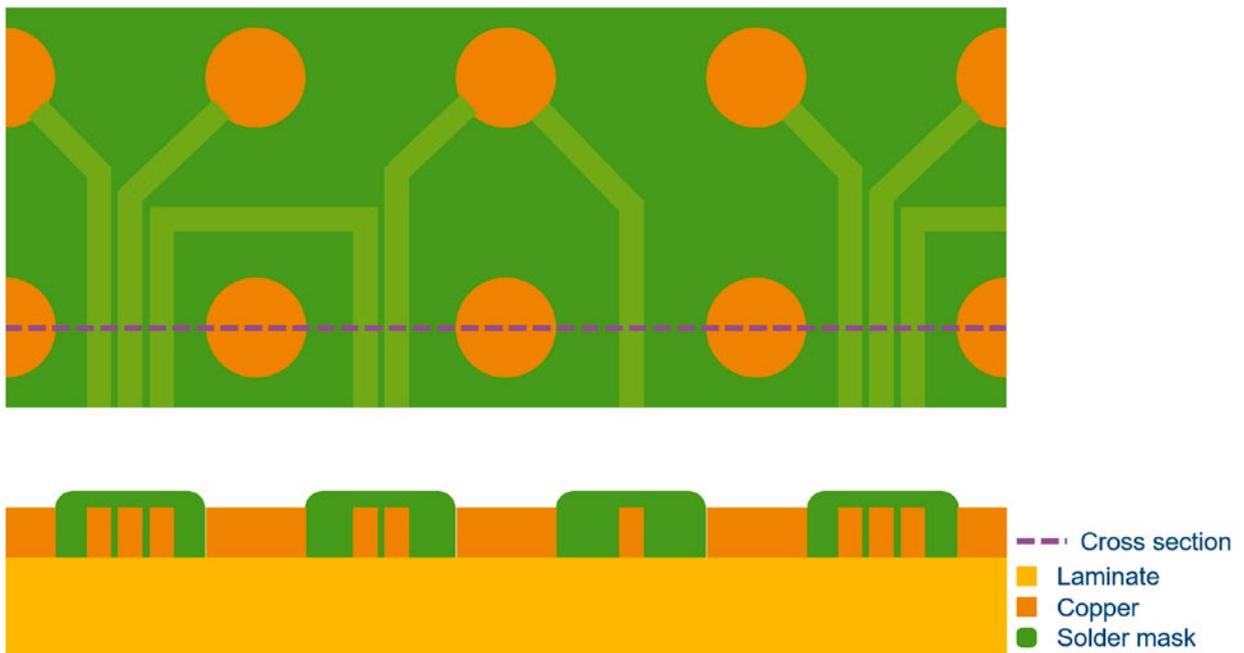


Figure 5: What about a more relaxed BGA structure? The traces between pads can have a reduced pitch since inkjet will place a defined volume of solder mask.

- The cross-section of a narrow solder mask feature resembles a dome (Figure 2). The traditional rectangular cross-section is no longer present. Instead, an edge-less, cavity-less profile replaces it that increases mechanical stability and chemical inertness.
- The structuring of the solder mask is based on layers. This means that additional geometrical features on top of the solder mask for mechanical support of components or confinement of dispensed coatings are also possible.

As mentioned, today's CAM solutions cope with the details mentioned above: solder mask thickness, copper thickness and holes. However, it is not yet the right place for defining it. Eventually, it should be something integrated in the CAM software for manufactur-

ing or, even better, already in the designing tool. The final dream is that the components themselves would impose on each location the desired solder mask thickness. This would make it all come together. Designers will put components to rest in peace, this time without a tombstone. **DESIGN007**

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Luca Gautero is product manager at SUSS MicroTec (Netherlands) B.V. and an I-Connect007 columnist. To read past columns or contact Gautero, [click here](#).

Trouble in Your Tank

Additive, Semi-Additive and Subtractive Fabrication

Feature Column by Michael Carano

It seems the operative word today is additive circuit board manufacturing, or for that matter, additive for everything. It is true that the use of additive manufacturing technology has found its way into different industries. While there may be several advantages to adopting additive technology in various industries, one should take a step back and truly assess where we are today in relation to conventional and advanced printed circuit board technology. It makes sense to understand the differences



between fully additive, semi-additive, modified semi-additive (mSAP) and subtractive. In the end, there are several options available to the fabricator and OEM to achieve high density and ultra-density circuitry to support higher end technologies, including IC substrates.

Overview

In my opinion, there is much confusion with respect to additive fabrication for printed circuit boards. Well over 45 years ago, there was full build (or "fully additive") circuit technology. One could employ a special pre-catalyzed substrate and build up the circuitry with an electroless copper process. However, the circuitry would still need to be formed via subtractive process.

Preceding the full build electroless process was the CC4 technology. A microroughened substrate was coated with a metal catalyst, then plated to 25-plus microns over a 24-hour or so period.

To read this entire column, which appeared in the February 2022 issue of *PCB007 Magazine*, [click here](#).

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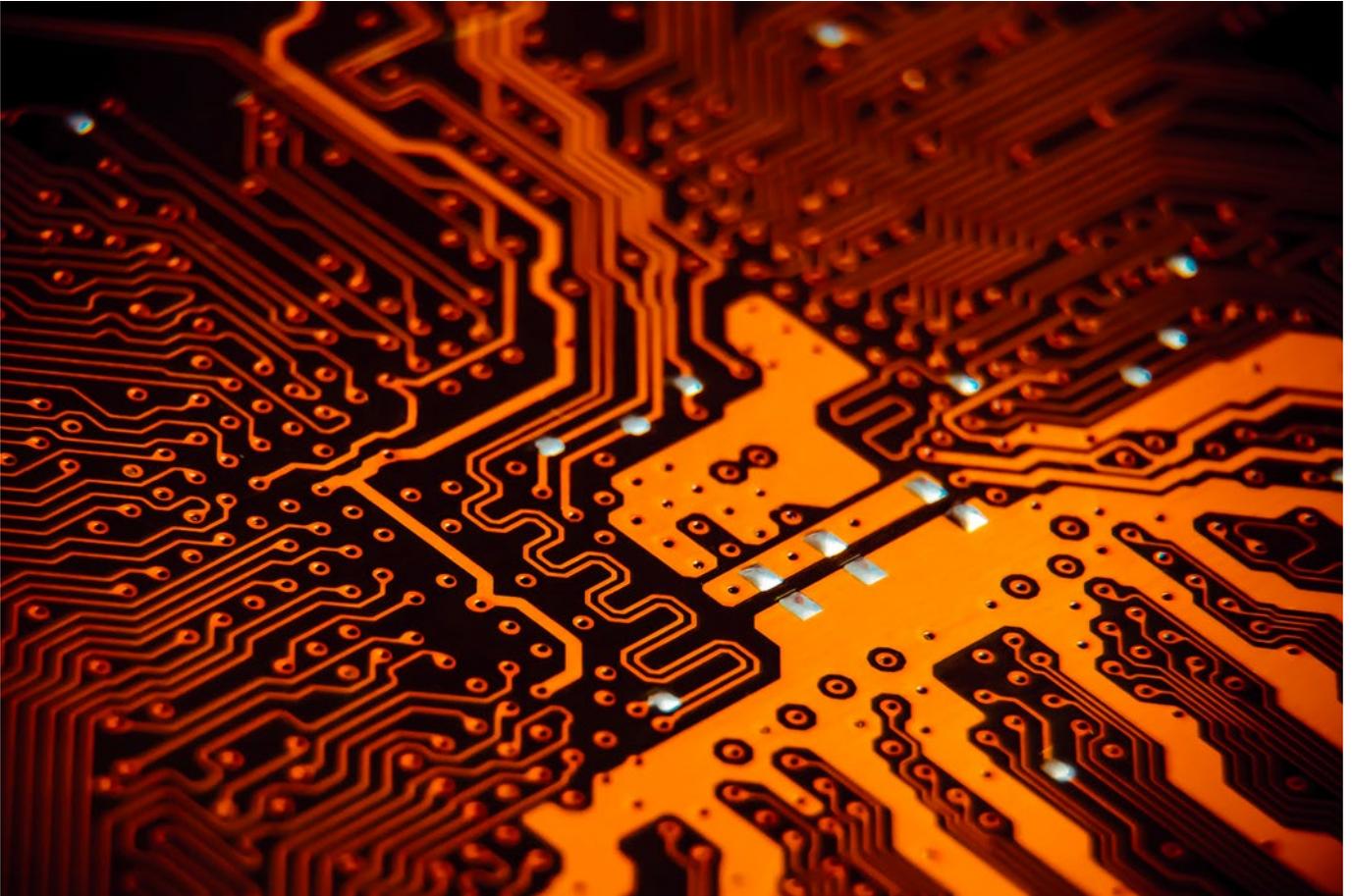
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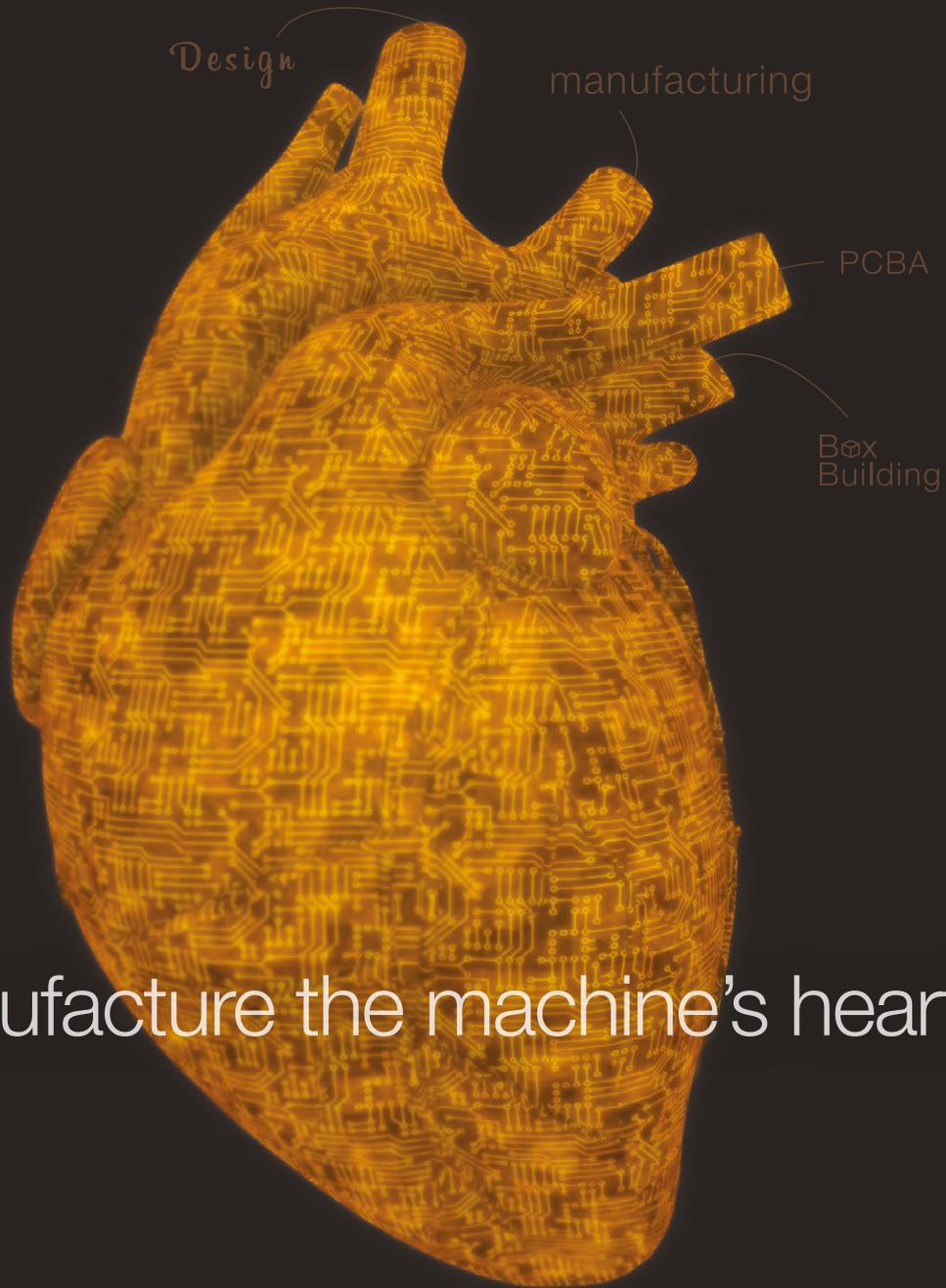


Feature Article by Tomas Chester

CHESTER ELECTRONIC DESIGN

Advances in technology have been clear to see within the component packaging industry, as the ball grid array (BGA) package sizes reduce from 1.0 mm pitch to 0.8 mm, 0.4 mm, and even beyond. However, while these improvements have occurred with component packages, it has become increasingly more difficult to break out and route the dense circuitry associated with these parts. Currently, the high-density interconnect (HDI) method typically used for the breakout of such parts has been to create the smallest possible subtractive-etched traces with microvias to allow for connections and escapes on the innerlayers of your PCB.

Now there are new fabrication processes that change how we can approach some of these layout difficulties. Additive and semi-additive construction now allows us to get down below 0.075 mm trace and gap sizes easily and reliably, however, utilizing it brings its own series of challenges to the table. Before designers and engineers can start to use this technology, we need to understand the difference between the standard subtractive fabrication method and these new additive fabrication methods, as well as their respective design requirements for trace impedance, and the signal integrity impact from routing traces closer together.



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Subtractive vs. Additive

Let's start by taking a brief high-level view of the different fabrication processes. With subtractive fabrication, our PCBs start with a base layer of copper of some thickness already laminated to the substrate. Then copper is electrolessly plated onto the board's outer layers, including inside the drill and via holes. A design image is then applied, an etch resist plated onto the exposed traces and holes, after which etching will occur. This is our subtractive step, where we remove the copper in areas where there was no image applied. This is also the limiting step in the subtractive fabrication process, because as we etch vertically down through the copper, the etching agents also remove copper in a horizontal direction, under the applied design image. The result of this process is a final copper trace cross-section with a trapezoidal shape. The critical concern here is that if the trace height is half as tall as its width, likely the etching process will remove the trace.

The critical concern here is that if the trace height is half as tall as its width, likely the etching process will remove the trace.

With additive fabrication, the process can be imagined as similar to 3D printing. The PCB starts with no copper on the laminate material and is instead "built" up on top of a thin seed layer of electroless copper, or on top of a thin laminated copper foil. This not only allows for trace and gap sizes down to 0.010 mm; it also creates a trace cross-section that has a rectangular shape.

Thanks to the manufacturing process, with the formation of these traces now complete, our attention needs to focus on trace imped-

ance. Depending on the impedance calculation, our resultant value is based upon the width of the created trace and the height from the trace to its referenced return path. Whether the construction is stripline vs. microstrip, of course, has some impact here. Typical subtractive-etch processing provides us with an easy and established method for a 0.075 mm trace with 50 ohms of impedance, by utilizing a 0.050 mm thick dielectric material between the trace and its return path plane. This construction becomes significantly more difficult once we move down into sub-0.050 mm traces that you would find using additive fabrication; the dielectric material also needs to decrease in thickness to be able to maintain that 50-ohm impedance, which is where problems exist. Materials that thin, if they are available, are extremely specialized and expensive.

While switching to a coplanar waveguide approach for our trace impedance does offer some minor improvements, our dielectric material thickness still plays a major role in our final impedance.

Effects on Signal Integrity

To complete our overview of additive design, we need to examine its impact on signal integrity. The intended use for these micro traces is to be able to increase our density within our design and assist with dense components. With the decrease in the trace size down to micro traces, we improve our ability to route more traces in a smaller area. However, we understand from our impedance examination that our return path copper remains the same distance away, due to dielectric material thickness limitations. This means that the resultant field size that is created by signals flowing down our traces has stayed the same; however, we have pulled in our neighboring traces closer within that field to increase our design density.

All this comes down to a simple statement: Increasing our routing density also increases the opportunity for crosstalk and other signal integrity issues. To combat possible crosstalk

issues, our traces need to be as spread as possible, with return path guard traces where possible. If we need to have traces close together, we want to reduce any parallelism as much as possible by fanning out wherever possible. Finally, we want to group together traces that are a part of the same interface as this will assist with our noise immunity.

Armed with this knowledge, how can a designer or engineer start utilizing this new fabrication method within our designs? One of the first things to do is talk to your fabricator. At present there are a few different additive methods on the market, like A-SAP™ (Averatek semi-additive process) and mSAP (modified semi-additive process). Each of these has different potential, from trace width to trace heights, so an understanding of your fabricator's capabilities is important to enable design to the appropriate additive specification. The fabricator's capabilities define our minimum trace size, and we already have our crossover point of around a 0.075 mm trace width. Now, it is possible to have additive designs with larger trace sizes, just like it is possible to have subtractive designs with sub-0.075 mm traces; however, that 0.075 mm trace size is a good crossover point to consider switching to using additive design technology.

From experience, designing with additive traces is best suited for those tight or micro-component package breakouts. It results in a less expensive, more reliable PCB by enabling access to more of the component pins, without needing to increase the number of layers in the PCB. However, the focus needs to be within the package area; once you can route to free space, both trace width and gap should increase. This allows for a small impedance mismatch between the regular trace across much of the PCB, and the small breakout section within the package area.

A New Route

When routing boards that feature additive technology, a designer may experience a slight

mental shift away from the traditional routing method. Typically, once your board's shape, stackup, and constraints have been added into your design, each block or section of the design is then placed and routed on the outer layers of the PCB, with the intent of connecting most of these different routed sections using the internal layers of the PCB. With additive design, coplanar waveguides can be utilized, allowing for increased routing on outer layers of the PCB. This decreases layer count, reduces the number of vias, and maximizes the utilization of every layer.

With additive design, coplanar waveguides can be utilized, allowing for increased routing on outer layers of the PCB.

Conclusion

Additive and semi-additive processes offer a variety of advantages compared to traditional subtractive etch fabrication. These include spaces and traces as small as 0.010 mm, far smaller than anything possible with subtractive methods, and nice, rectangular-shaped traces instead of the old trapezoidal traces. But with increased density comes the potential for greater crosstalk and other signal integrity issues.

Additive and semi-additive PCBs are likely to become more mainstream. And any designer or design engineer can begin designing additive PCBs—with a little prior planning. **DESIGN007**



Tomas Chester is a hardware designer and founder of Chester Electronic Design.

Burning Questions About Designing for SAP

PCB Talk

Feature Column by Tara Dunn, AVERATEK

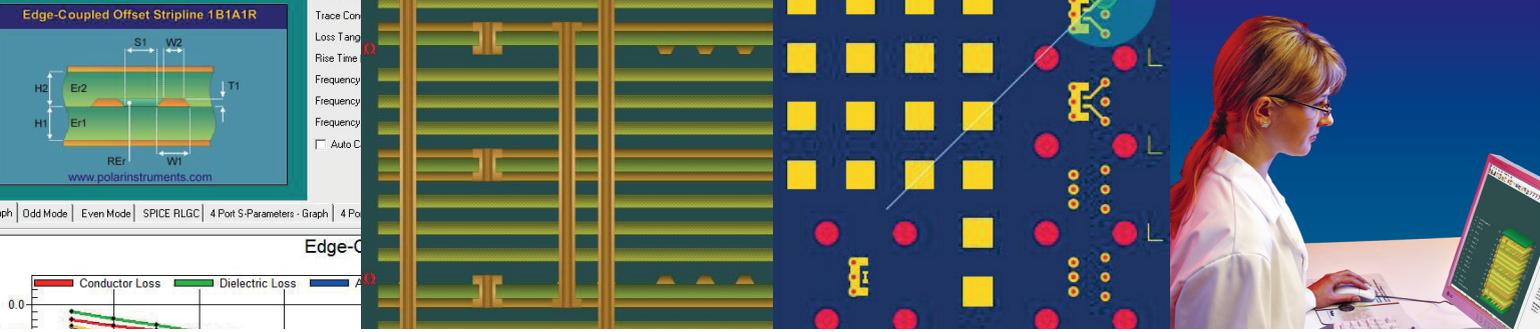
Do you have a smartphone? Most of us do. Did you know that most smartphones contain PCBs fabricated with mSAP (modified semi-additive process) technology? The ability for a fabricator to produce 35-micron feature sizes has long been taken advantage of by this consumer market segment. A handful of very high-volume fabricators specialize in this technology and serve the industry. But outside this high-volume market, SAP processes have not been widely available for other lower- to medium-volume PCB applications.

The good news is that this is changing. Fabricators now have access to both A-SAP™ (Averatek's semi-additive process for PCB fabrication) and mSAP, and the PCB design com-

munity is just starting to scratch the surface to find creative ways for this technology development to benefit next generation electronics. Reduced size, reduced layer count, reduced lamination cycles, and dependence on stacked microvias' increased functionality within the same footprint; the list of benefits can go on and on.

As the PCB design community embraces the benefits of this newly available printed circuit board fabrication technique, there are, of course, many questions to be answered. This column will address some of the most frequently asked questions related to circuit layer combinations and routing as people are introduced to this new technology.



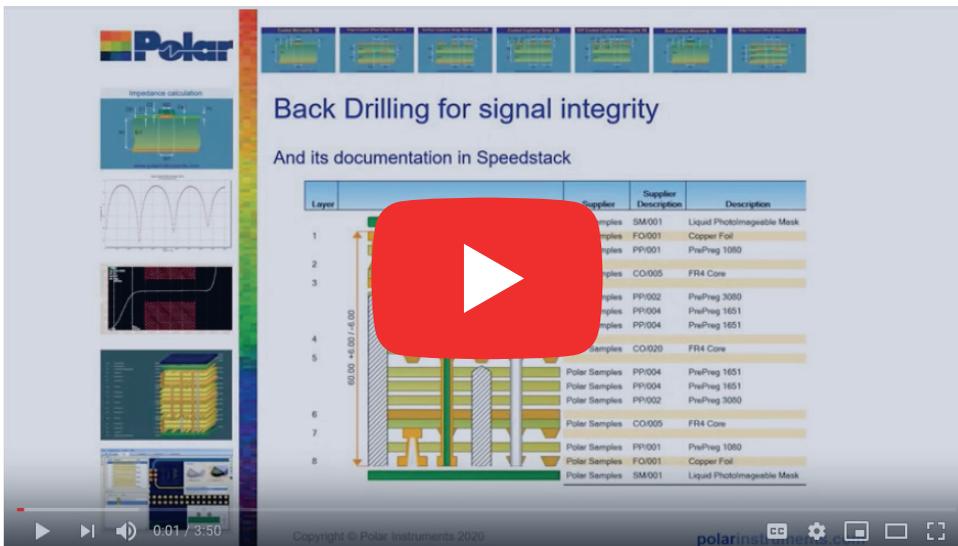


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What about power and ground layers? Do all layers need to be produced with these ultra-high density feature sizes?

It is most common to use a hybrid approach utilizing both subtractive etch layers and SAP layers in the same printed circuit board stackup. Stackups do not need to be all semi-additive or all subtractive. The layers do not need to be either one technology or the other. Typically, signal layers will utilize SAP technology, often to simplify the breakout of ever smaller BGA packages, reducing the number of layers and the number of lamination cycles required for the design. Traditional subtractive etch technology can then be used for layers that contain only larger feature sizes.

**It is most common to
use a hybrid approach
utilizing both subtractive
etch layers and SAP layers
in the same printed
circuit board stackup.**

Can SAP processes also produce larger feature sizes? Does the entire layer need to have the same trace and space dimension?

SAP processes can produce larger feature sizes as well. In fact, there are signal integrity benefits to these semi-additive processes that make this fabrication technique sought after, independent of the ultra-high density routing benefits.

Just a quick peek into the fabrication process: The SAP processes move the limiting factor for fabrication from the etching process to the photolithography process. Independent of the seed layer of copper selected, which may be a thin copper foil (mSAP), or an ultra-thin layer of electroless copper (SAP), the dry film

resist is patterned, and electrolytic copper is then used to form the printed circuit board traces that were patterned.

The lower limits of those trace capabilities and the tolerance of the circuit traces formed vary based on the process used. The mSAP processes, even with an ultra-thin copper foil, have a seed copper layer that is considerably thicker than the electroless copper seed layer used in the A-SAP process. Because the seed layer of copper needs to be etched where it is not required, the thicker copper will take longer to etch, which impacts the trace itself. Both the line width and space need to be larger with the mSAP process and the line width tolerance will need to be greater than with the A-SAP process. While both processes provide an improved line width tolerance, the A-SAP process with thinner electroless leaves the circuit sidewalls straight with no trapezoidal effect.

Tip: Adjust your modeling software to show traces with no trapezoidal effect and investigate how this changes the numbers. In fact, this should be a topic for a future column.

Can outer layers and plated through-holes be created with SAP processes?

Yes, a PCB designer can confidently design a printed circuit board with ultra-HDI features on outer layers and connect with reliable plated through-holes using the A-SAP process. When working with mSAP, circuitry on the outer layers is most often discouraged.

Fabricators building with A-SAP have been running regular lots of material using standard D-coupons with stacked and staggered microvias to help PCB designers and OEMs feel comfortable with the reliability of the plated through-holes created with the electroless seed layer of copper I've explained.

What is the minimum spacing from trace to pad (external layer)?

The copper-to-copper spacing can be a cost adder in subtractive etch processes. In the

semi-additive environment, this is not the case. There are a couple things to consider. First, on innerlayers, this spacing could be 25 microns or below, depending on the technology being used by the PCB fabricator.

Outerlayers need to take solder mask into consideration. There needs to be enough space to allow the solder mask to fully cover the trace and not expose any copper. The thickness of copper typically determines how far you need to be away from the pad. A good rule of thumb would be to use a 50-micron gap.

What do I need to know to meet a 50-ohm impedance?

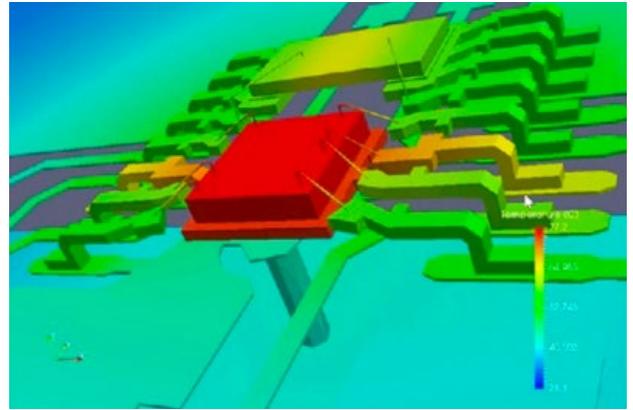
First, this topic will be addressed in a future column in much more detail. But I will tease a few high-level tips here. First, be sure that the modeling tool you are using is set for straight sidewalls if you are working with a fabricator offering A-SAP. This does have an impact. Second, pay close attention to copper height. Narrow traces will have higher loss, which is a fact, but decreasing dielectric thickness and increasing copper height do mitigate that. The ability to fabricate high aspect ratio traces (taller than wide) is dependent on the SAP technology used, so be sure to work with your fabricator as your PCB design develops.

There is a lot of work being done to help educate PCB designers about this new technology. This is our opportunity to design with manufacturing and to creatively approach these new capabilities both from a fabrication perspective and a design perspective. We will continue to dive into this in future columns, but please contact me with any burning questions. **DESIGN007**



Tara Dunn is the vice president of marketing and business development for Averatek. To read past columns or contact Dunn, [click here](#).

All Systems Go! Find and Fix Thermal PCB Problems Sooner Than Later



by **Melika Roshandell**
CADENCE

In an earlier column, “[Bridging the Gap Between Design and Analysis with In-Design Analysis](#),” Brad Griffin discussed how the “shift left” that’s happening with electronic design means it is no longer sufficient for signal integrity (SI) and power integrity (PI) analysis to be performed in isolation. Designing, analyzing, and verifying the design in its entirety is key. Another facet of this shift left is the need to address thermal integrity (TI) sooner rather than later. In other words, finding and fixing thermal PCB design issues early in the design process is necessary to save costs, reduce design spins, and maintain your own sanity.

Electrothermal co-simulation—understanding the implications (intended or otherwise) of thermal interactions on electrical performance for high-speed (or high-frequency) PCB designs—is now essential for successful end-product development.

Let’s start by looking at things from the highest level, which is that we want to design a PCB. At some stage, this PCB (possibly accompanied by one or more additional PCBs) will be mounted in an enclosure. Eventually, this system will be deployed into the field. The designers of the PCB(s) and the system as a whole want to know how well the system will perform and how long it will survive.

To read the entire column, [click here](#).

Leaning into Lean Manufacturing

Connect the Dots

by Matt Stevenson, SUNSTONE CIRCUITS

The worst part of the global COVID pandemic brought unpredictability and uncertainty to an otherwise stable PCB Industry. Like many in the board business, Sunstone faced increasing demand from essential businesses while also dealing with inconsistent employee availability and social distancing guidelines that slowed the manufacturing process. We knew immediately that even though the status quo had worked to this point, the situation was not temporary, and the operation would have to adapt.

Commitment to Lean Sustains Quality

We have been vocal proponents of the Lean manufacturing philosophy for some time, as it is a foundation for delivering quality to our customers. For the past few years, our Lean culture and adherence to Lean principles helped

Sunstone survive and excel during the most challenging business environment in recent memory. COVID renewed and expanded our commitment to Lean principles to sustain the quality of our work and maintain the safety of our employees.

Lean manufacturing is a set of guiding principles aimed at improving efficiencies and productivity—reducing waste in the process. As defined by the Lean Enterprise Institute, the five core principles of Lean are:

1. Defining value
2. Mapping the value stream
3. Creating flow
4. Using a pull system
5. Pursuing perfection

Lean builds more value into the PCB manufacturing process. Customers benefit from improved products and employees find themselves working in safer conditions. Our Lean work environment made it easier for us to adapt to changing safety requirements brought about by COVID. While many shops struggled with adapting manufacturing processes to social distancing guidelines, Lean practices helped Sunstone more quickly construct a safe, more productive workplace.

The core of Lean is the practice of identifying the true value of every component in the manufacturing process. The pandemic caused us to look more closely at the nature of each task, eliminating those elements of production that did not add value, but perhaps did present



Integrated Tools to Process PCB Designs into Physical PCBs



Visualize

Use manufacturing data to generate a 3D facsimile of the finished product.



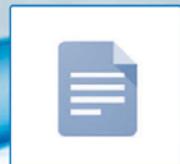
Verify

Ensure that manufacturing data is accurate for PCB construction.



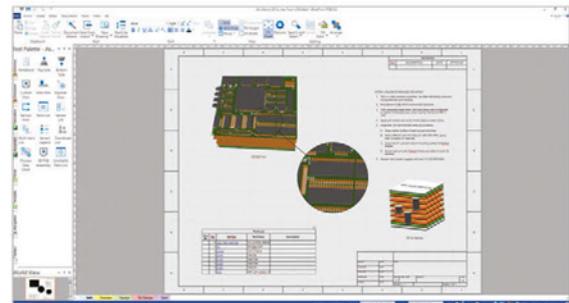
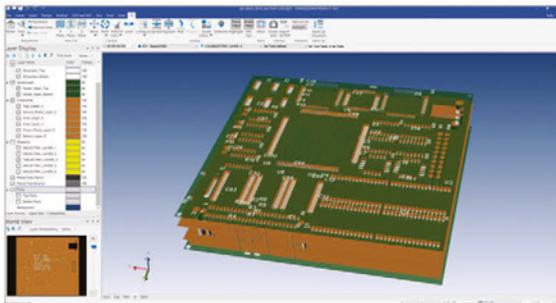
Panelize

Minimize costs in both PCB fabrication and assembly through maximum panel usage.



Document

Quickly and easily specify the PCBs form, fit and function.



CAM350

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BluePrint-PCB

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risk of transmission. This enhanced attempt to eliminate waste helped us become more profitable, improved employee productivity, and removed unease about COVID risk in the workplace.

Adherence to Lean Practices Makes the Difference

At the outset of the pandemic, we didn't really have a grand plan to reinvigorate all five Lean manufacturing principles. We just knew we had to adapt to the drastically changed operating environment. Focused on customer satisfaction and employee safety, we took what we were already doing and amplified it to meet each new challenge COVID brought with it.

There was no formal decree about using Lean philosophy to respond, but with the benefit of hindsight, it was clear that was exactly what we did. Like muscle memory that results from persistent training, we relied on our experience with Lean throughout. Even if our efforts to deal with COVID didn't always result in a classic Lean project or structured application of its principles, Sunstone's adherence to Lean manufacturing got us through the hardest times and put us on a path to come out stronger than when we went in.

Now, two years after the initial shutdown, we have maintained operations, kept all our employees healthy and employed, continued to satisfy our customer needs, and reacted quickly to environmental changes.

Dedicated Leadership Lights the Way

None of that would have happened without dedicated leadership across the organizational chart. Success with Lean has always required executive management commitment to the core principles. When COVID hit, that commitment was front and center, and communicated throughout the organization. We set expectations appropriately at every level, and recognized small, early victories to build momentum that would take us through the worst of the pandemic.

That momentum was sustained by clear, two-way communication throughout the organization. The great ideas for process improvement and safety enhancement come from the personnel doing the work each day. By keeping the channels of communication wide open, company leadership was ready to hear about opportunities to effect change.

Even with normalcy closer on the horizon, the competitive landscape of the PCB industry may be permanent. If last year taught us nothing, it was that economic disruption can come from anywhere. We can't predict what the next challenge will be, but we can be as prepared as possible before it arises. Lean offers a path to readiness, one that considers value for the customer and safety for the employee. By making Lean decisions on everything from equipment type to production floor layout in the midst of a crisis, we found ways to improve process we had never even considered in the past. **DESIGN007**



Matt Stevenson is the VP of sales and marketing at Sunstone Circuits. To read past columns or contact Stevenson, [click here](#).

The Printed Circuit Designer's Guide to... Stackups: The Design within the Design



Book Review by Skyler Sopp

If you have ever contemplated crosstalk, eye closure, power loss, or a list of other issues defined in this textbook, then you also need to understand what, why, and how stackups can and will impact your circuit's performance. After all, the stackup is one of the few things that directly touches every single part of your design; therefore, you must set yourself up for the highest probability of success by establishing a strong foundation through a well-designed stackup.

There are many incredible resources out there for those in the high-speed design industry: Eric Bogatin's *Signal & Power Integrity Simplified*, Lee Ritchey's *Right the First Time*, and a host of other books and websites. However, there is an apparent void in the realm of stackup design. How has industry gone so long avoiding such an important topic as one that influences everything on the board? *The Printed Circuit Designer's Guide to... Stackups: The Design within the Design* begins to fill the industry-wide void in an easy-to-understand overview that helps define the aspects that you as the engineer need to be thinking about when putting together a stackup.

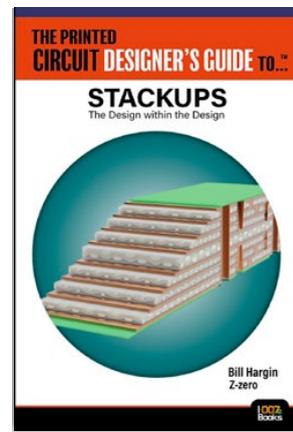
With 25 years of experience in PCB manufacturing and signal integrity, author Bill Hargin is an expert in the field of stackup design and it shows here. In Chapter 3, Bill shows how your dielectric of choice will directly impact your "eye." He explains the breakdown of how each variable contributes to the overall loss budget, then defines how he recommends material planning before any routing has begun. This book helps the reader establish the variables

of interest and the impact of those variables, and makes a recommendation on what to do about it so you can improve your future designs.

Boards are getting thinner, power requirements are increasing, and routing densities are becoming finer. You will need to make compromises in your stackup, so understanding that trade space is vital. This book breaks down concepts like board loss, material selection, impedance planning, and more to help you understand how each one of them will influence your design when fabricated. This book will assist you in learning how to make educated compromises earlier in the design cycle.

If you are a hardware or electrical engineer who is not already deeply invested in stackup design, this book is really for you. It is full of practical information, not bogged down by technical jargon, has easy to understand and useful images, and gets you off to the races quickly. Even the seasoned veteran will find this book a worthy reference for understanding when one needs to know things like the contribution percentage of each variable on impedance. Regardless of where you are in your stackup knowledge, I recommend [downloading the book](#) and reading it! It will be well worth your time and may just save you future headaches. **DESIGN007**

Skyler Sopp is a signal integrity engineer for Mercury Systems.



Designing for the SAP Fabrication Process

Beyond Design

Feature Column by Barry Olney, IN-CIRCUIT DESIGN PTY LTD / AUSTRALIA

PCB designers are continually challenged with demands for reduced product size. However, form factor-driven design pressures have been relieved, in part, by the increased use of high-density interconnects (HDIs), which enable more functionality per unit area than conventional PCBs. Leveraging finer lines, thinner materials, and laser-drilled vias, HDIs have played a crucial role in device miniaturization. However, the traditional PCB subtractive etch processing becomes very difficult for feature sizes below 3-mil trace/space. This forces PCB designs to become more complex as electronics packages shrink—adding extra routing layers and microvia layers, and increasing the number of lamination cycles required, which impact yield, reliability, and thus cost.

As smartphone technology evolves to 5 Gbps, the PCB industry's approach to HDI manufacturing has also evolved. Vast multiple input/output antenna configurations and increasingly complex RF front-ends expand

the RF content footprint. The higher bandwidth inherent to 5G requires much stricter impedance control. If not formed with extreme precision, the thinner traces of HDIs can introduce an increased risk of signal degradation. To fulfill these demands, the amount of available space for HDI PCBs, within 5G smartphones, needs to be significantly reduced.

The semi-additive process (SAP) is a production-proven method used on low dissipation loss (Df) build-up materials that enable the manufacture of ultra-fine-line circuitry. This technique utilizes additive process steps, adding copper to the base dielectric, rather than subtractive processes to create the circuit pattern. Fabricators previously only able to offer 3-mil trace/space can now reliably produce 1-mil trace/space and below. Further reductions required the adoption of various SAP manufacturing processes commonly used in the IC substrate industry, including laser direct imaging (LDI), improved laser drilling,

extremely thin copper foils, via fill pattern plating, and flash etching, into a process called modified SAP (mSAP).

SAP enables the printed circuit board fabricator to employ an additive screen process instead of an edge-removal, etched process—the end result is a PCB design that can dramatically reduce area, layer

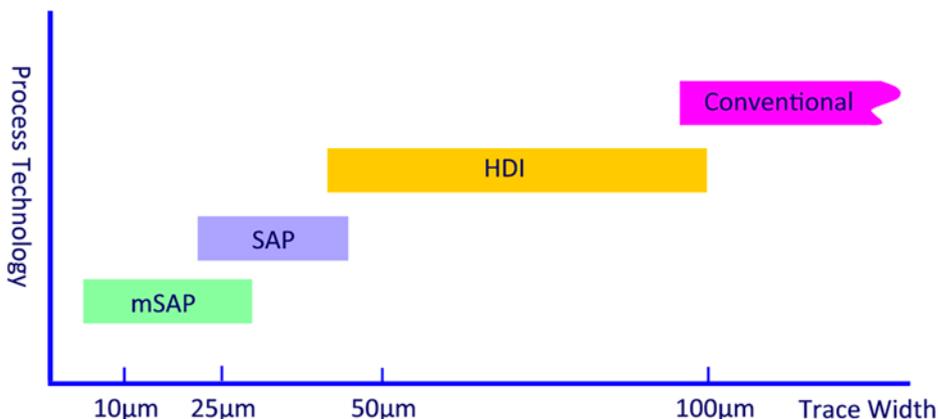
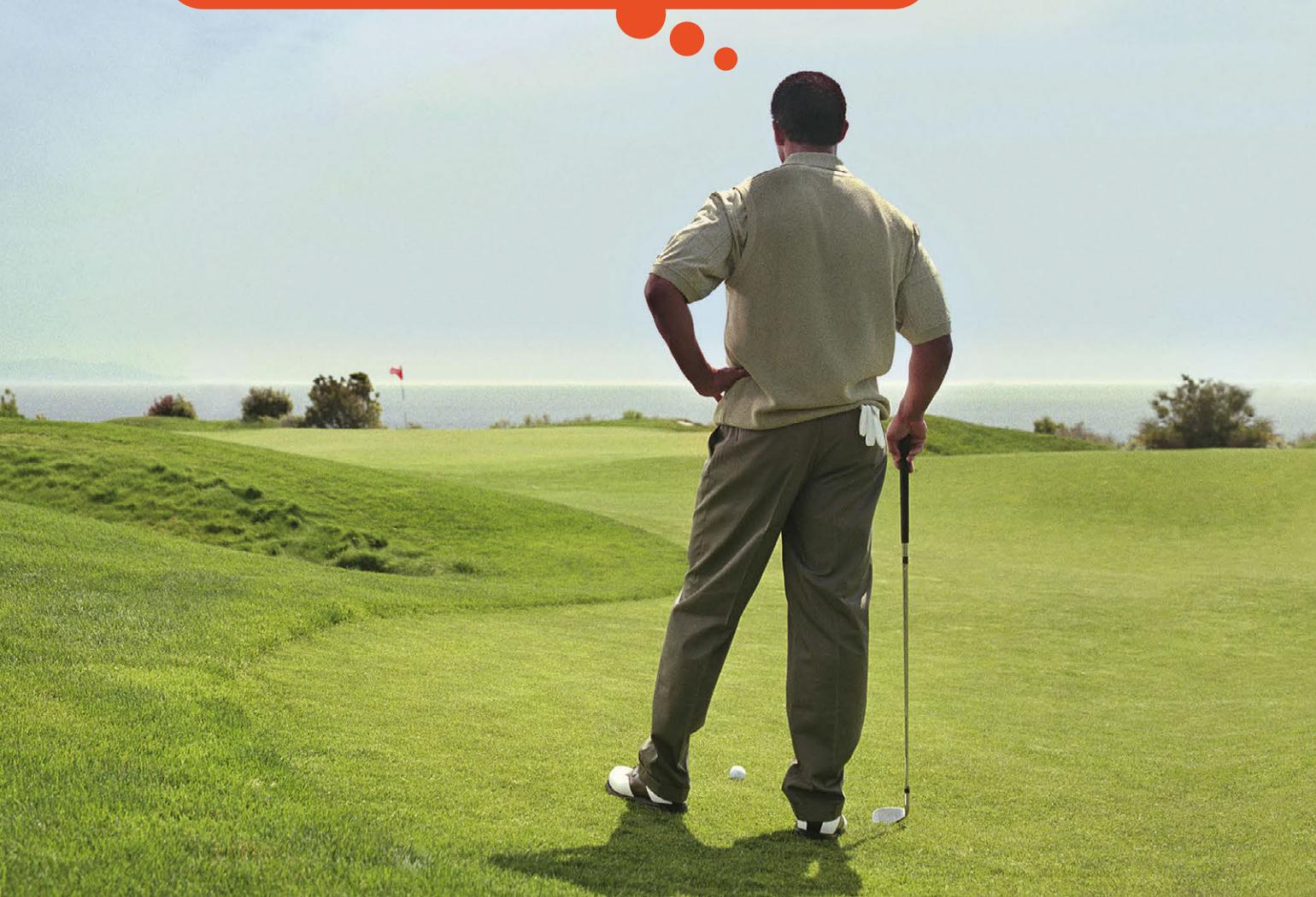


Figure 1: Trace width vs. process technology.

Hmm, what is recommended
**minimum distance for
copper to board edge?**



PCBs are complex products which demand a significant amount of time, knowledge and effort to become reliable. As it should be, because they are used in products that we all rely on in our daily life. And we expect them to work. But how do they become reliable? And what determines reliability? Is it the copper thickness, or the IPC Class that decides?

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count, and weight of electronics products, as well as provide significant RF benefits. Figure 1 shows the trace width for the available technology processes.

The smartphone, tablet, and wearables markets have advanced the mSAP processes to be compatible with high volume PCB fabrication. Current designs merge both subtractive-etch processing and mSAP processing. This combination is crucial to the thinner, smaller motherboard design which frees up space for a more robust battery. A technology teardown of the Gen 11 iPhone X shows trace/space designed at 1.2 mils (30 μm) and more advanced designs have 0.4 mils (10 μm) features. That is a complete game-changer for PCB design.

SAP provides tighter line width control and straight conductor sidewalls, greatly improving impedance control. In a subtractive process, fine lines are formed by coating the copper layer with an etch resist where the copper should be retained and etching away the remaining copper. The main drawback of this approach is that the chemical etchant used to vertically etch the lines will also dissolve the copper in the trace walls. In a cross-section view, the resulting traces will appear trapezoidal (Figure 2).

With SAP, a much thinner copper layer is coated onto the laminate and plated in the areas where the resist is not applied. The thin copper remaining in the spaces between conductors is then etched away. The traces are formed with much greater precision, in straight vertical lines, yielding an almost rectangular-shaped cross-section that maximizes circuit density

and enables accurate impedance control with lower signal loss. With traditional subtractive etch processes, controlled impedance is typically specified with a $\pm 10\%$ tolerance due to variation in the material and the process. With SAP, the line width tolerances are much more tightly controlled and controlled impedance can be held to a stricter tolerance.

The standard SAP process utilizes some roughening or texturing of the dielectric substrate to achieve sufficient adhesion; however, the rough surface at the plating/resin interface potentially increases transmission loss at high signal speeds. To promote the signal integrity of high-frequency signal transmission, the SAP process should provide high plating-to-resin adhesion as well as a very smooth interface in between. Consequently, the copper roughness should be kept under 1 μm .

Routing channels between BGA ball contact lands is progressively restricted as the contact pitch is reduced. Some suppliers of FPGAs understand the challenges facing the PCB designer in signal routing and have maintained a constant 0.30 mm contact diameter to maximize conductor routing channels on the outer surface of the circuit board. Even though smartphones and tablets may have stabilized in size and the trend is more toward system-in-chip than it is toward further shrinking, we definitely will be seeing more chips with pitches of 0.30 mm and less.

Generally, PCB designers can only route to the outer two rows of lands on the perimeter of a BGA using HDI technology. Squeezing one signal trace between BGA lands or break-

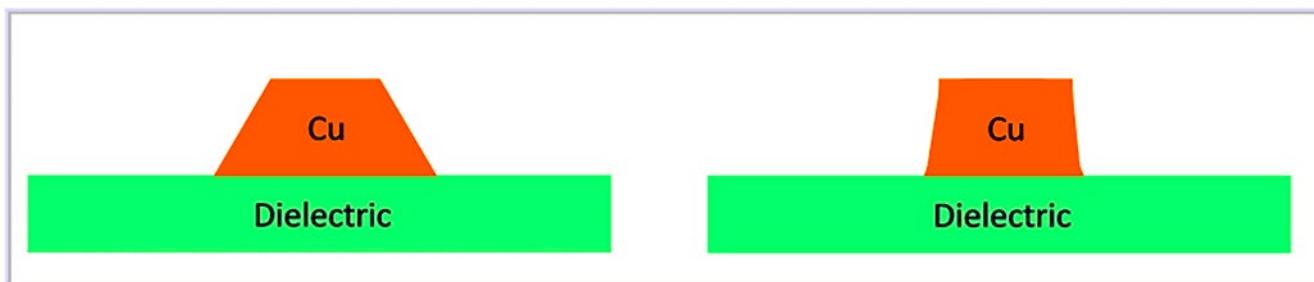


Figure 2: Trace geometry for the subtractive (left) and additive processes (right).

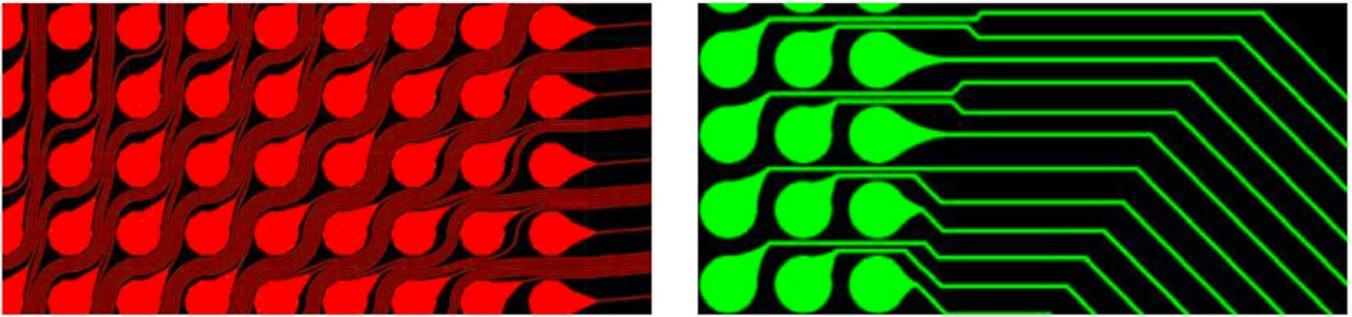


Figure 3: SAP (left) vs. HDI routing (right). (Source: Averatek)

out vias has been the unofficial limit for typical low-cost multilayer boards for many years. Although, if you choose to pay a premium, then the limits can always be stretched as in Figure 3 (right). However, the SAP process promises greater freedom with six 1/1 mil trace/space between lands. Figure 3 (left) is a drawing of multiple traces routed between 0.3 mm pitch lands. However, this may be pushing the limit, not because of physical size, but rather because of signal integrity requirements for impedance and coupling. There are a few issues with tightly routed signal traces:

1. Unintentional coupling of parallel segments is extremely strong between 1-mil spaced traces. This might be fine

for grouped synchronous buses and data lanes but horrendous for unrelated signals. Figure 4 illustrates the exponential increase in crosstalk with tight coupling, particularly on outer microstrip layers.

2. The impedance of the trace must be maintained at 40–50 ohms and this is not possible with the standard dielectric thickness of HDI stackups. An extremely thin dielectric of 1 mil or less is required to maintain 50 ohms impedance with a 1-mil trace; this technology may not be suitable for standard HDI rigid boards. However, flexible circuits are ideal with Apexyl LPEN/LPET, Dupont Pyralux Flex, Thin-Flex A/H, Ultrflex GTS 7800, and Rogers

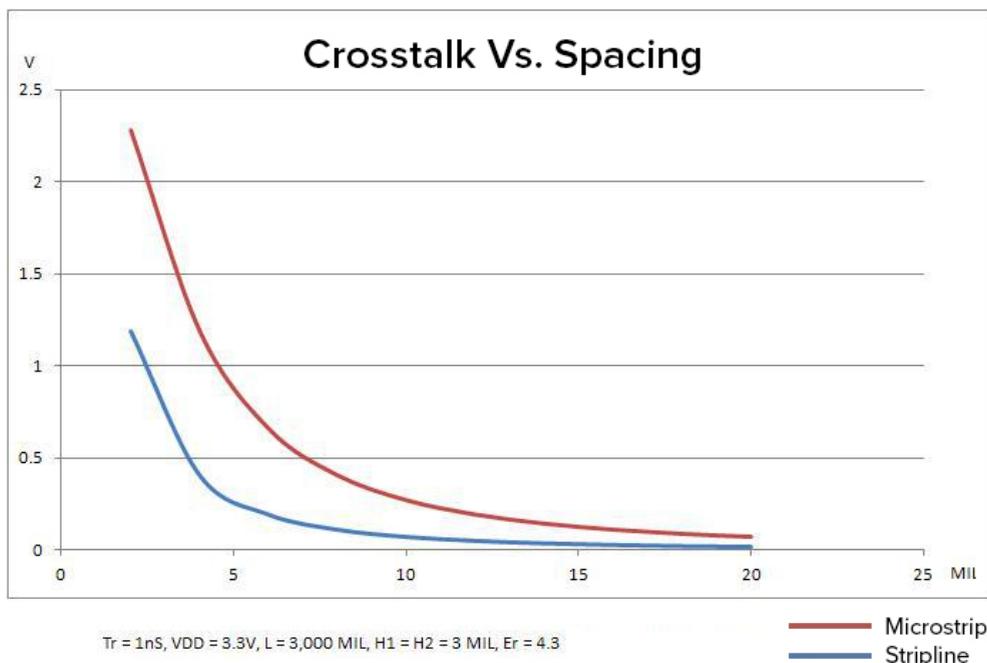


Figure 4: Crosstalk vs. spacing for microstrip and stripline layers.

R/Flex Crystal and Jade materials all providing low loss flexible materials of 1 mil thickness.

3. Unless all the routing is completed on the top (component) layer, breakout vias are still required—although the use of via-in-pad and blind vias dramatically reduce the real estate required.

There are also substantial signal integrity benefits from semi-additive processing. Tighter line width control and straight conductor sidewalls greatly improve impedance control. Also, the technology helps reduce parasitic inductance by reducing loop area, as well as increasing density. Fine-line precision RF features can also be realized with SAP technology.

3D printing of multilayer PCBs is also an additive process. With its game-changing technology, 3D printing allows free-form shapes, enabling you to find novel solutions to development challenges, thus enabling new devices and designs. It allows a seamless, one-step manufacturing process from digital design to functional devices. Plus, it enables printed 3D antennas/coils and eliminates loss-generators. Although 3D printing is currently limited to 3/4 mil trace/space construction, it has a huge advantage for prototype construction, of multilayer boards in-house, within a matter of hours.

Key Points:

- Form factor-driven design pressures have been relieved, in part, by the increased use of high-density interconnects.
- The traditional PCB subtractive etch processing becomes very difficult for feature sizes below 3 mil trace/space.
- The thinner traces of HDIs can introduce an increased risk of signal degradation.
- The SAP process is a production-proven method used on build-up materials that enable the manufacture of ultra-fine-line circuitry.

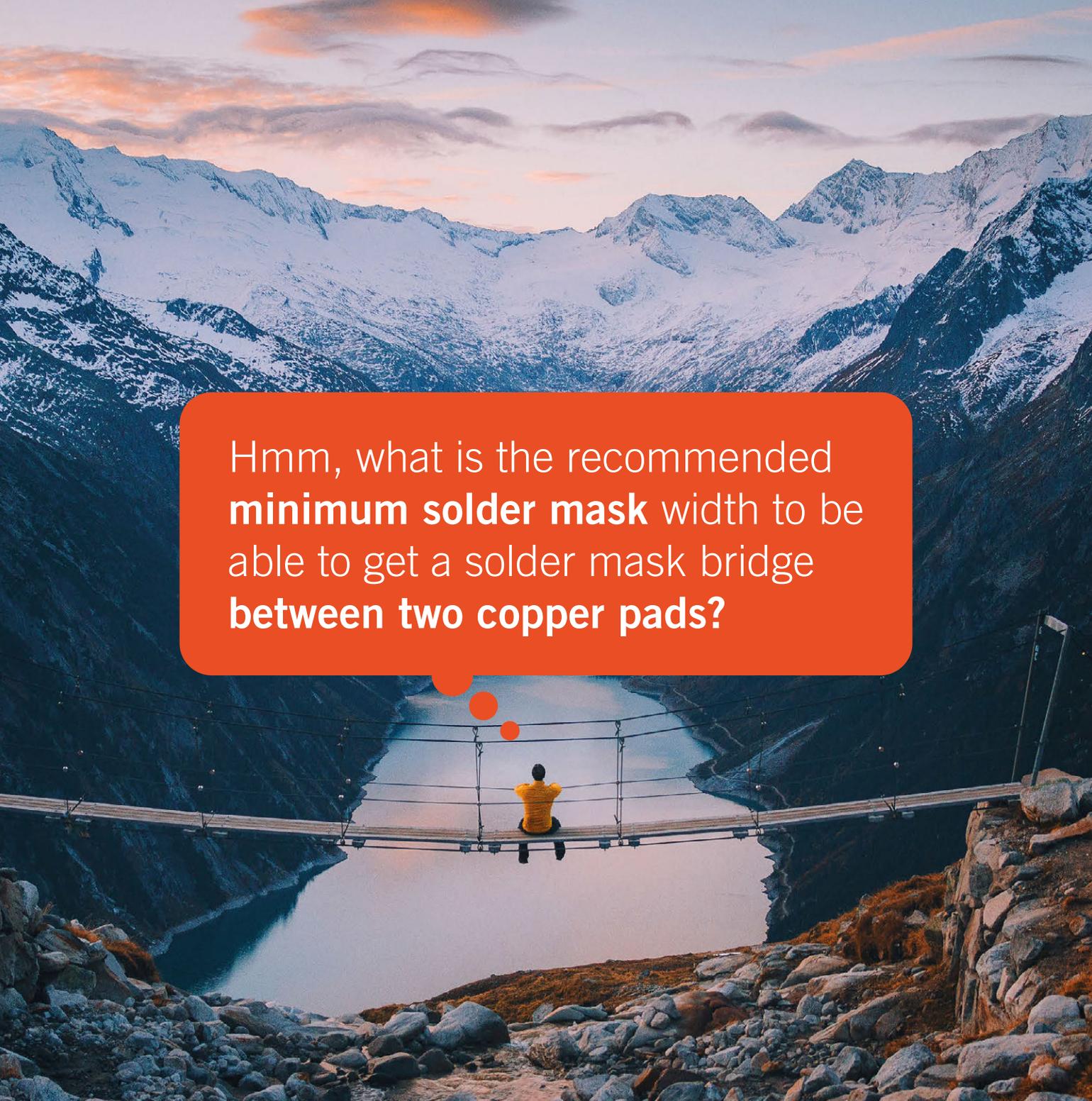
- Fabricators previously only able to offer 3 mil trace/space, can now reliably produce 1 mil trace/space and below.
- Further reductions required the adoption of various mSAP manufacturing processes.
- SAP enables the printed circuit board fabricator to employ an additive screen process instead of an edge-removal, etched process.
- SAP provides tighter line width control and straight conductor sidewalls greatly improving impedance control.
- SAP provides tighter impedance tolerance than the traditional subtractive etch processes.
- The SAP process promises greater routing density with six 1/1 mil trace/space between lands.
- Unintentional coupling of parallel segments is extremely strong between 1 mil spaced traces.
- An extremely thin dielectric of 1 mil or less is required to maintain 50 ohms impedance with a 1 mil trace.
- Breakout vias are still required with SAP—although via-in-pad dramatically reduces the real estate required. **DESIGN007**

Resources

1. [Beyond Design: “Controlling the Beast”](#) by Barry Olney
2. “SAP and mSAP in Flexible Circuit Fabrication” by Tara Dunn
3. “Achieving Fine Lines and Spaces Using mSAP” by Rich Bellemare and Jordan Kologe
4. “mSAP: The New PCB Manufacturing Imperative for 5G Smartphones” by Many Gantz
5. Nano Dimension, Dragonfly product datasheet



Barry Olney is managing director of In-Circuit Design Pty Ltd (iCD), Australia, a PCB design service bureau that specializes in board-level simulation. The company developed the iCD Design Integrity software incorporating the iCD Stackup, PDN, and CPW Planner. The software can be downloaded at www.icd.com.au. To read past columns or contact Olney, [click here](#).

A person in a yellow shirt is sitting on a suspension bridge that spans across a deep valley. The bridge is made of wooden planks and is supported by cables. Below the bridge is a calm lake that reflects the surrounding mountains. The mountains are covered in snow and are very high. The sky is a mix of blue and orange, suggesting a sunset or sunrise. The overall scene is peaceful and scenic.

Hmm, what is the recommended **minimum solder mask** width to be able to get a solder mask bridge **between two copper pads**?

PCBs are complex products which demand a significant amount of time, knowledge and effort to become reliable. As it should be, because they are used in products that we all rely on in our daily life. And we expect them to work. But how do they become reliable? And what determines reliability? Is it the copper thickness, or the IPC Class that decides?

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The Digital Transformation of Advanced Additive Electronics

Digital Transformation

Feature Column by David Wiens, SIEMENS EDA

Previously in this column, we've explored the digital transformation of different aspects of the traditional electronic systems design process. This time I'll look at emerging technologies for additive manufacturing, but with the same goal: an optimized digital thread through design, verification, and manufacturing.

Additive manufacturing has been around electronics since thick-film screened hybrids came on the scene more than 30 years ago. And while those never quite went away, they never gained the prominence we all expected alongside the more traditional laminated, subtractive-etched PCBs. Today, emerging technologies are bringing a resurgence in additive manufacturing, thanks to a host of new materials, machines, and processes.

Electronics have historically been discrete structures encapsulated in some mechanical package. The drive now is to integrate electronics more seamlessly into the end-product's form factor, requiring circuits that are flexible and/or conformal to the contours of any product surface. In addition to reduced size and weight, other drivers include customization with localized

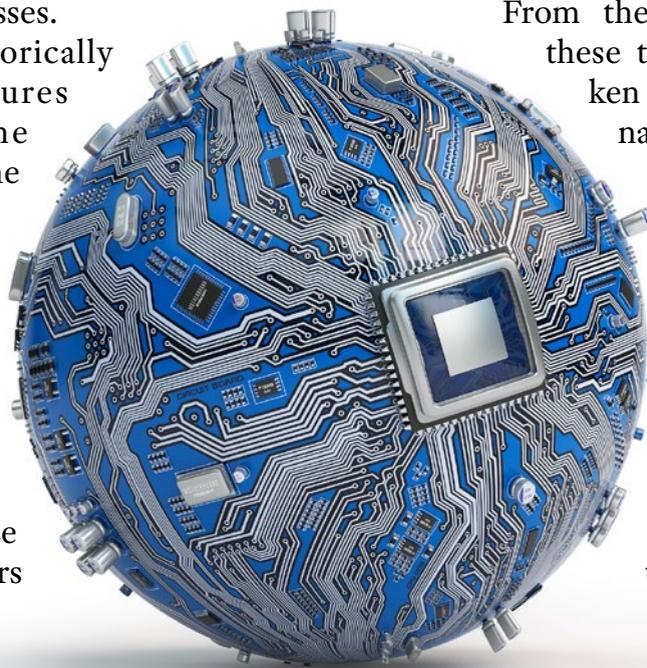
manufacturing, reduction in part count, new 3D structures, and a reimagined supply chain.

There are several applications for this new technology, including radar systems and other sensors molded to the surface of an airplane, smart textiles with integrated sensors to measure human performance and provide identification, and medical bandages that sense infection and accelerate healing. Cars are rife with sensors across both the exterior and interior surfaces, conforming to the design of the car, not the other way around. Even product packaging includes sensors that track conditions during shipment to ensure quality.

Design for Additive Manufacturing

From the designer's perspective, these technologies can be broken into planar and non-planar categories.

Planar electronics are designed with processes like those used for traditional, flat PCB-like layered structures. The manufacturing may be very different (e.g., using an additive printer), but it's still creating the structure one planar layer at a time. Post-production, they can





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TUC's PegaClad 1 and 2 are designed for high frequency, very / super low loss applications, including mmWave printed circuit board designs. Their electrical properties are equivalent to PTFE laminates, yet they perform in multilayer circuit boards requiring excellent thermal reliability in harsh environments.

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be flexed or molded into the final form. Advanced technologies that fit the planar design model today include flexible hybrid electronics (everything's flexible, including the ICs and batteries), molded interconnects, and 3D conformal "wraps" (e.g., 2D designs converted to fit a 3D structure, then printed).

PCB design tool advances made over the years to support rigid-flex, localized dielectrics, HDI, wire bonding, and embedded actives/passives can aid in the design of planar structures (i.e., make the digital twin more intelligent, rather than creating workarounds that must be explained or converted for manufacturing). Certainly, design for manufacturability takes on new meaning when you must ensure things like interconnect and impedance continuity in the final flexed/conformal structure. In this design chain, MCAD tools become more critical, but there's still the physical separation between electronics and associated mechanical enclosures or mounts.

Non-planar electronics can have interconnects and components placed at any angle, in any location in a given space. There's no functional reason to separate electronics from a mechanical enclosure. They're one and the same—the ultimate in electro-mechanical structures. Given the geometrical challenges, current prototypes of these structures are often designed in MCAD as non-electrically intelligent structures, forgoing much of the automation and verification technologies built up over decades in ECAD. These structures are still relatively simple, so the trade-off is acceptable, but as complexity increases, the need to maintain electrical intelligence and model performance will increase.

Optimizing the Tool Chain

Over the last 50-plus years of PCB design and manufacturing, the tool chain from design through manufacturing has become fairly optimized (there are still areas for improvement).

As noted in the introduction, the goal for additive manufacturing is to achieve the same optimizations, ensuring a continuous digital thread so that there is absolutely no redesign as the design passes through various design and verification tools and on through to manufacturing (Figure 1). Part of the challenge today is that there are so many manufacturing technologies and materials in research that it's hard to focus on optimizing a moving target.

At first glance, the process chart in Figure 1 could easily represent traditional PCB flows, but a closer look reveals many new challenges:

- The delineation between ECAD and MCAD is blurring so much that electro-mechanical design may have to be done in one tool.
- Design constraints will have to consider the variability of the materials used.
- Given the operating conditions of these new structures, a host of multi-physics analysis will be required to ensure performance (e.g., signal, power, thermal, EMI, stress, vibration, stretch, moisture, impact, deformation, and manufacturability).
- The product model transferred to manufacturing will need to maintain design intent to eliminate redesign. Planar electronics could leverage existing PCB models (e.g., ODB++, IPC-2581), but today many of the tools in additive manufacturing don't accept them. Non-planar electronics will likely require a completely new model. In both cases, the path from design may flow through MCAD, rather than the traditional ECAD outputs.
- In manufacturing, the process preparation stage must apply to multi-material "slicing" and "tool-pathing" algorithms to ensure that the structure is printed as designed.

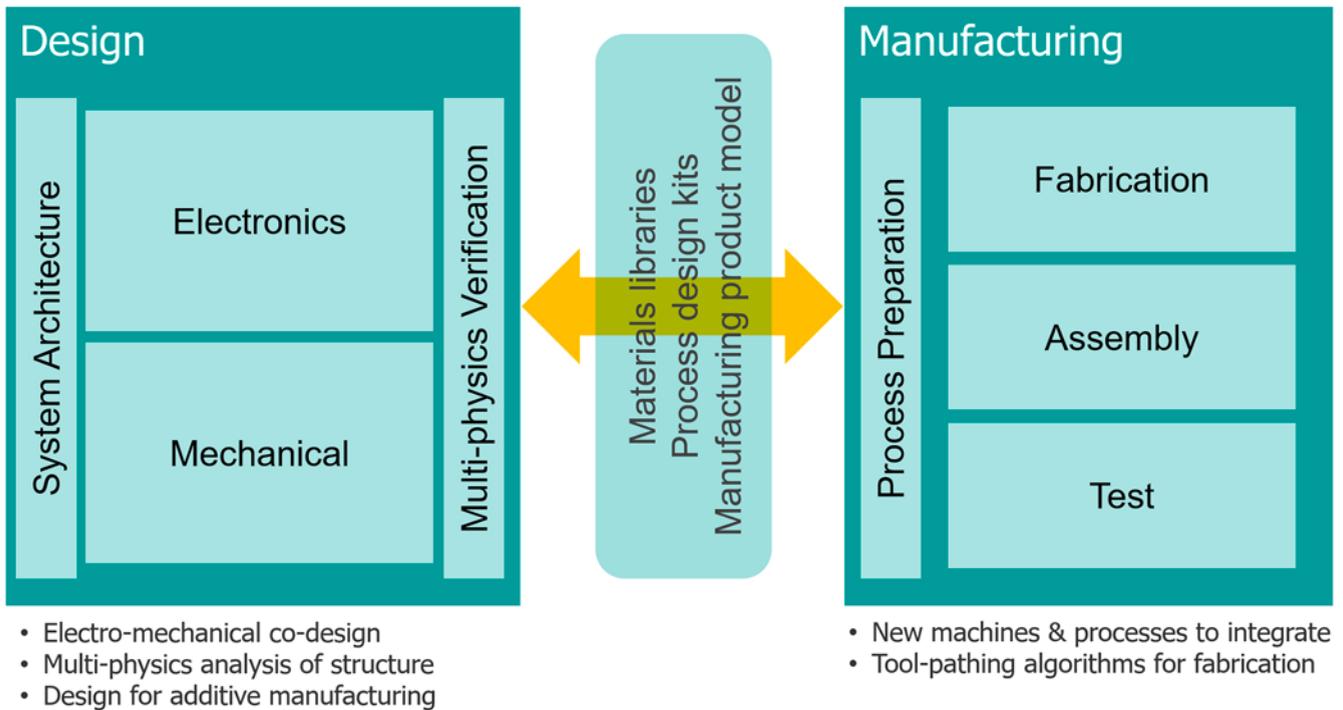


Figure 1: Tool chain for 3D-printed electro-mechanical structures.

- In manufacturing, a host of new machines must be integrated (e.g., 6-axis robotic printers, reel-to-reel processing, and assembly of bare, flexible dies). In addition, the traditional PCB fabricate-then-assemble process could be upended, with the ability to integrate active and passive components during the “substrate build.”

The net results currently are multiple tool chains in various states of optimization. To address these challenges, Siemens is leveraging its multi-domain portfolio of ECAD, MCAD, and simulation technologies. We are partnering with NextFlex and its members to refine the tool chains and then work to optimize the digital thread from concept through manufacturing. **DESIGN007**



David Wiens is Xpedition product manager for Siemens Digital Industries Software. To read past columns or contact Wiens, [click here](#).

Additional content from Siemens Digital Industries Software:

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- *RealTime With... Siemens and Computrol: Achieving Operational Excellence in Electronics Manufacturing Roundtable*

Using **Touchstone Files** to Build Measurement Confidence

The Pulse

by Martyn Gaudion, POLAR INSTRUMENTS

Measuring PCB insertion loss can be time consuming (when compared with impedance testing), and the probes and cables tend to be significantly more costly (and delicate) than those used for characteristic impedance measurement. Nonetheless, given the high capital investment required for test systems, cables, and probes—and the design of the test vehicles themselves—wouldn't it be nice if you could have a way of looking at your expected results before you put a test probe to a PCB?

I am not talking about simply simulating the result, rather recreating the raw files that can be used to drive the insertion loss test software and feeding the test software with data “as if” it was idealised measurement data.

Wouldn't it be handy if you could prepare simulated raw files “as if” from a VNA to feed

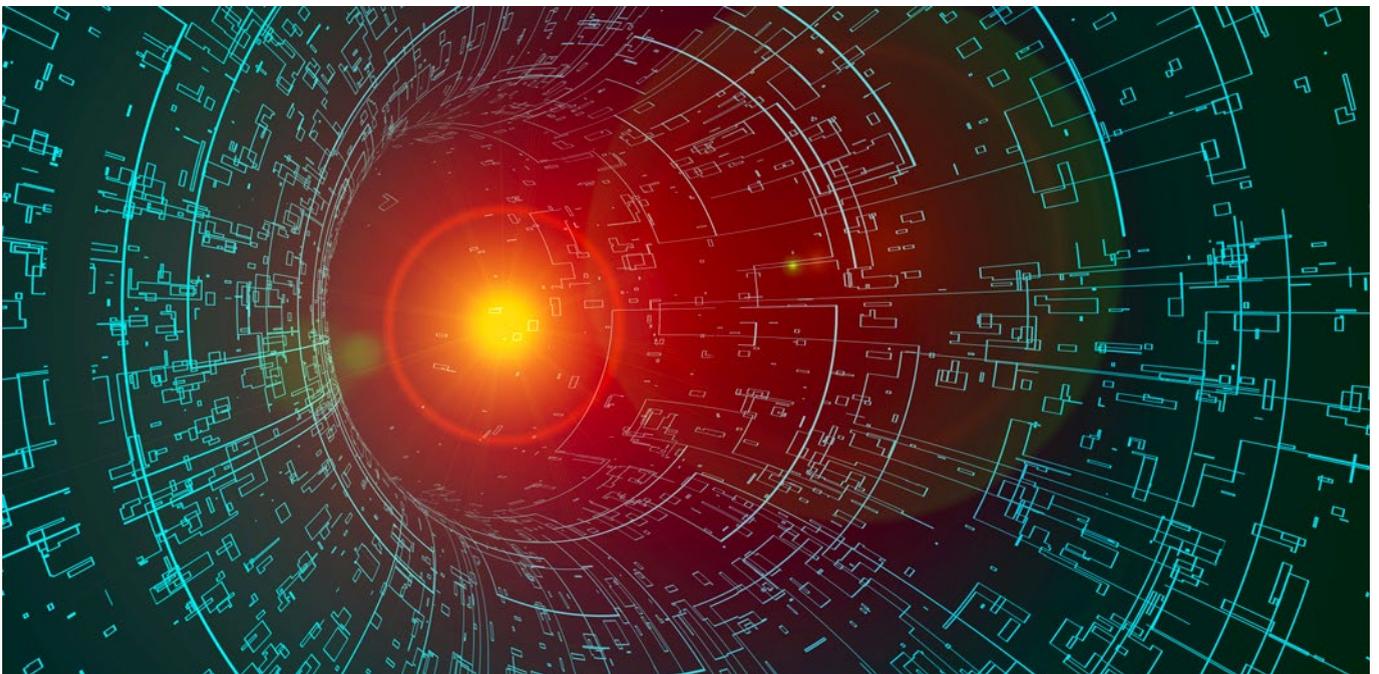
into your de-embedding software to ensure that it processes and the results from the test software are what you expect?

If you have followed this column for some time, you will recall the advice on measurement I have shared before, courtesy of Eric Bogatin:

“To make a good RF measurement, you need some engineering intuition to get a gut feel for what the measurement should be, and you also should model the expected results with a field solver before making the measurement itself.”

My column proposes an extra step made possible using Touchstone files.

Touchstone files are an industry standard ASCII file used across the EDA community for the recording and sharing of network parameter data, such as s-parameters (and more).



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They are the common output of vector network analysers, and of simulation tools. Originated by EEs in 1984, the file format has lived through a variety of owners and is now under the umbrella of Keysight Technologies. The files themselves have become a de-facto industry standard with their simplicity and lack of variation leading to very widespread usage.

Most fabricators are familiar with impedance measurement and can possibly make impedance measurements with their hands behind their back and their eyes closed. For insertion loss measurements, the list of who can do that is arguably much smaller. One of the reasons is the process of modeling and measurement is inherently more complex, even with attendant software to help, so a non-SI specialist in the fab industry needs all the confidence tools available to have trust in a measurement.

Let's look at the process difference from modeled to measured. First for impedance:

1. Model expected Z_0 result by entering trace geometry and base material characteristics with a field solver.
2. Create suitable test vehicle, typically a four- to six-inch coupon with via connection at each end. The via characteristics are not super critical.
3. Test the coupon trace with a suitable TDR or impedance test system.
4. Compare 1 with 3. Provided you made what you thought you made, you will have a reasonable chance of good correlation.

Now to the process for insertion loss. The principle is the same but because of the much higher (and lower) frequency content there are some extra steps which can lead to disappointment if you don't plan.

1. Model the expected insertion loss by entering trace geometry, coupon length, and add in loss tangent and appropriate surface roughness to the characteristics.
2. Create a suitable test vehicle, typically a pair of differential traces with identical

cross-section but one pair shorter than the other; five-inch and 10-inch traces are not uncommon. Most ultra-high-speed architectures are differential, so a pair of differential traces is required. The vias and landing pads need to be specifically designed to an OEM specification or to the advice of the probe manufacturer you choose. Via design is much more critical than with impedance.

3. Measure the s-parameters of the two traces over the desired frequency band.
4. Post process the s-parameter pair data. Most methods require the test data to be processed by mathematically removing any residual via effects by looking at the difference between the long and short line. This is a complex process: One algorithm for this is Delta-L 4.0, but many other methods exist.
5. The post processing software will give you the dB loss per unit length of the trace under test which you can compare with my first point.

What Could Go Wrong?

Quite a lot actually. The VNA operator needs to ensure that the VNA is calibrated to the particular cable setup (and possibly the probe as well). Though Delta-L 4.0 does a pretty good job of removing probe effects, there is still a multi-step process to initially calibrate the VNA before measurement starts with a given setup. The probes deployed are precision RF measurement probes, and either need placing with a probe station, or need to have the coupon design tooled with location holes to ensure the operator is not at risk of misaligning. Also, the differential probes need to be connected to both ends of the short line and gather one set of s-parameters and both ends of the long line. Contrast this with a differential impedance measurement which requires a precalibrated TDR and one differential probe. There are far fewer steps.

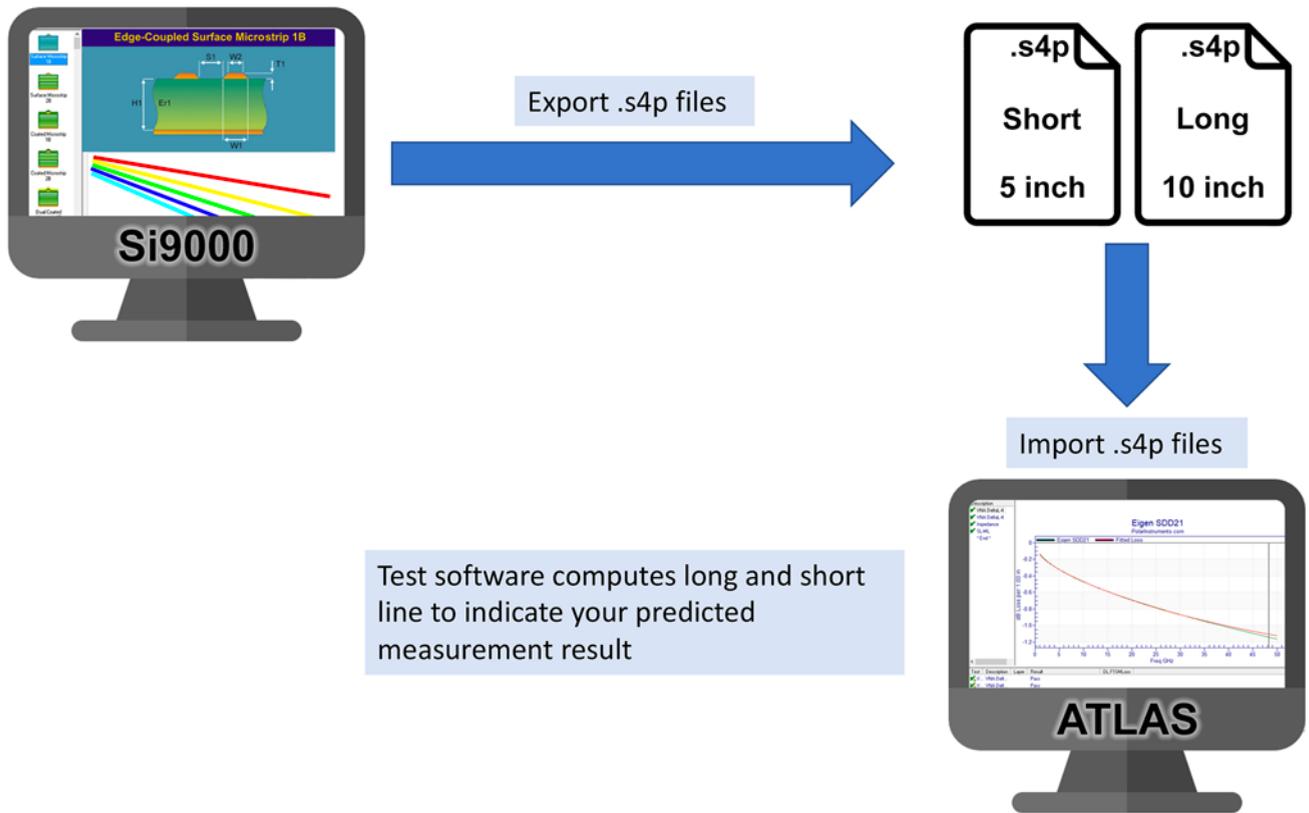


Figure 1: Injecting ideal data into measurement system for pre-validation.

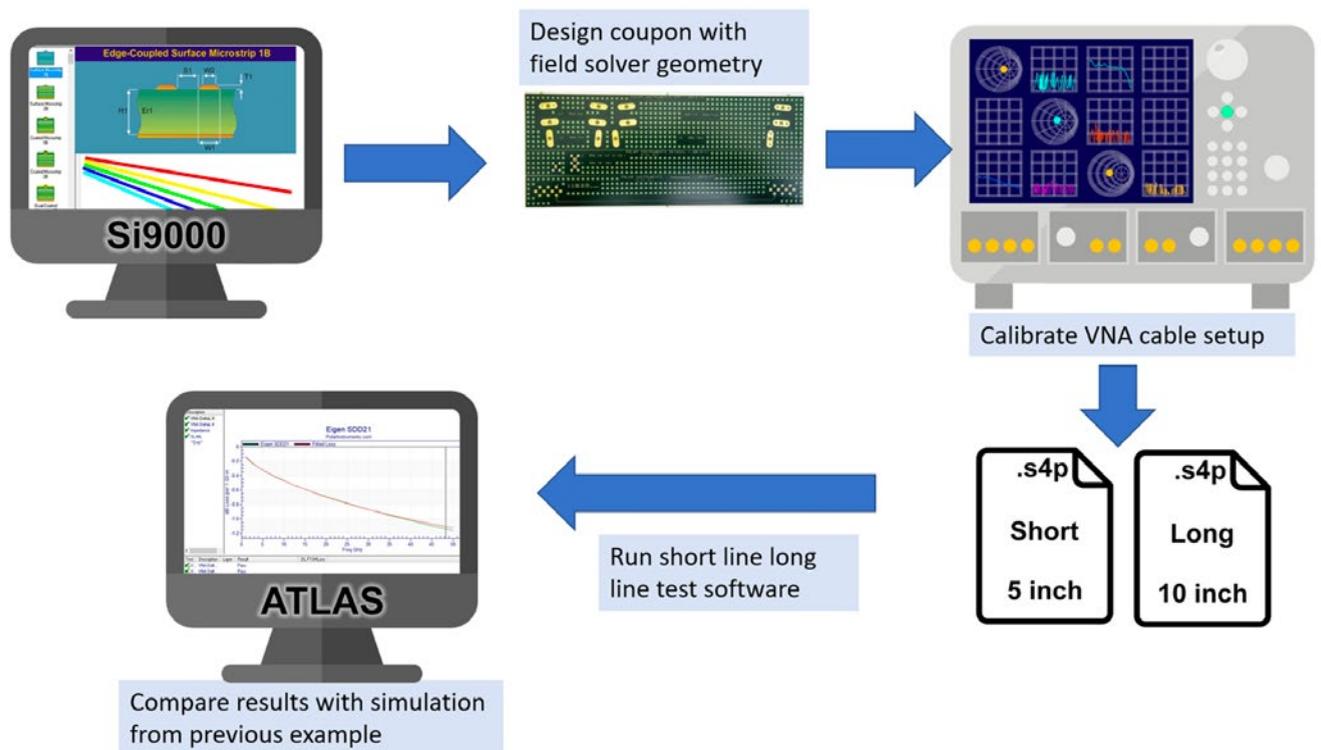


Figure 2: Measuring with increased confidence after system validation.

I often get asked why a measurement isn't as expected; without being physically present, even via a weblink, that's a tough call. What can be done to rule out as many things as possible and build confidence in the complete system? Interestingly, as soon as the user is confident that the system is okay then good measurements become simpler to achieve.

I often get asked why a measurement isn't as expected; without being physically present, even via a weblink, that's a tough call.

This is where the Touchstone files come in handy. Simply by exporting a pair of 4 port .s4p Touchstone files for the coupon under test from the modeling software, these two files can be fed to the long line/short line post-processing software. With Polar Atlas you can set the input to the Delta-L to be Touchstone rather than the VNA. This simple step allows you to send idealised results for the two coupons direct into the test software. Post-process the results and verify that with "ideal" data the long line/short line post processing works as expected. Once that is proven, the operator can go back, recalibrate the VNA cable setup, and make the measurement again with increased confidence of a quality result.

What kind of situations can this help with? A first time or inexperienced VNA user can be faced with a variety of unfamiliar situations during insertion loss measurement: The VNA needs to be correctly warmed up and stabilised, a calibration procedure needs

to be run once the cables are connected with the appropriate artefacts, and care must be taken for all the ports to be connected in the correct order to the correct artefact. With practice, "muscle memory" makes this process easy but first-time users need to take care, and it's best to do this in a quiet situation without interruption.

Connectors all need to be torqued to the specified level, and whilst this is recommended on TDR measurements, in practice you can get away with manual connections on a TDR. With a VNA, the need to torque connectors is far more critical. Simple errors, like connecting the VNA probes to the short line when you should be probing the long line, are easy to fall into. The ability to dry run the measurement with accurate simulated s-parameters removes a level of doubt and raises an operator's confidence that good measurements are possible and, indeed, with practice are repeatable and normal.

In conclusion, the ability to insert trusted s-parameter transmission line data directly into the insertion loss processing software in place of raw measurement data raises operator trust in the system when using with "real" data from a VNA. **DESIGN007**

Additional related content:

- [The Printed Circuit Designer's Guide to... Secrets of High-Speed PCBs, Part 1](#) by Martyn Gaudion
- [The Printed Circuit Designer's Guide to... Secrets of High-Speed PCBs, Part 2](#) by Martyn Gaudion



Martyn Gaudion is managing director of Polar Instruments Ltd. To read past columns or contact Gaudion, [click here](#).

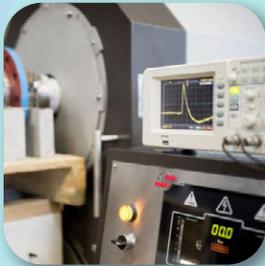


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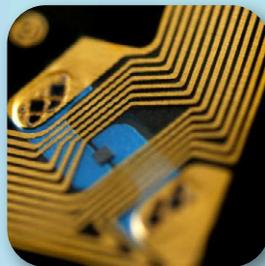
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Calumet on Additive and Semi-Additive Design



Feature Interview by the I-Connect007 Editorial Team

Editor's note: The following is an excerpt from our interview with Calumet's Todd Brassard and Meredith LaBeau originally published in the February issue of PCB007 Magazine.

Calumet Electronics has been a domestic pioneer in manufacturing with additive and semi-additive electronics manufacturing processes. We recently asked Calumet's Todd Brassard and Meredith LaBeau to discuss the state of this technology, which traditional processes that they might replace, and some of the challenges facing OEMs or PCB shops that are considering these options.

Meredith LaBeau: Because semi-additive and additive technologies are relatively new fields in the United States, young engineers have

an opportunity to get in on the ground floor so to speak. This is an inroad for young engineers.

With respect to a new market of products enabled by semi-additive processes, we are seeing that U.S. designers lack experience designing at the smaller scales. Designers who are exploring additive manufacturing are doing so on their most complex designs, which makes sense, but it means the additive technology is being piled on top of an already messy build. It will take some time before board designers take full advantage of ground-up additive design.

What I'm really seeing with the semi-additive process is that designers don't know how to design for it. They can't take their heads out of what they originally did and say, "I'm going



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Meredith LaBeau

to use this additive technology to reduce or reset the technology curve.” Rather, they think, “I’m going to throw it into my kitchen sink of soup, and I’m going to add it all at once.” That has been a hard adoption.

Barry Matties: What is the tipping point for a designer to start looking at additive technology?

LaBeau: One example would be placing a component with particularly dense I/O or having to add layers to accommodate fan-out. A designer can route many more 20-micron traces than 75-micron traces inside of a BGA. The ability to redesign PCBs to take advantage of additive manufacturing will depend on where a design is within the OEM’s lifecycle, although component shortages may force redesigns. When it comes to new engineering or manufacturing technologies, for example direct dispense solder mask, the PCB industry is pretty risk averse. To get PCB shops to accept new manufacturing methods, the product had better not come out looking much different. Conversely, taking a little risk may just lead to a PCB shop

developing manufacturing capabilities that support next generation electronics.

Matties: It’s better to be in the front than in the rear. The first fax machine didn’t make all the money. It was the second one.

Todd Brassard: Again, the fracturing of the manufacturing pipeline represents a significant barrier to innovation. One way we believe we can break down these barriers is with the multi-party NDA, allowing OEMs to have direct conversations with supply chain CTOs and high-level engineers with the goal of developing novel solutions. You want 2,500 or 5,000 I/O on a substrate the size of your thumbnail? You will need the materials, chemistry, lithography, and equipment suppliers and distributors’ CTOs in the room with the OEM. I’m thinking about this as a “micro industrial commons.” If the team can make it work, all companies have something novel to sell to their customers.

Matties: What do you think the most important message we should be communicating to the industry regarding additive and semi-additive should be?

LaBeau: I think people need to be aware of what additive technology is, and that they understand how to get their shop to utilize it. Maybe they’re not ready for it yet. What are the opportunities, and where can they start to dabble with additive technology?

It seems that if we can prepare the material correctly, we can apply copper to anything. If a company can have foresight of what the future can bring and start to think about their design for manufacturing and engineering, and how they take the next step to utilize an additive technology, or even use thinner foils, that’s a first step into mSAP. Just use some thinner foils, and start to baseline your Cpk’s, and how you can keep going further.

No one can flip that coin that easily unless their capital expenditure budgets allow for

rapid expansion. We're still working at the numbers, but we believe it's somewhere in the realm of a couple million for a small shop that's already in business, just to add a couple of specialty materials, specialty imagers.

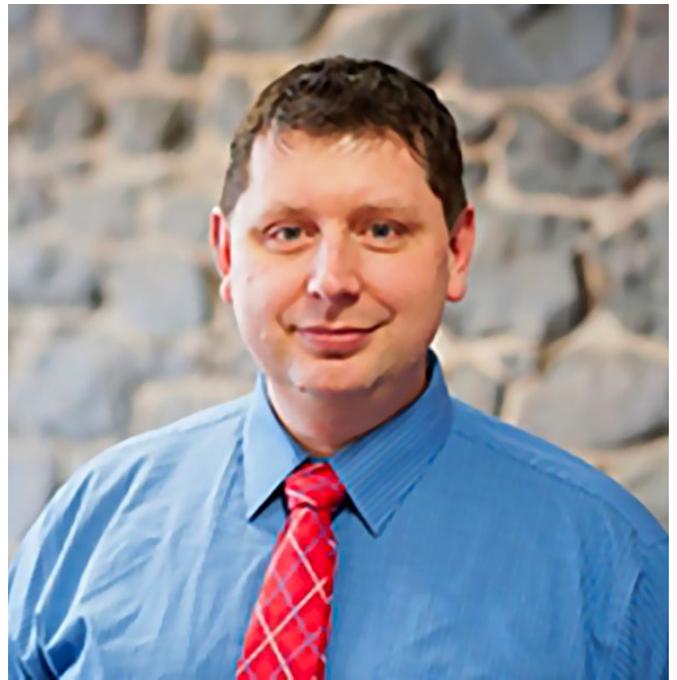
You're just going to need low-stress chemistries, is really what it comes down to, and some different prepping chemistries, and different etching chemistries because of adhesion. But the other thing I would suggest is that additive technology is not that far away from what you're already doing. It is not this complete change; well, it is, because we're adding instead of subtracting. But you're still using a lot of your same traditional pathways to bring the technology to bear.

Nolan Johnson: Can you foresee the additive process being as economical as subtractive in the future? Is it as economical already?

Brassard: Maybe it's not about additive being as economical as subtractive, but rather what new opportunities are opened to migrate a shop toward a more profitable business. Sure, there are cost tradeoffs between subtractive and additive manufacturing. There is the capital cost of upgrading a factory, consumption of specialized chemistries, and direct materials; it really depends on how the additive technology is applied in product realization.

For instance, a designer may take an existing design that needs to drop from 75- to 55-micron traces to achieve the desired fanout for a high-density I/O chip. Converting a couple of layers from subtractive to additive processes will allow this, but it's going to be a pure cost adder because nothing else about the design changed to take advantage of the economy of scale that additive can achieve.

On the other hand, taking full advantage of the small scales of copper traces and features that additive can achieve, designers can meaningfully reduce cost by reducing board size, eliminating layers, and running fewer lamination cycles. If a standard 18" x 24" panel origi-



Todd Brassard

nally fit six parts, the new smaller board may fit 80 parts. Dividing the panel cost by 80 rather than six results in per part cost savings.

This scenario adds cost for additive, but removes cost by reducing size, layers, and cycles, and the panel is cut up into a greater quantity of parts—like how components have been miniaturized to reset profit margins by getting more parts out of the same materials. The result is cost savings and a reduced form factor that may benefit the final system in which the final PCBA is placed.

Johnson: Same question, but on your operating costs for an additive line. Can you see that reaching parity with subtractive in the future at some point?

Brassard: As Meredith indicated earlier, we do not have a separate factory where we're doing additive manufacturing. Ninety percent of the processing that we do for an additive board is identical to what we do for a subtractive board. In some cases, we will realize the traces by etching and in other cases we'll grow the traces.

LaBeau: You're going to have some capitalization costs, but I don't think your operating costs will change that much by the time you get it into a production environment.

Brassard: There are challenges to overcome in learning additive manufacturing. Like anything new, it's about many iterations, and learning from each failure and success. Many iterations and working with amazing engineering teams at OEM and supply chain partners. Being a few years into the process, Calumet Electronics has gained the know-how. Next, it's scaling capacity to start meeting some of the needs of the domestic market.

Calumet is exactly the type of small business that the DoD wants to be strong and thriving in the defense and commercial markets. The DoD would like to see many PCB shops with high technology manufacturing capabilities to provide redundancy, reduce risk, and reduce cost through competition. But I'll say it again: The U.S. government and DoD need to help jump start the U.S. electronics manufacturing industry—not just the chips, but the entire ecosystem.

Matties: Some of the partnerships with the OEMs come in, and they fund a lot of this. Are you seeing that co-op?

LaBeau: Not at the level we would like to see just yet.

Brassard: Nothing gets the attention of OEMs like supply chain shortages or disruptions. As demand continues to increase for complex technologies to be produced in the U.S., the urgent need may drive more and better funding opportunities.

Matties: I've seen in the past where they have funded equipment.

LaBeau: They can, but often a shop can only use the equipment on the OEM's work. This is not especially helpful in building a strong shop. Perhaps it's more effective at a larger scale.

Matties: Thank you both for your time. This has been great.

Brassard: Thank you. Always a pleasure. **DESIGN007**

Boeing, AWS Join Forces to Transform Aerospace Design and Manufacturing

Amazon Web Services and Boeing announced an expanded relationship that extends the aerospace leader's existing cloud operations and streamlines Boeing's approach to cloud computing. Boeing will migrate applications out of on-premises data centers to AWS and create a technology foundation that will strengthen engineering and manufacturing processes. Beyond the cloud relationship, Amazon Air has grown its fleet to more than 110 Boeing aircraft to facilitate the movement of goods to Amazon customers worldwide.

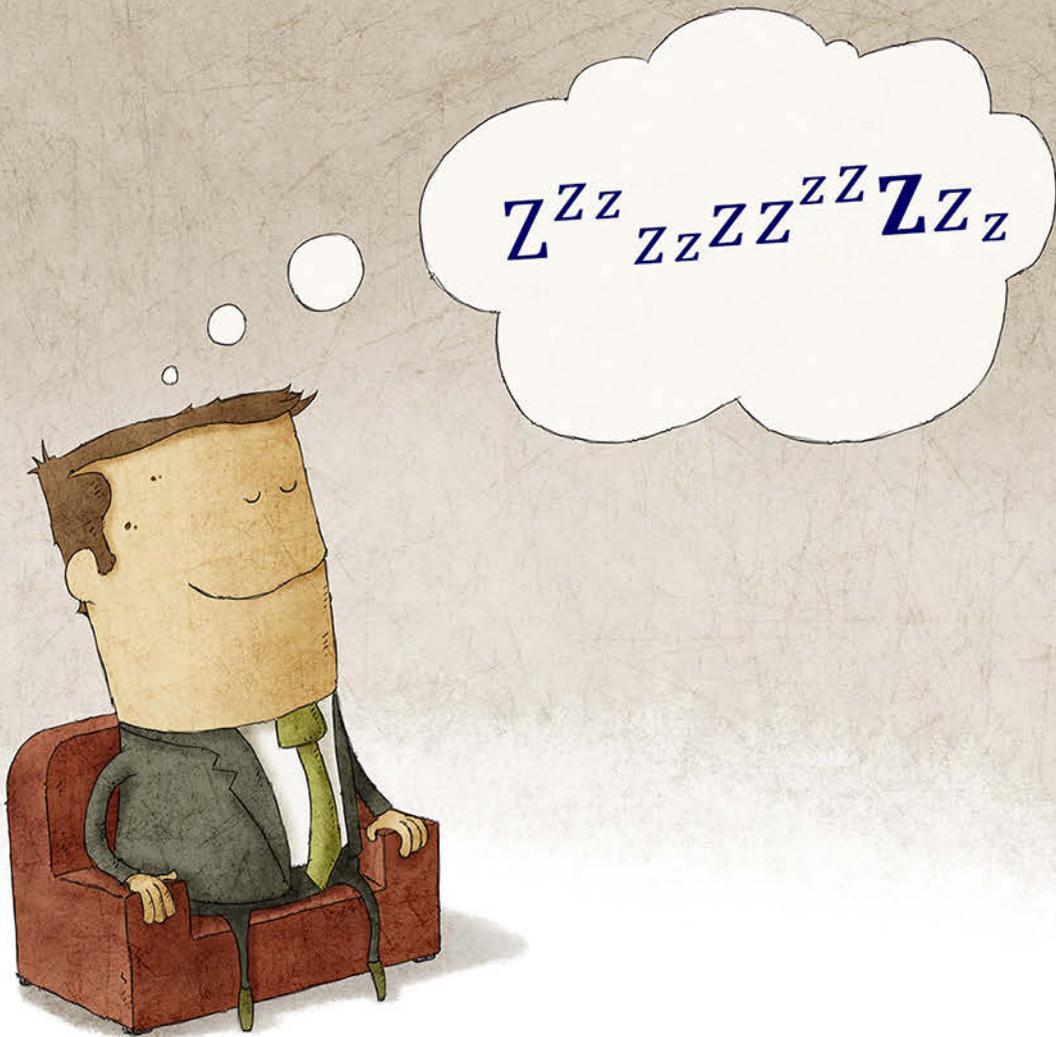
Boeing is a leading global manufacturer of airplanes and space systems, with aerospace engineering at the heart of its operations for more than 100 years. This collaboration with AWS expands the company's current cloud operations and allows

Boeing to take advantage of AWS's scalable, power-efficient, and high-performing infrastructure, as well as its industry-leading cloud services, including high performance computing (HPC).

"Boeing and AWS share a builder culture and are committed to using advanced technologies to take on the most ambitious engineering feats like developing new sustainable energy sources and interplanetary human travel. Together, we will deliver more powerful, sustainable, and efficient aerospace design, engineering, and management solutions that will help Boeing customers today and in future aerospace travel," said Matt Garman, Senior Vice President of Sales and Marketing at Amazon Web Services.

(Source: Business Wire)

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The Importance of Circuit Features for Millimeter-Wave Applications

Lightning Speed Laminates

by John Coonrod, ROGERS CORPORATION

Over the past several years there has been a steady increase in millimeter-wave (mmWave) applications. This was probably sparked by the chip industry, which has the capability to produce chips in large volume that have good mmWave performance. As the mmWave applications increased, most aspects of the electronics industry, including the PCB industry, were forced into a steep learning curve. As a general statement, the quality of the circuit board is more critical to mmWave applications as compared to lower frequency applications. To be more specific, the quality concerns are mostly related to consistency of circuit features such as conductor widths, conductor shapes, conductor spacing, substrate thickness, copper thickness, and final plated finishes.

Millimeter-wave applications are more sensitive to circuit features, due to wavelength. Wavelength is the physical length of a propagating wave and, as an example, the physical length of a wave at 3.3 GHz is about 2.3 inches. That is assuming a microstrip built on a thin laminate with a Dk of approximately 3.0. Within that 2.3 inches, the wave is made up of 360 degrees, which is also referred to as phase angles. If the propagating wave encounters an anomaly which is 0.023" in size, this is the same thing as 1% of the wavelength or about 3.6 degrees. This small anomaly, in relation to the wavelength, will have very little effect on the propagating wave. However, at a mmWave frequency, such as 77 GHz, the physical length of the wave is about 0.095" and if the same





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0.023"-sized anomaly is part of the propagating wave path, it is now equivalent to 24% of the wavelength or about 87 degrees of the wave. Having a 24% portion of the wave affected by an anomaly may have an impact on the propagating wave and cause distortion and other unwanted wave properties.

Having a 24% portion of the wave affected by an anomaly may have an impact on the propagating wave and cause distortion and other unwanted wave properties.

Additionally, at mmWave frequencies, the high frequency material used in the PCB construction is typically thin. A thin laminate will translate to a narrower conductor to maintain a certain impedance. A typical conductor etching tolerance of ± 0.5 mil is usually acceptable for most lower frequency applications, but with mmWave applications this tolerance may not be tight enough to give good RF results. The reason is a narrower conductor with a total variation of 1 mil will have more impedance shift, as compared to a wider conductor. Some impedance matching networks in the antenna array areas of the auto radar sensor have conductors as small as 5 mils in width. A difference of 5 to 6 mils on a thin substrate can be a difference of 6 ohms impedance. However, when using a thicker substrate for lower frequencies and the appropriate wider conductor to maintain a given impedance, a 1 mil difference in conductor width will make an impedance difference of less than 1 ohm. There are many items in circuit fabrication which can alter the impedance of a circuit and having very good etching control is a major advantage for a PCB

fabricator working with mmWave applications.

There are several different RF structures used in mmWave applications, and the structure that is normally least affected in RF performance by the normal variations in circuit fabrication processes is microstrip. The microstrip construction is typically the top two conductor layers on a multilayer RF board and has a signal conductor on top and a ground plane below. Another structure often used in mmWave circuitry is grounded coplanar waveguide (GCPW). This structure is also a two-copper layered circuit; however, the top signal plane has three conductors electrically oriented as ground/signal/ground. This configuration is very good to minimize certain unwanted wave characteristics at mmWave frequencies, however this structure may be impacted more by normal variations of circuit fabrication.

The space between the ground/signal/ground in the GCPW is critical and if that space varies much, so will the RF performance of the circuit. However, it is more complicated than that. On the top signal plane, there are strong electric fields between the neighboring ground planes which are on both sides of the signal conductor. In a cross-sectional view, if the side-walls of these conductors are straight, there will be more fields in air. However, if the conductors are trapezoidal shaped, there will be fewer fields in air and more fields in the substrate. The difference of these fields being in air impacts the effective Dk the propagating wave experiences. Air has a Dk of about 1 and when the fields use more air, the wave will experience a lower effective Dk, and that can impact multiple RF circuit properties. That is especially true at mmWave frequencies. To have more consistent RF performance when using a GCPW at mmWave frequencies, controlling the conductor width and spacing is important, but having a consistent conductor shape is also very important.

There are many things to consider in the circuit fabrication process for achieving a consistent conductor width, space, and shape. The image and etching process using an additive

process is often better than a subtractive process for conductor shape consistency. However, even with the additive process, there can be concerns for trapezoidal shaped conductors. It is usually a flipped trapezoidal shape as compared to the same concern when using the subtractive process.

Another item which can assist in consistent conductor shape and etching control is using thinner copper. Thinner copper will naturally give less trapezoidal shape and controlling the etching of the conductor width and space is easier. Rogers Corporation has several high frequency circuit materials which are used in mmWave applications with a laminate available with one-quarter ounce (9 μm) copper. Using this laminate with very thin copper can be beneficial for the PCB fabricator to have more consistent conductor shape, width, and spacing.

Millimeter-wave applications are more sensitive to circuit feature variability, as well as small circuit anomalies, which may have been acceptable for lower frequency applications. The PCB fabricator is challenged to control conductor widths and spacing to a tighter requirement and the shape of the signal conductor also needs to be more consistent. Additive processing at the PCB fabricator can be beneficial for these mmWave circuit requirements and using a laminate with thin copper can also be advantageous. **DESIGN007**



John Coonrod is technical marketing manager at Rogers Corporation. To read past columns or contact Coonrod, [click here](#).

Happy's Tech Talk

Semi-Additive Processes and Heterogeneous Integration



by **Happy Holden**

The semi-additive processes (SAP) are not new. I first used them with a novel process back in 1978. MacDermid had a novel SAP process called PLADD II (plated additive). It was an anodized aluminum foil applied to laminates that we could easily etch off after drilling and continue with a special electroless copper for thin metallization.

In his Tech Talk column, Karl Dietz wrote about SAP many times from 2000 to 2010.¹⁻⁵ In a 2010 column, Karl included a table to show the relationship between copper thickness, resist thickness, and resolution capabilities of processes.⁵ Karl devoted many Tech Talks to “fine-line imaging” and to related topics such as photoresist adhesion, developing, fine-line etching, stripping, and pattern plating.

Semi-Additive Processes

The older mSAP processes used thinned copper, usually to nine or five microns, from half-ounce foil or very thin copper foil (usually with a peelable

protection). They would usually have a flash copper strike and may use tin plating as the etch resist.

The IC substrates (for flip-chips) were always the leading edge of this technology, from 2005 onward, but quickly converted to the use of the Ajinomoto build-up film (ABF) from Japan that was additive electroless on the bare-etched, vacuum laminated dielectric films.

The advanced-modified SAP (amSAP) processes did away with the copper strike and further exploited the thin-copper foils.

Averatek's new A-SAP™ (or pure additive) starts with a treated copper foil on the laminate, but after drilling, the copper foil is etched away. This allows a new generation of nanoparticle Liquid-Metal Ink™ catalysts to be used to prepare the surface for fine-grain electroless copper application. After pattern electroplating and resist stripping, this electroless copper, being only around 0.7 to 1.2 microns thick, permits a flash etch without any etch resist.

To read this entire column, which appeared in the January 2022 issue of *PCB007 Magazine*, [click here](#).



PCB007 Highlights



EIPC Technical Snapshot: A European Roundup ▶

Although it was originally proposed to hold a one-day face-to-face EIPC conference in Frankfurt, travel restrictions in Germany made this impractical. But the Technical Snapshot webinar format has proved so successful that it was decided to run an extended version as an alternative—two sessions, with three presentations each. It worked extremely well. The carefully selected program on February 23 featured excellent speakers, and seamless organisation added up to an outstanding event.

Happy Holden Reflects on Successful IPC APEX EXPO 2022 ▶

The attendance at this year's IPC APEX EXPO seemed higher than I expected, so thank you all for making the necessary arrangements to attend. One of my cherished reunions was with Pete Starkey, who fought through the red tape of government restrictions to make his way from England for the show.

Rogers Corporation Reports Q4, Full Year 2021 Results ▶

Rogers Corporation announced financial results for the full year and fourth quarter of 2021.

Institute of Circuit Technology: A Novel Approach to Recycling PCBs ▶

A two-year project funded by an Innovate UK SMART Grant aims to reduce the impact of e-waste using naturally derived, biodegradable and nontoxic products. Those attending the webinar for the Institute of Circuit Tech-

nology's annual meeting on March 2 learned more about the project, as well as statutory paperwork obligations of the UK REACH regulations.

Calumet is Bullish on Additive and Semi-Additive ▶

Calumet Electronics has been a domestic pioneer with additive and semi-additive electronics manufacturing processes. We recently asked Calumet's Todd Brassard and Meredith LaBeau to discuss the state of this technology, which traditional processes that they might replace, and some of the challenges facing OEMs or PCB shops that are considering these options.

IPC Student Director: Three Things IPC APEX EXPO Taught Me ▶

IPC APEX EXPO 2022 was my first in-person APEX EXPO event, and it surely did not disappoint. The show this year was packed with high quality technical courses, engaging professional development courses and, of course, an admirable show floor exhibition. This year APEX EXPO really resonated with me, and I would like to leave you with three insights I learned while attending.

Arlon Takes on Role as EMC Master Distributor in North America ▶

Arlon EMD, a division of Elite Materials Company (EMC), and an American manufacturer of specialty laminates is assuming the role of Master Distributor for EMC materials in North America. Arlon has a 45-year history of manufacturing specialty materials for the aerospace, industrial and military (AIM) markets.

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Design for Test, Part 3

Designers Notebook

by Vern Solberg, CONSULTANT

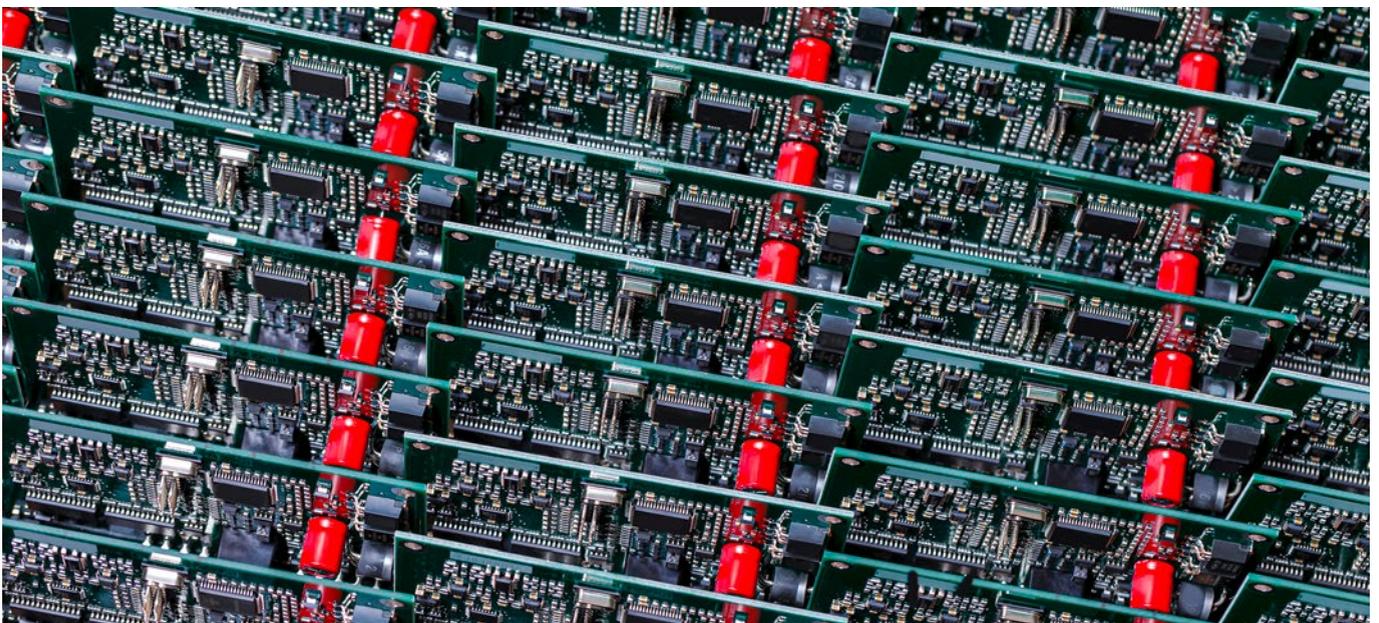
The general trend in electronics is to improve performance and minimize product size, often leading to more complex printed circuit boards and higher component density. Semiconductor packages in particular have become more complex, with many having multiple functions interconnected within the package or onto the silicon itself. For products with very high component density, companies soon realize that 100% test-probe access may not be possible. For example:

- A significant number of circuit boards include components assembled onto both sides, limiting access for physical probing
- It is impossible to probe the terminals of the very fine-pitch array configured components to identify functional or assembly process-related defects

- Very high density, small-size circuit boards do not always have accessible test lands, making it challenging to probe suspected nodes

Programmable logic devices (PLDs) and flash memory devices, for example, are often supplied in array packaging and soldered directly onto the circuit board. When a design includes programmable devices from multiple sources, the user must often rely on different software variations for programming these devices.

The focus of [Part 1](#) and [Part 2](#) of this “Design for Test” series was on bare-board testing and fixed-probe assembly test. Information gathered for Part 3 furnishes the designer with an overview of preparing for boundary scan testing, an integrated method for testing interconnects on populated printed circuit boards.



Electrically testing assembled circuit boards in a high-volume production environment requires a significant amount of engineering resources to develop the fixtures and programming required for in-circuit testing. Increasingly, the more complex semiconductor devices feature bus technology, enabling the potential to rapidly access thousands of test nodes for evaluating each component's function and interconnection integrity.

Network access can be made from board edge contactors or by surface probe contact to a few designated semiconductor terminals. This is an extremely thorough test method, enabling both in-circuit test coverage and system diagnostics. Implementing boundary scan negates the need for the traditional ICT "one node per net" requirement (at least on the devices furnished with self-test capability).

JTAG Test per IEEE 1149.1

Joint Test Action Group (JTAG) is a team of test engineering specialists that developed a standard procedure for verifying designs and testing complex circuit board assemblies. Although the process requires that unique test programs be generated before use, the programming provides a cost-effective method for testing products having restricted surface area for probe interface. This boundary-scan test architecture offers the capability to efficiently test high-terminal-density core logic

components, capturing functional data while the device(s) operate normally. Boundary-scan cells built into each device capture data from core logic signals. This captured data is then serially shifted out and externally compared to projected results (Figure 1).

Boundary scan testing can identify structural fault locations, even beneath array-configured semiconductor packaging, without requiring physical access to all nodes on the circuit board. In a typical boundary scan test, the tester sends diagnostic signals to the device's data input pin. The boundary-scan cells capture the signals and serially shift them through the core logic. The output is then serially shifted out of the core through the data output pin.

Test Node Access Requirements

The JTAG boundary scan test technique uses a shift register latch cell built into each external connection of every boundary scan compatible device. One boundary scan cell is contained in the integrated circuit line adjacent to each I/O pin or terminal, and when used in the shift register mode it can transfer data along to the next cell in the device. There are defined entry and exit points for the data to enter and exit the device, and it is therefore possible to progressively link several devices together.

The test equipment typical of that developed by JTAG Technologies (Figure 2) offer maximum flexibility and independence and can be

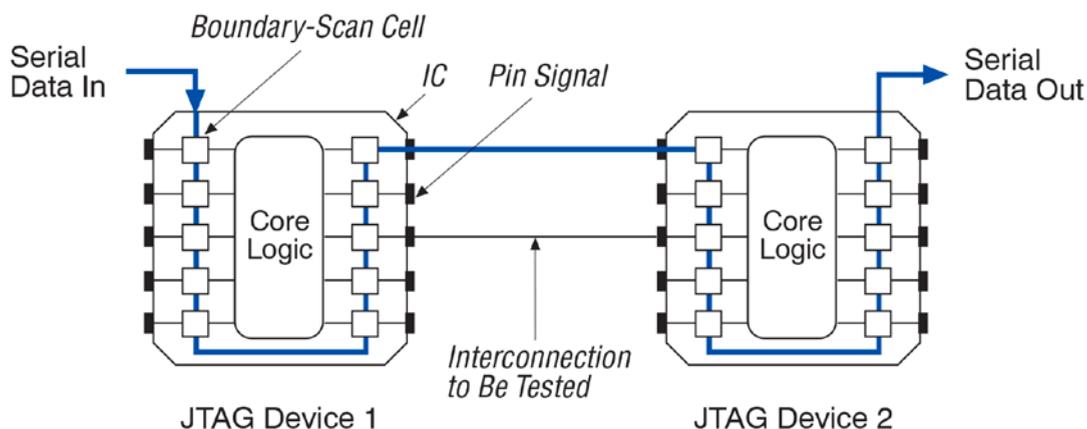


Figure 1: Basic concept of boundary scan testing. (Source: Altera Corporation)



Figure 2: Stand-alone JTAG/boundary-scan test station. (Source: JTAG Technologies)



Figure 3: Flying probe test system for providing maximum access. (Source: SPEA Test Systems)

set up as a stand-alone boundary-scan station integrated or combined with functional test and in-circuit test (ICT) or when using flying probe testers (FPT).

There are several control and data lines that form the test access port. These lines, known as test clock and test mode select, as well as an optional test reset line, are connected in parallel to the semiconductors in the boundary scan chain. Connections designated test data input and test data output are daisy-chained together to provide a path around the boundary scan enabled devices. Functional data is sent into the test data input node of the first semiconductor. Output from the first device is next connected to test data input of the next device(s).

Boundary scan implementation benefits include:

- Accelerate new product development
- Reduced time-to-market
- Fast and efficient test program generation
- Ideal for boards undergoing design revisions

The JTAG test procedure is highly versatile and will be used across the circuit board assembly production process for design verification, in-system programming, testing, and debugging procedures. Boundary scan testing will rely on built-in component test functions,

typically accessing four to six terminals of the semiconductor package as noted above. These terminals enable full analysis of the device. Fault detection is achieved by exploiting test-enabled components on the PCB which, in addition to their normal functionality, provide special test logic that scans through the serial JTAG interface.

X-JTAG has been working with a variety of test solution providers, including flying probe test system providers, to offer the best-in-class test capability and value for users. Ensuring continuous design for test improvement, and that testing ball grid array (BGA) devices on dense boards does not affect test coverage in, will require combining JTAG boundary scan and bed-of-nails with high-speed flying probe test systems (Figure 3) to achieve the absolute best results.

Powerful and easy to use, integrated testing enables engineers to minimize test time while maximizing test coverage.

Documentation Transfer for Assembly Test

The test program engineering specialist will require the netlist for the specific circuit board designated for testing, and will include boundary scan description language files for the boundary scan for all components contained within the circuit. With this information it is

possible for the test program engineer to create the test patterns used to accomplish the test. This data allows the system to detect and isolate any faults for all boundary-scan testable nets within the circuit. It is also possible for the test program developer to create test vectors that enable the system to detect faults on the nodes or pins for non-boundary scan components that are surrounded by boundary scan devices.

While requirements may vary, most documents required for setting up assembly test are quite standard to the industry. These include:

- **Assembly detail:** This will include graphics representing component outline, location, and reference designators for each device mounted on the board surface
- **Electrical schematic diagram:** Will furnish interconnect detail between all passive and active components mounted on the board's surface with corresponding reference designators
- **Circuit board fabrication detail:** Will include the primary mechanical outline dimensions, tooling locations, materials specified for fabrication, and circuit layer sequence with a representative cross-section detail
- **CAD file:** The digital data developed for component placement and circuit interconnect will furnish specific X-Y component coordinates, component orientation, and features provided for test probe access
- **Gerber file:** The Gerber file is a standard vehicle developed for PCB design data storage or transfer of PCB circuit image for each layer of the board and includes solder mask and nomenclature images
- **Bill of materials:** All components are listed by type, value and/or identifying part number and quantity. For two sided SMT assembly, component types are to be separated and identified by where located
- **Approved vendor list:** The vendor list represents the user's "qualified suppliers" for all materials and components designated for the circuit board assembly

- **Netlist:** Identifies the electrical connections (node) between component terminals in the circuit. The list will include component reference designators, component type, and terminal numbers
- **Test node X-Y coordinates:** The specific location of each node identified on the netlist must be referenced from a single fiducial target feature chemically etched within the circuit pattern

In addition to the documentation noted above, the circuit board developer will furnish requirements related to the end product's expected operation or use environment and include key data for all non-standard semiconductors.

Boundary Scan Test Compliance

Prior to releasing the board for fabrication, the designer and/or cognizant engineer responsible for developing the board will review the design with the test program developer to ensure the end-product can be tested effectively. If the design cannot meet full probe access to all nets or boundary scan terminals, the test fixture developer will probably request the addition of any test lands needed to enable the effective probing of all nodes in the network. Doing so may challenge the designer in altering the design to add test probe features, but the change will not likely affect the price of the actual circuit board fabrication. However, it will make a significant difference in achieving 100% testability of the PCB design. **DESIGN007**

Resources

1. JTAG Technologies, Technical support Americas: support@jtag.com.
2. XJTAG Technologies, "Design for Test Guidelines:" enquiries@xjtag.com.



Vern Solberg is an independent technical consultant, specializing in SMT and microelectronics design and manufacturing technology. To read past columns or contact Solberg, [click here](#).

Mandatory Masking Guidelines

Target Condition

by Kelly Dack, CIT, CID+

I was recently asked to participate in a video interview to discuss the topic, “Who defines the solder mask clearance for a PCB design?”

Though I’m not certain if the interview will be published, it is a fair topic to cover here as there are a few designer opinions I’ve come across which could use a little masking themselves, as they appear to be uninformed and can come across as downright dictatorial. After spending a few years now as a captive PCB designer working within the walls of PCB fabrication and assembly, I am qualified to say that it takes exhaustive communication efforts to work with our manufacturing stake-

holders when a design does not allow for a manufacturer’s unique manufacturing process capability.

Solder Mask

Printed board designs which move on to the component assembly phase include a coating of solder mask. It is often referred to as solder resist. Many know it as “the green coating,” though it can be procured in a variety of colors. This material serves a dual purpose. It provides a coating which seals the exposed outerlayer copper conductors, preventing them from becoming oxidized or contaminated. But

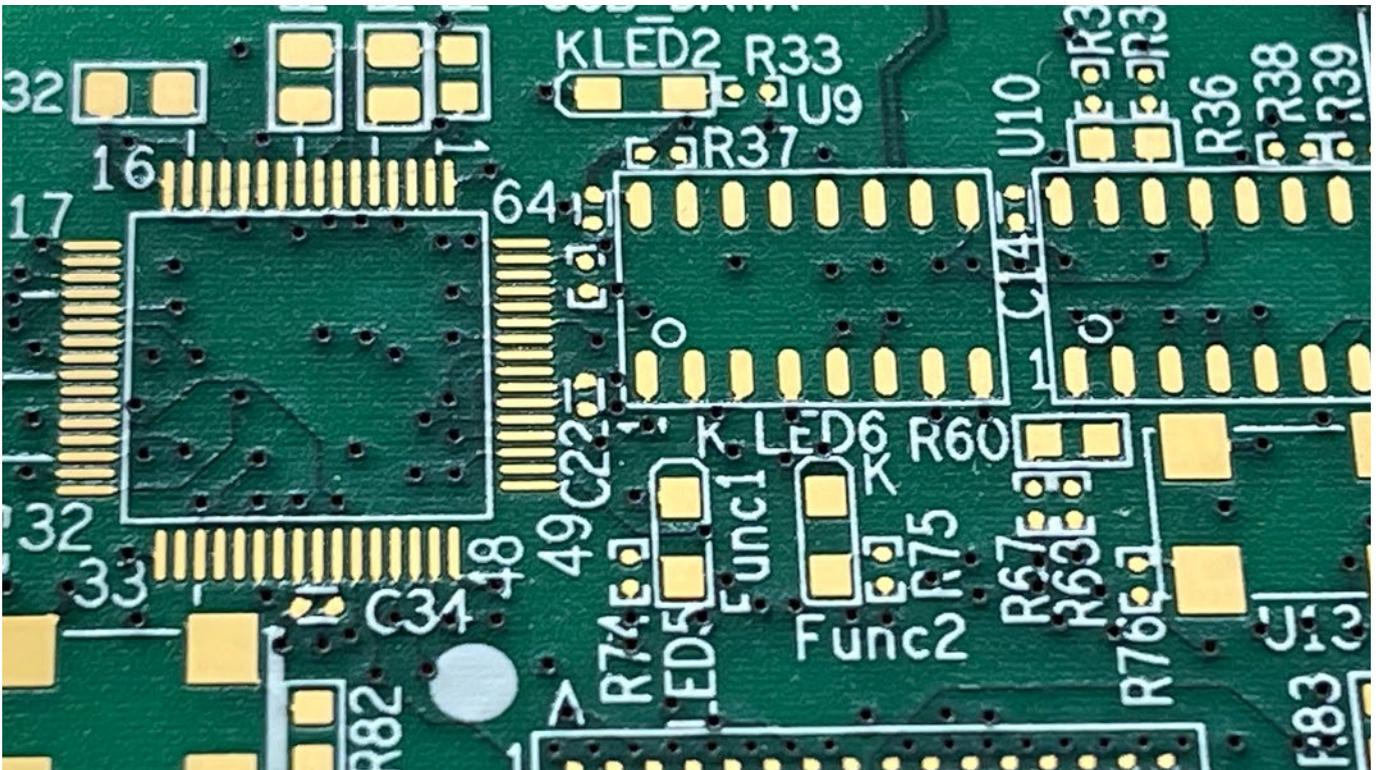
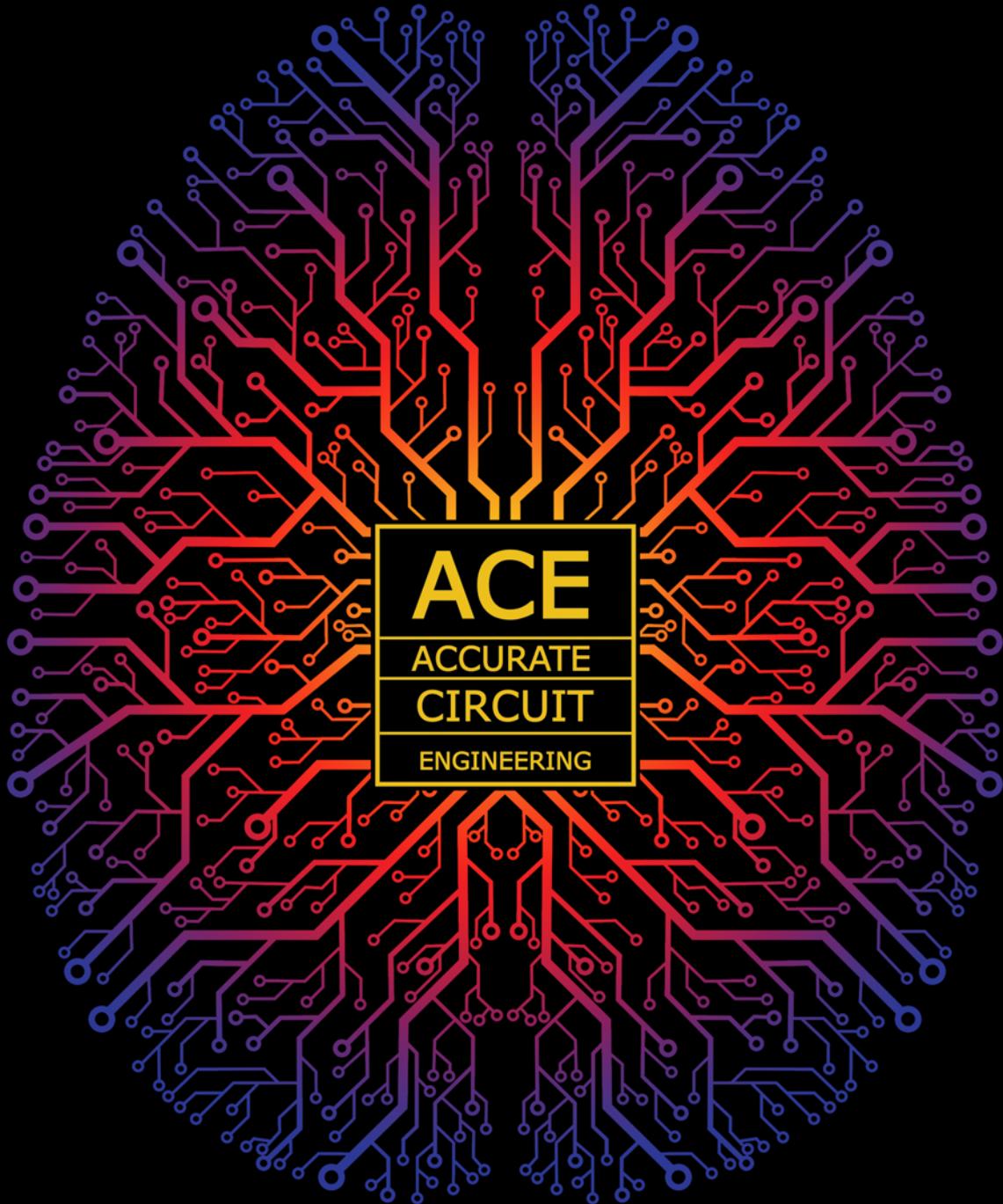


Figure 1: Example of solder mask.

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the main purpose of solder mask material is—are you ready for this?—to mask solder. During the reflow phase, the solder melts and will flow away from the contacts if not masked.

How Much Clearance?

In all cases, unless allowed by design, solder mask material is not allowed to end up on solderable land surfaces because it blocks or masks the solder from coating the intended surface to be welded. For instance, if a solderable land surface on a PCB happens to receive a lost blob of solder mask which mistakenly finds itself on a land during processing, or is missed in inspection and continues to the assembly soldering process, the anomaly will corrupt the solder joint by reducing the surface area of the land. This is considered a nonconforming defect in the pages of the IPC-A-600 Acceptability of Printed Boards (Figure 2).

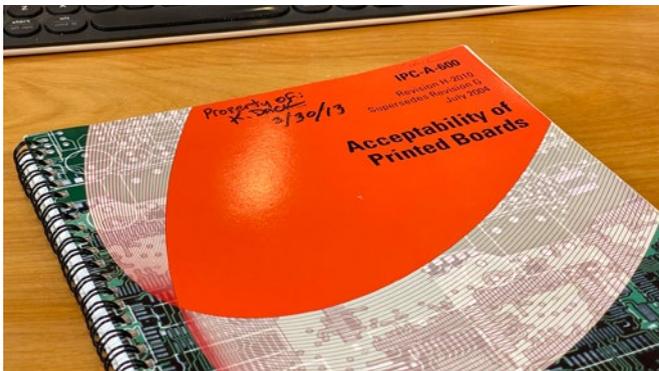


Figure 2: Find information about manufacturing target conditions in the IPC-A-600 Acceptability of Printed Boards.

But there are other manufacturing conditions which can cause solder mask material to end up on solderable surfaces. Misalignment of the artwork, material movement, and expansion or shrinkage of the PCB over the entire span of its length are conditions which must be considered. These are conditions for which additional solder mask clearance is required. Therefore your design tool supplier has added a control feature in your design tool. But how do you set it? What values do you use?

For years, I have asked these questions of the students in the IPC CID classes I teach and



Figure 3: Setting the solder mask clearance values of your design tool.

I've heard some very interesting opinions. One will say, "I have had very good luck by setting my solder mask clearance to 6 mils (0.006")." Another will brag that his supplier is so good that clearance can be set at only 2 mils (0.002"). Still another argues that for consideration of "DFM," everyone in their design group opens up the clearance to a whopping 10 mil (0.010") clearance.

The Goldilocks Zone

Again, per the widely accepted IPC acceptance criteria, no solder mask is allowed to end up on solderable lands as a manufacturing defect related to imaging, alignment, or sloppiness. So, with regard to DFM, a PCB designer might conclude that an overly robust clearance would be the best choice to help with PCB manufacturing as it makes the target zone hard to miss. But wait a minute here. As "the hub" of the PCB manufacturing process, a PCB designer must consider all the stakeholders' requirements. While the PCB supplier might applaud this DFM consideration as something they'll not have to worry about, the decision

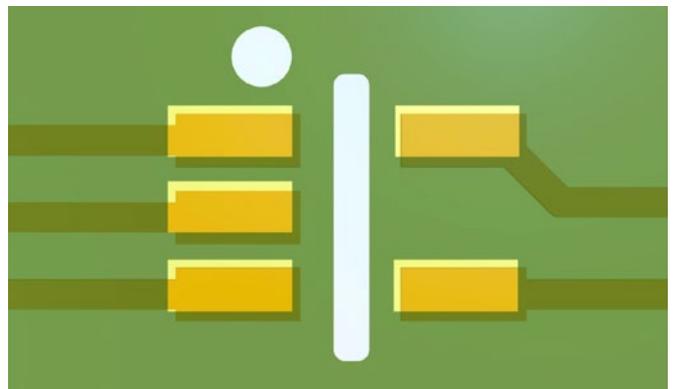


Figure 4: Too little clearance.

will most certainly affect the assembly stakeholders in a negative way. Let's examine the Goldilocks zone for solder mask clearance.

The two-mil clearance example in Figure 4 challenges fabrication capability for some volume production suppliers. If the image misregisters even a little, the board fails acceptability due to solder mask material on lands.

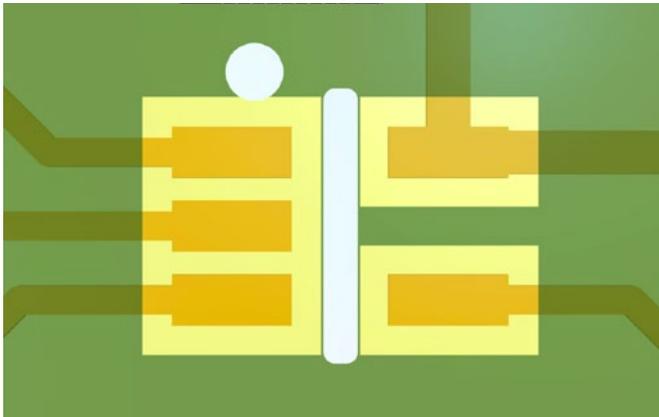


Figure 5: Too much clearance.

If the solder mask clearance is too “robust,” as shown in Figure 5, the clearance will void masking between lands, possibly allowing solder at the assembly level to drift or “bridge” and short to neighboring lands. Notice that significant portions of the traces entering the land are not covered with solder mask. This condition allows solder to spread out away from the contact points of the land pattern and creates the notoriously problematic condition of inconsistent paste geometries.

Target condition for all classes: No solder mask misregistration. The solder mask is cen-



Figure 6: Clearance is just right and matches supplier capability.

tered around the lands within the clearance space provided. Figure 6 shows solder mask coverage which tightly surrounds the lands and provides for optimal solder dams. But for many volume suppliers this tight manufacturing constraint capability cannot be met due to process or equipment limitations or advanced design topologies. In this case, should the PCB supplier's CAM engineer be allowed to grow the clearance between the contact land and the solder mask opening to the point that it will not adversely affect solderability but allow for potential misregistration? Read on.

Avoiding DFM Confusion

By setting the solder mask clearance in your design to a certain value you are in effect dictating the design parameters for solder mask clearances unless you make some notational provisions. We've covered the case in which designers set their solder mask clearances based upon checking in with their own favorite fab shops. This may work for the design in the proto stages, but if the PCB designer cannot check in with the production supplier who will be building the PCB in production, what is the point? The point is that far too many designers do not understand that just because “their own” custom prototype shop can accurately mask with nearly zero increase or “swell” of the solder mask opening doesn't mean that many volume-capable, offshore suppliers possess the capability. This fact is compounded by another fact that by the time the design goes to volume, the PCB designer's favorite proto-shop is long removed from the EMS assembly stakeholder which will be ordering the boards from their own suppliers which most certainly will have entirely different manufacturing constraints.

When there is a lack of vision the people perish, says the proverb.

So, who is “the hub” of the manufacturing process helping by interpreting DFM as “dictate for manufacturing” when they have absolutely no vision regarding the capabilities of the EMS provider's supply chain?

Help the Supplier to Achieve the Target Condition

I really do like to think that our design data serves as the hub of the manufacturing process. In my mind the data and fabrication specification criteria must be output with all the PCB industry stakeholders in consideration so that it provides a viable starting point for all to be successful in hitting the design, procurement, manufacturing, test, and inspection targets of the whole team project stakeholders. How can a PCB designer “design” solder mask clearance without knowing the manufacturing constraints of unknown suppliers?

The key to this dilemma is found within a simple twist of context which is occurring within our industry.

With the continuous developments in the creation and utilization of intelligent design and manufacturing data, smart factories leveraging IPC CFX standards will have more and more access to our data to make corrections without the PCB designer—who may be blind to the process—being involved. This advanced paradigm sets the stage for our whole PCB industry of product stakeholders to design, manufacture, and collaborate with each other simultaneously with access to standardized, accessible data.

I suggest setting the solder mask clearance values in a design layout to “zero” and allow the PCB supplier to swell the openings to the minimum value which their overall manufacturing capabilities can achieve acceptability. Coupled with a simple fabrication note which will allow the supplier’s CAM group of manufacturing engineers to make clearance and sliver adjustments, your EMS supplier will no longer have to field engineering queries regarding these issues. This philosophy will transfer the responsibility to the stakeholders who are the most qualified, and most in touch with the manufacturing processes and capabilities, to vary the solder mask clearance values throughout the design as required. By doing so, they will manufacture with design to set the design data up for success. **DESIGN007**



Kelly Dack, CIT, CID+, provides DfX centered PCB design and manufacturing liaison expertise for a dynamic EMS provider in the Pacific Northwest while also serving as an IPC design certification instructor (CID) for

EPTAC. To read past columns or contact Dack, [click here](#).



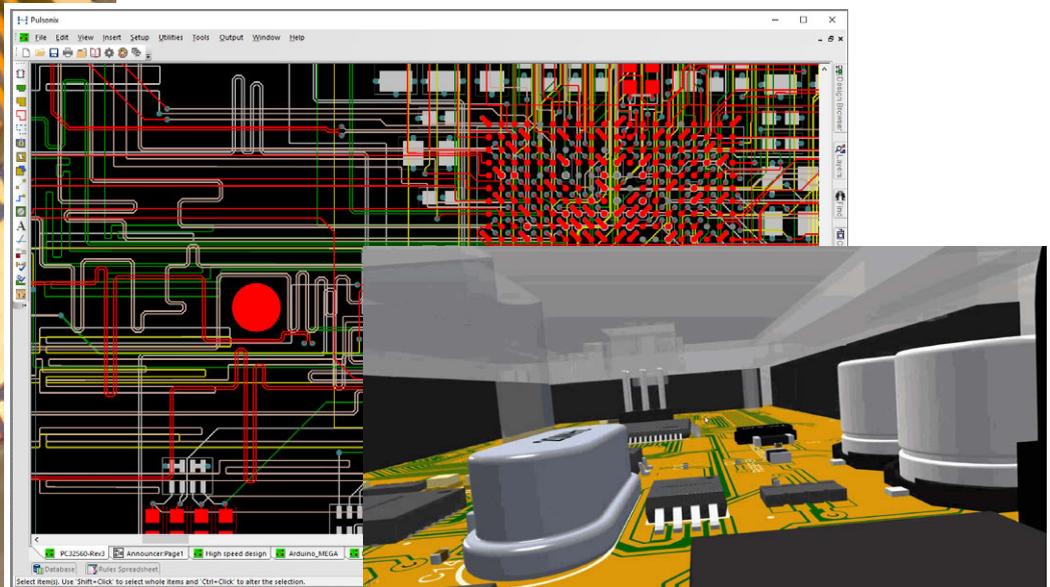
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MilAero007 Highlights



Doug Pauls, Collins Aerospace, Receives Dieter Bergman IPC Fellowship Award ▶

Doug Pauls holds a B.A. in chemistry and a B.S. in electrical engineering, worked nine years for the Navy, eight years as technical director of Contamination Studies Labs, and 19 years at Rockwell Collins (now Collins Aerospace), in the Advanced Operations Engineering group, where he is a principal materials and process engineer. Doug was awarded the Rockwell Collins Arthur A. Collins Engineer of the Year Award in 2004.

SMT Perspectives and Prospects: Critical Materials, A Compelling Case, Part 1 ▶

It has come time for a national strategy, in a deliberative and comprehensive manner, to address the critical materials/minerals. Doing so is increasingly critical to the long-term economy, national security, and the nation's global competitiveness. With the handling of conflict minerals as an exemplar, there is perhaps an even more urgent need to rally another concerted effort to tackle the critical materials/minerals.

Cadence, Dassault Systèmes Partner to Transform Electronic Systems Development ▶

Cadence Design Systems, Inc., and Dassault Systèmes announced a strategic partnership to provide enterprise customers in multiple vertical markets, including high tech, transportation and mobility, industrial equipment, aerospace and defense, and healthcare, with integrated, next-generation solutions for the development of high-performance electronic systems.

David Pogue: Is the Fear of Change Holding Us Back? ▶

David Pogue, an American technology and science writer and TV presenter, talks about today's technology, the breakthroughs that have shaped our current landscape, and whether fear of change and innovation is what's keeping us from the next technological revolution.

IPC Applauds Biden's Focus on Semiconductors, Urges Passage of Competitiveness Legislation ▶

During his State of the Union address, U.S. President Joe Biden urged Congress to pass much-needed funding for semiconductor manufacturing and other advanced technologies as part of a new competitiveness measure.

EMC Launches 112Gb/s Design and New IC Substrate Materials at DesignCon 2022 ▶

At DesignCon 2022, EMC will highlight extreme low loss materials EM-892K / EM-892K2 ("K" indicates low Dk/Df glass, while "K2" stands for next generation low Dk/Df glass).

Electronics Industry Praises Congress for Providing \$7.5 Million for Lead-Free Electronics R&D ▶

The U.S. Senate approved an FY 2022 spending package that contains \$7.5 million for further research and development on lead-free electronics in defense and high-performance applications, sending the measure to President Biden for his expected signature.

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Turn Down the Heat, Go Green on Resins

Sensible Design

by Beth Turner, ELECTROLUBE

This month, I continue my series on how resins are currently playing a vital role in the modern world, while also offering an insight into their thermal conductivity, suitability for RF applications, and exploring a new era of bio-based encapsulation resins that not only improve the environment at large, but also end-use reliability and increased consumer satisfaction.

1. Thermally conductive encapsulation resins: Why would you use one of these over a conventional thermal paste or TIM?

Thermal pastes are often applied between heat-generating components and heat sinks to

maximise heat transfer, improve device reliability, and extend lifetime. This is due to their high thermal conductivity values and, when applied as a thin bond line, they exhibit low thermal resistance. By applying a thin, uniform layer of a thermal interface material, it is possible to obtain the maximum efficiency of heat dissipation. It is also important to consider the operating temperature conditions; in the case of LEDs where devices are switched on and off regularly, this results in the unit going through a thermal cycle, heating up once switched on and cooling again when powered down. Over the lifetime of the product, many thermal cycles take place, and this may affect the posi-

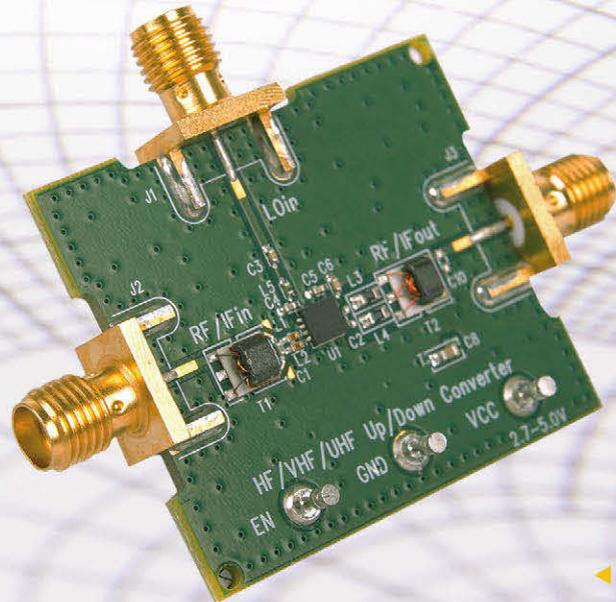




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tioning of a thermal paste over time. In other words, a poorly formulated paste can migrate over time and reduce the efficiency.

Thermally conductive resins can be used as an alternative solution to “keep things cool.” Such resins also provide lots of other value-added benefits such as mechanical protection. If protecting components from mechanical shock and vibration are a concern, then a thermally conductive encapsulation resin is likely to be the best solution as it adds a level of stability that helps to insulate the potted components against adverse mechanical movements. The arch enemy of electrical and electronic devices is the dreaded “moisture”; besides producing short-circuits moisture also causes corrosion, which leads to premature deterioration of components. You might also need to protect electrical or electronic components from encountering chemicals, including acids, alkalis, solvents, and other substances that pose a threat to delicate circuits and components. Encapsulating with a thermally conductive resin will help to ruggedize against all these harsh external factors. Lastly, it’s worth citing that, aside from providing all the protections listed above, opaque potting and encapsulation resins also conceal what lies beneath. This could provide an effective foil against counterfeiters or those wishing to copy a circuit layout, helping you to protect your intellectual property.

2. Which chemistry (if any) lends itself to thermal conductivity, i.e., epoxy, polyurethane, or silicone?

Epoxy, polyurethane, and silicone chemistries are all capable of producing resins with high thermal conductivity values. The thermal conductivity is dictated by the type of filler used, particle size, particle size distribution, and morphology. When these four factors are carefully considered as part of the product design, you get encapsulation resins with high thermal conductivity values, irrespective of the reactive chemistry that hold the filler in place.

One of our products provides the highest level of thermal conductivity combined with environmental protection afforded from the encapsulation process. This highly-filled epoxy resin possesses very high thermal conductivity, 1.54 W/m.K. Thermal conductivity, measured in W/m.K, represents a material’s ability to conduct heat. Bulk thermal conductivity values give a good indication of the level of heat transfer expected, allowing for comparison between different materials. We utilise a modified transient plane source (MTPS) method, amongst others, to provide accurate comparisons of bulk thermal conductivity. Note there are different methods to determine thermal conductivity so remember that when comparing datasheets from different suppliers.

3. Apart from the obvious assumed benefit to the environment, what other benefits could be expected from bio-based resins and are there more to come?

There are many observed benefits to using bio-based resins aside from the obvious environmental credentials. Research has shown that quality of performance can be significantly improved. Resins where the reactive component is derived from biobased feedstocks can have improved performance in harsh environments, particularly their electrical insulation in hot, humid conditions, as compared to reactive components derived from crude oil. Comparing biogenic powders with mineral rock powders shows that bio-sources can be used to effectively dissipate heat away from high power density devices and they show improved protection in underwater environments.

There can also be health and safety benefits. For example, the curing agent or hardener typically used for polyurethanes is based on methylene diphenyl diisocyanate (MDI); crude oil is a crucial raw material for the synthesis of MDI. It is a respiratory sensitiser and harmful if vapours are inhaled, from a H&S label perspective it contains the “exploding chest”



pictogram (GHS08/health hazard). We can replace this hardener with alternative reactive agents derived from bio-sources which do not contain the GHS08 pictogram and are much safer for operators to use.

4. Do bio-resins lend themselves to RF applications?

They most certainly do. We have another with bio-sourced content of over 60%, which is an unfilled polyurethane resin that has found success in sensor applications as it has a low dielectric constant (relative permittivity). Most IoT communication takes place in blocks of the radio frequency spectrum; a low dielectric constant is essential to ensure the resin does not interfere with the RF signal. It provides excellent electrical insulation across a wide operating temperature range, which is required for long-term performance, and has a high toughness, offering protection from physical shock and vibration. It has good resistance to lots of deleterious substances, making it the ideal choice for ruggedizing sensors exposed to harsh environments.

5. What sort of testing programmes have these new bio-resins been subjected to?

The bio-resins have been tested extensively. There is a common perception that going green, or bio-based, means there will be some sort of compromise on quality of performance. For a new product line to be relatively disruptive and have a high bio-derived content, extreme testing was essential to generate valuable data. The barriers to entry for encapsulation resins in the electronics market is relatively low when compared with other ruggedization techniques such as conformal coatings. Typically, a lot of resin qualification comes down to customers screening for their own unique application; the resin either passes or fails. There is no formal industry standard that outlines a specific test criterion; this is mainly because every application is truly unique.

To recall just a handful of the tests these new bio-resins have been subject to:

- Surface insulation resistance testing (SIR) on copper and tin B-24 test coupons at 85°C/85% RH, to ensure the encapsulant

remains electrically insulative in hot humid conditions

- Volume resistivity before and after immersion in water and salt water to ensure the bulk material remains electrically insulative in underwater applications
- Thermal shock testing at -40°C to +85°C for plastic housing and -40°C to +125°C for galvanised steel housing, to monitor for any cracks or loss of adhesion in this accelerated life test
- 1,000-hour thermal ageing was performed on type IV specimens in accordance with ASTM D638
- The tensile strength and elongation were measured before and after high temperature exposure for 100, 500, and 1000 hours to monitor the consistency in physical performance with long term exposure to high temperatures, to determine the maximum operating temperature

Numerous accelerated life tests have been performed to evaluate the performance of novel bio-based materials alongside commercially available resins derived from crude oil and mineral rock powders. Comparison of data concludes that “going green” can deliver per-

formance advantages in underwater applications as well as hot and humid operating environments.

Resins play an integral part in ensuring that an electronics product can survive for at least its design life, and often well beyond. Be it chemical, physical, or thermal, whatever the conditions, there is a resin system that can be found or developed to provide the protection required. I hope you have enjoyed learning more about the benefits of bio-based resins and what they can bring to your applications. Over the coming months I hope to provide more useful tips and design advice that will help make life a bit easier for those who are responsible for making the decisions on protecting components and circuitry. Watch for my next column, where I will be exploring resin systems in more detail. **DESIGN007**



Beth Turner is head of encapsulation resins at Electrolube. To read past columns from Electrolube, [click here](#). Download your free copy of Electrolube's book, *The Printed Circuit Assembler's Guide to... Conformal Coatings for Harsh Environments*, and watch the micro webinar series “Coatings Uncoated!”

Helping the World Build Electronics Better

Hundreds of experts from around the world will discuss electronics manufacturing standards in more than 80 standards meetings May 7–12, at IPC SummerCom 2022 in Milwaukee, Wisconsin.

Facilitated by representatives from OEMs, PCB manufacturers, EMS providers, design firms, and other organizations, IPC standards development committees establish benchmarks for excellence in electronics manufacturing.

According to David Bergman, IPC vice president of standards and technology, industry standards enable companies to negotiate commerce and they contribute directly to the success of the industry as a whole.

Standards development committee meetings will cover industry benchmarks in assembly and join-

ing; assembly equipment, base materials; cleaning and coating; electronic documentation technology; electronic product data description; embedded devices; environment, health and safety; fabrication processes; flexible and rigid-flex printed boards; high speed/high-frequency interconnection; management; packaged electronics components; printed board design, printed electronics; process control; product assurance; product reliability; rigid printed boards; terms and definitions; testing; and wearable electronics/e-textiles.

This year, IPC SummerCom will be co-located with the Electrical Wire Processing Technology Expo (EWPTE) at the Wisconsin Center.

(Source: IPC)



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DFM 101: Solder Mask and Legend

Article by Anaya Vardya

AMERICAN STANDARD CIRCUITS

Introduction

One of the biggest challenges facing PCB designers is understanding the cost drivers in the PCB manufacturing process. This article is the latest in a series that will discuss these cost drivers from the PCB manufacturer's perspective, and the design decisions that will impact product reliability.

Solder Mask Availability

Most shops provide a variety of solder masks to satisfy the needs of all customers. Table 1 is a description of typical solder masks currently available. The need for closer tolerances has driven the implementation of laser direct imaging (LDI) solder masks (laser-defined solder mask pattern instead of screening).

Solder mask is a protective coating that shields selected areas of a PCB from oxidation, handling and unwanted solder during assembly.

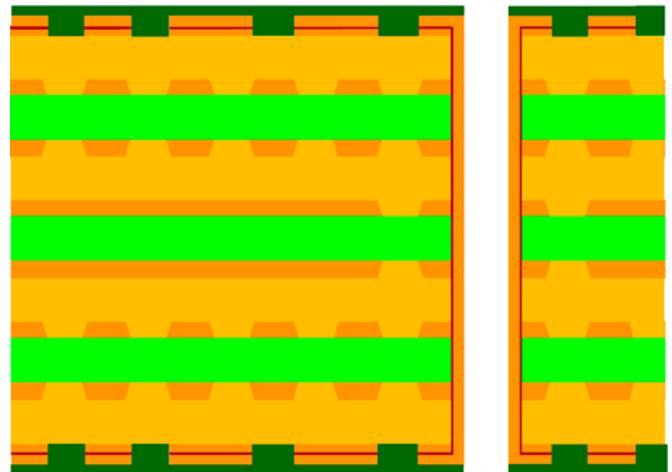


Figure 1: Green is the preferred solder mask color.

- Solder mask allows a 0.003" web to be placed between pads in an SMD array, provided the minimum spacing between these pads is 0.007" (by design).
- Green solder mask allows a 0.003" web to be placed between pads in an SMD array, provided the minimum spacing between these pads is 0.007" (by design). All colors cannot maintain this dam size.

SPECIFICATION	STANDARD PRODUCTION	ADVANCED OR PROTOTYPE
TYPE	Taiyo PSR4000, EMP 110	Taiyo LDI Solder mask
COLORS	All	
MIN. SOLDER MASK CLEARANCE	0.003" per side 75 µm per side	0.002" per side 50 µm per side
MIN. SOLDER MASK WEB THICKNESS	0.003" 83 µm	

Table 1: Description of typical solder masks available.



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- To assure no solder mask on any pad in an SMD array, the minimum solder mask clearance for a surface mount pad is 0.002” per side (not applicable for panel sizes over 18”x24”). As space permits, a clearance of 0.0025” per side is preferred.
- Allow 0.030” per-side solder mask clearance for score lines.
- To prevent solder mask from going into and/or plugging a hole, solder mask clearance should be 0.010” (0.005” per side) larger than the pad size on both sides of the board.
- Generally, the non-test vias are capped on the top side of the board. Thermal (epoxy) via caps will have a raised surface of approximately 0.0017” ±0.004” above the outer layer copper pad.
- This is to make sure the via hole being capped is not plated shut or plugged with solder during reflow (such as HASL). In this case, due to trapped air between the via cap and plug, the via cap may “dome” during the cure process, thus creating height 0.0035”.
- UV (acrylic) via cap will have a raised surface of approximately 0.0019” ±0.0004” above the outer layer copper pads. Unlike thermal (epoxy), UV (acrylic) is not influenced by plated or solder-plugged holes, therefore the via cap height will remain constant.

Tenting of Via Holes with Solder Mask

With via tenting, the annular ring and via barrel are capped with solder mask. On a board coated with LPI mask, the vias can be screened with an epoxy or acrylic solder mask material, creating a cap over the hole.

Artwork modifications necessary for processing are performed as part of the initial tooling. A separate design file must be provided by the customer, which includes only those vias which are to be capped. The customer needs to provide master pad solder mask and via fills, i.e., solder mask and via pads that are the same size as the outer layer pads.

Via Capping Design Constraints

- The maximum finished hole size for via capping is 0.020” diameter (preferred drill diameter 0.021”).

Note: via cap height thickness measurements may include solder and/or permanent solder mask thickness.

- For product that receives either immersion silver or tin, UV via cap material must be used and applied after the surface finish.

Legend Marking Design Guidelines

- Modern legend technology uses an ink jet printer for black or white legend; traditional technology is to screen it on.
- To ensure all letters, numbers and figures are legible on the finished board, character

SPECIFICATION	STANDARD PRODUCTION	NON-STANDARD PRODUCTION
TYPE	Ink Jet Printer	U.V. / Thermal
COLORS	White, Black	All
SMALLEST LINE WIDTH	0.003” (Aspect 7:1) 75µm (Aspect 7:1)	0.010” 254µm

Table 2: Legend marking design guidelines.

line widths should be greater than 0.006” and at least 0.030” high.

- Space letters at least 0.008” apart so they don’t bleed together.
- No legend nomenclature should overlap a copper pad or plane area.
- This is especially important for surface mount pads and fiducials.
- White is the standard legend ink color. Use the fabrication print notes to specify special features to be screened onto the board, and non-standard colors.
- All legend should be kept 0.003” (minimum) away from solder mask clearance.

Nomenclature

Letter size:

- Screened: 0.006” line width minimum
- Photoimageable: 0.004” minimum

Table 3 lists recommended letter sizes.

Note: Nomenclature placed over parallel or heavy copper traces may have poor legibility.

LINE WIDTH	HEIGHT AND WIDTH
0.004” (LPI)	0.020”
0.005” (LPI)	0.025”
0.006”	0.030”
0.008”	0.035”
0.010”	0.040”

Table 3: Recommended letter sizes.

Color:

- White (epoxy) preferred
- Yellow (epoxy)
- Black and white (LPI Ink) is also available

Considerations

Nomenclature over solder (HASL) will have poor adherence. Nomenclature placed over bare copper before HASL and immersion silver/tin will have an apparent copper “halo” after the HASL or immersion silver/tin. The artwork will need to be modified if this is not acceptable to the customer.

Understanding the cost drivers in PCB fabrication and early engagement between the designer and the fabricator are crucial elements that lead to cost-effective design success. Following your fabricator’s DFM guidelines is the first place to start. **DESIGN007**



Anaya Vardya is president and CEO of American Standard Circuits; co-author of *The Printed Circuit Designer’s Guide to... Fundamentals of RF/Microwave PCBs* and *Flex and Rigid-Flex Fundamentals*;

and author of *Thermal Management: A Fabricator’s Perspective*. Visit I-007eBooks.com to download these and other free, educational titles. He also co-authored *Fundamentals of Printed Circuit Board Technologies* and provides a discussion of flex and rigid flex PCBs at [RealTime with... American Standard Circuits](#). To read past columns or contact Vardya, [click here](#).

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FLEX007

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The Fascinating History of Wearable Electronics

Flexible Thinking

by Joe Fjelstad, VERDANT ELECTRONICS

Wearable electronics have been capturing much attention in the press, both technical and business, over the past few years. Articles for consumption by the public, as well as technical research papers on the topic, have been increasing steadily in recent times. However, wearable electronics are far from new. Moreover, the term “wearable” is quite fungible and encompasses a broad spectrum of prospective embodiments. The convenience and utility of

wearable electronics was, based on evidence, first conceived and conceptually reduced to practice over a century ago. Early in the history of electronics, the invention of the bi-telephone in-ear headphones were patented in 1891 by French electrical engineer Ernest Mercadier (Figure 1). Designed to be used by telephone operators, they even boasted perforated nipples to block out external sounds and support the apparatus.¹

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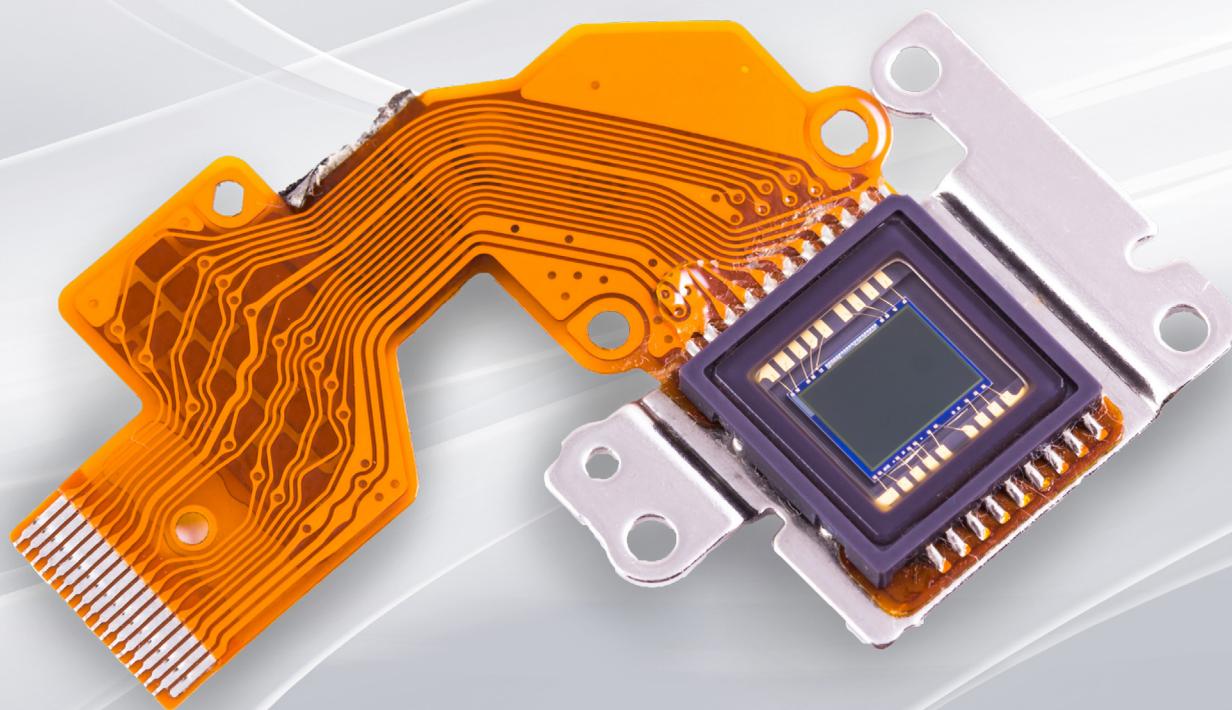
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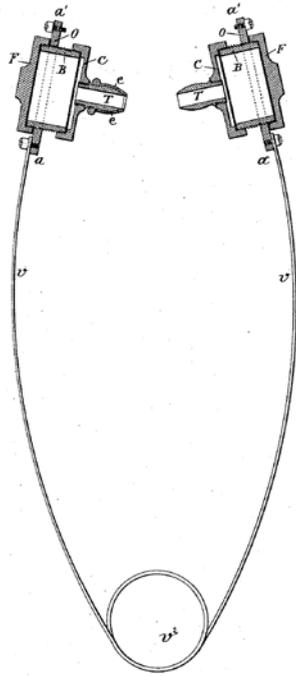


(No Model.)

E. J. P. MERCADIER.
BI-TELEPHONE.

No. 454,138.

Patented June 16, 1891.



Witnesses:
E. H. Kelton
E. H. Stewart

Inventor:
Ernest Jules Pierre Mercadier
By Richard S. B. Richards
his Attorneys

THE HERRICK PRESS CO., PHOTO-LITHO., WASHINGTON, D. C.

Figure 1: The first ever in-ear headphones from 1891, were designed to be “worn without inconvenience” or hands-free. U.S. Patent No. 454,138. (Source: patents.google.com)

A quick search online for photos of 18-year-old H. Day from the UK will show his 1922 invention of a top hat radio which appears to be the first invention of its kind. It was followed up 27 years later by inventor and gadgeteer Victor Hoeflich’s introduction of the “Man from Mars, Radio Hat.” The June 1949 issue of Radio-Electronics magazine had a two-page article describing the circuitry and construction of the radio.² The circuit was built on a flexible liner (Figure 3) that fit inside the hat which was covered by a chassis shield and a perfectly smooth interior liner. Hoeflich hoped his innovative packaging of a radio in a pith helmet would be a runaway success but just five years later, the pocket transistor radio was introduced, and the rest is history.

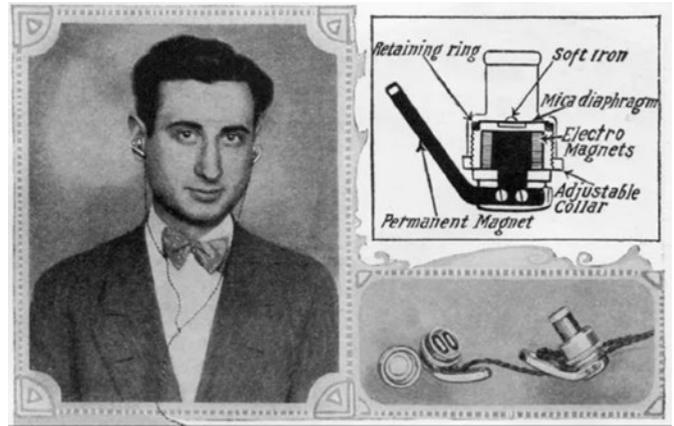
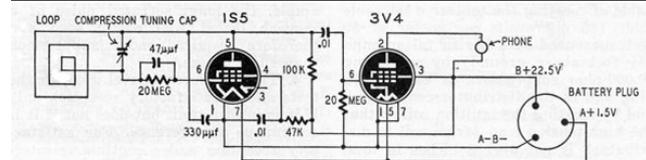
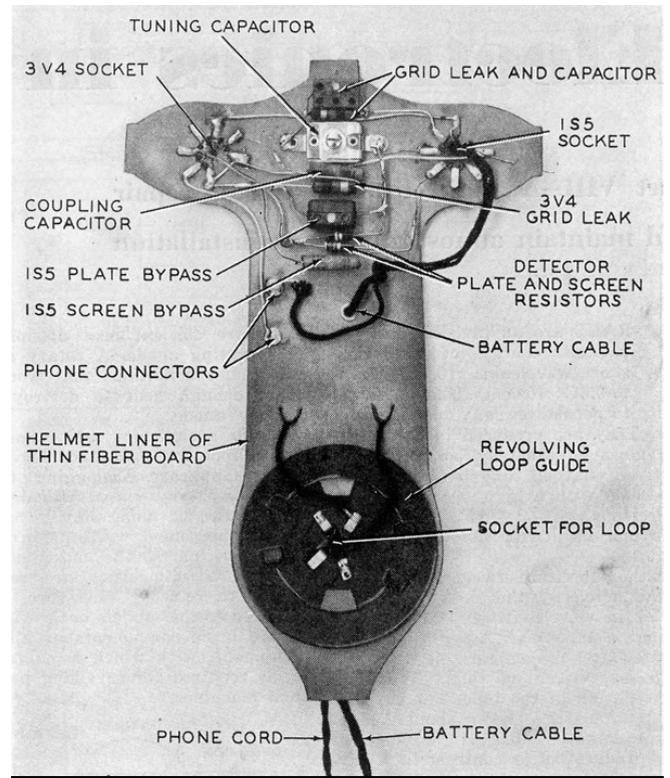


Figure 2: Demo of early earbud technology with the now-familiar shape and a flexible wire. (Source: May 1926 issue of Science and Invention)



The interesting detector circuit apparently adds considerably to the receiver's sensitivity.

Figure 3: The “Man from Mars, Radio Hat” internal circuit was built on a flexible liner. As shown in the schematic, the 1S5 vacuum tube converted the radio signal to audio and the 3V4 amplified the audio for the headphone. (Source: Wikimedia Commons)

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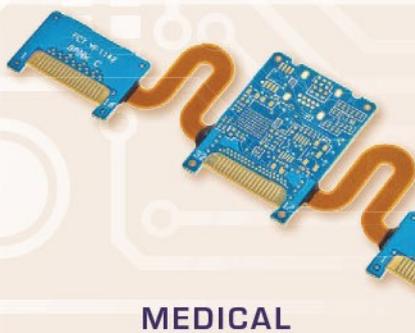
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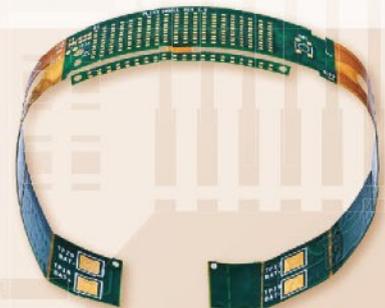
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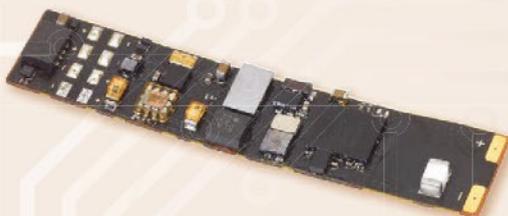
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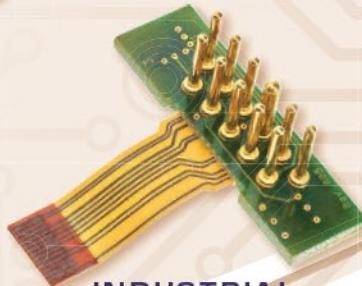
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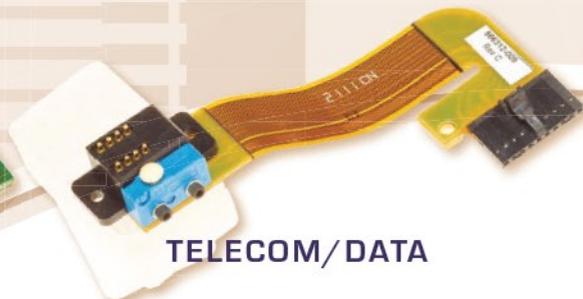
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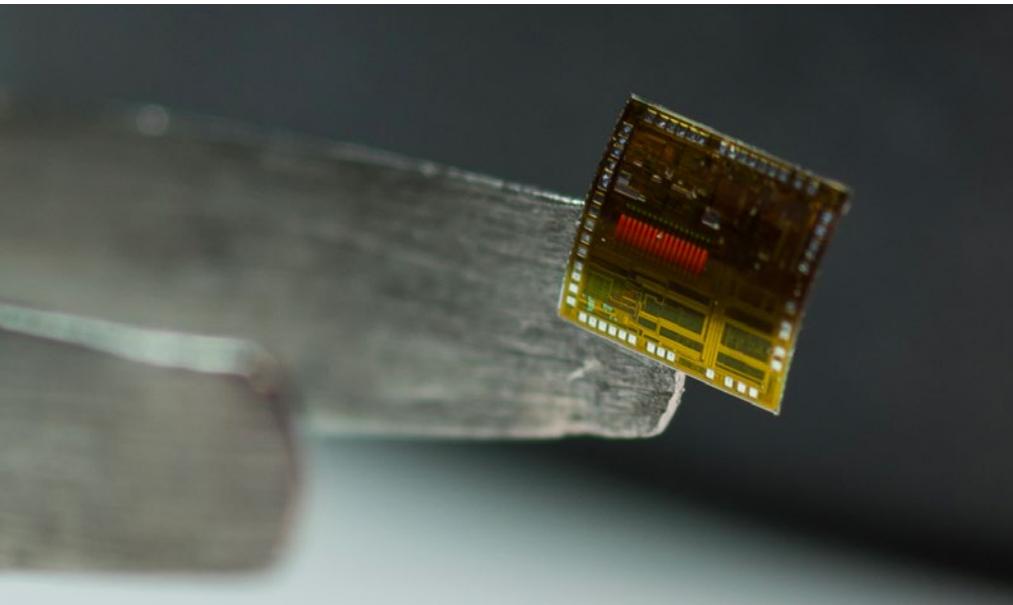


Figure 4: Silicon chips are brittle in their as-manufactured state, however, when thinned they can be bent and flexed as shown.
(Source: U.S. Air Force)

From those humble and practical beginnings, the spectrum of wearable electronic products has expanded immeasurably with improvements in materials, manufacturing, and processing technologies in concert with engineering and scientific creativity. Enabling most of the advances has been flexible circuit technology with integrated electronic devices of every imaginable type, including everything from simple LEDs to sensors of every stripe, processors, and even flexible batteries. What has also proven highly enabling to flexible electronic assemblies has been advances in silicon wafer thinning which makes normally brittle silicon integrated circuits truly flexible and bendable (Figure 4).

While thinning was developed for die stacking, it has proven an important benefit for making thin flexible electronic assemblies and thus opening doors to new applications. A collaboration between the Air Force Research Laboratory and American Semiconductor in 2017 produced a flexible silicon-on-polymer chip with more than 7,000 times the memory capability of any current flexible integrated circuit on the market at the time. The manufacturing took advantage of flexible hybrid electron-

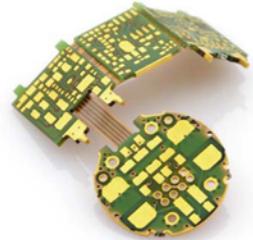
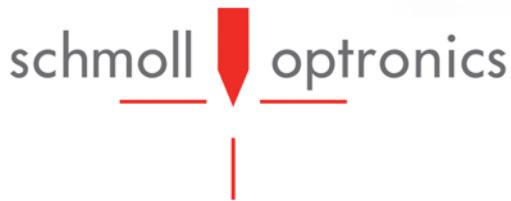
ics, integrating traditional manufacturing techniques with 3D electronic printing to create thin, flexible semiconductors that can augment efforts in wearable technology, asset monitoring, logistics and more.³

In recent years, some of the original terminology used exclusively for flexible has been altered and recast by technology marketers. What was once referred to as polymer thick film flexible circuit technology is being rebranded as “flex hybrid electronics” (FHE) and, with the newly intro-

duced term fueled by significant funding from the U.S. government (especially the military) and in-kind contributions from players in industry, FHE is making new electronic design industry inroads and bringing new-found attention to time-honored flexible circuit technology, with wearable electronics often serving as a marquee application under the newly applied terms.

For decades, flexible circuits/printed electronics have been employed to solve many challenges and create new solutions to problems; of high interest has been areas related to health, especially remote monitoring of individual health. Flexible circuits have long been used in medical products such as for the interconnection of piezo ceramic transducer heads for ultrasonic imaging systems, but they have also been successfully used in catheter diagnostics, such as for electrophysiology studies to pinpoint and correct heart nerve pathways to mitigate or eliminate life threatening heart arrhythmias. The recent boost in awareness of flexible circuit technology, brought on by the strong marketing of FHE, is causing a rising tide in interest, which is “lifting all boats” as increasing numbers of product designers turn

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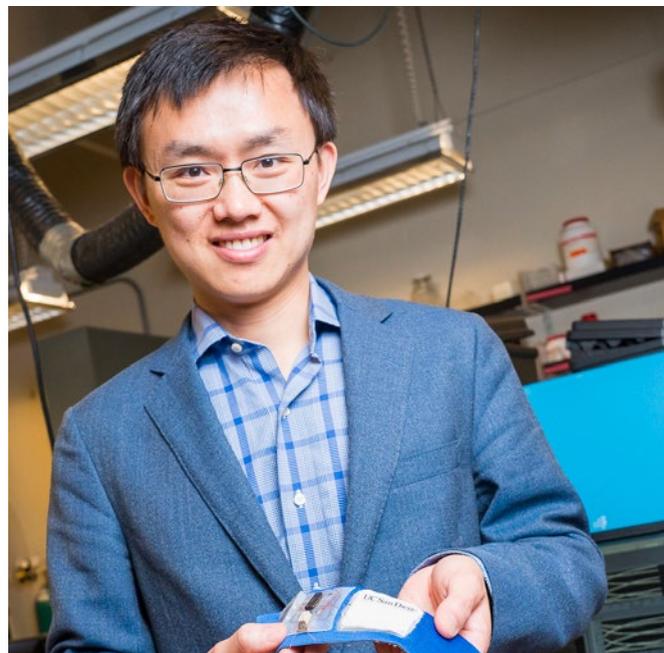


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to flexible circuit technology to solve old problems and address new ones, especially in the field of wearable electronics.

Today, physical fitness buffs are routinely employing flexible circuit-enabled products that help them monitor their vital signs “on the run” and transmit results wirelessly to smart devices in real time on their wrists or



Professor Sheng Xu

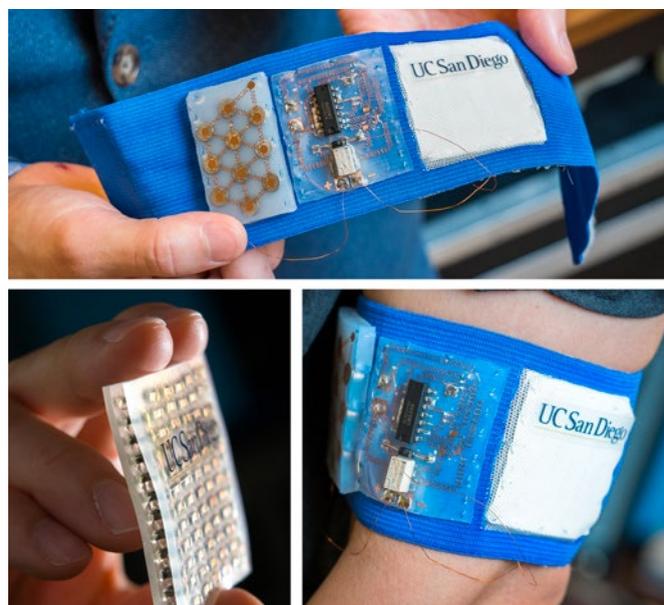


Figure 5: Prototype of the cooling and heating patch embedded in a mesh armband.
(Source: David Baillot/UC San Diego Jacobs School of Engineering)

in smart phones. Such thin flexible electronic devices are also used to help diabetics monitor their blood sugar in real time without having to stop and prick their fingers to measure glucose levels.

Flexible substrates are not the only kid on the block anymore. In the last decade, significant and growing attention has been given to stretchable circuits and stretchable electronics. Stretchable materials allow for circuit resilience not only in X and Y but also in the Z-axis allowing for a new dimension of design flexibility.

UC San Diego engineers have developed a wearable patch that could provide personalized cooling and heating at home, work, or on the go. The soft, stretchy patch cools or warms a user’s skin to a comfortable temperature and keeps it there as the ambient temperature changes. It is powered by a flexible, stretchable battery pack and can be embedded in clothing. Researchers say wearing it could help save energy on air conditioning and heating (Figure 5). Sheng Xu, UC San Diego professor of nanoengineering, developed the stretchable electronics for the system.⁴

“Woven” electronics are also now on the technological menu as e-textiles begin to capture interest for the manufacture of electronics-enabled clothing. While much of the early effort was for novel items of fashion, including programmable LED lighting in apparel items (Figure 6), it was quickly recognized that the technology could be applied to the integration of electronic circuits for data processing in wearable applications. Again, interest has been shown in remote health monitoring for those who are in ill health and less mobile.

Standards for Circuits: A Necessary Glue

Over the years I have often been heard to refer to standards as a sort of “industrial strength glue” in that, collectively, industrial standards serve to help glue industries together and make them stronger. The IPC, through the dedication of its industry volunteer members,

BENDING THE POSSIBILITIES

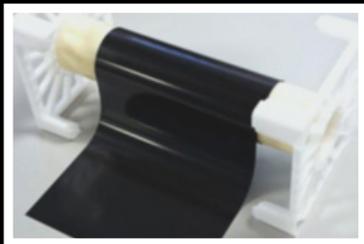


BY TAIYO

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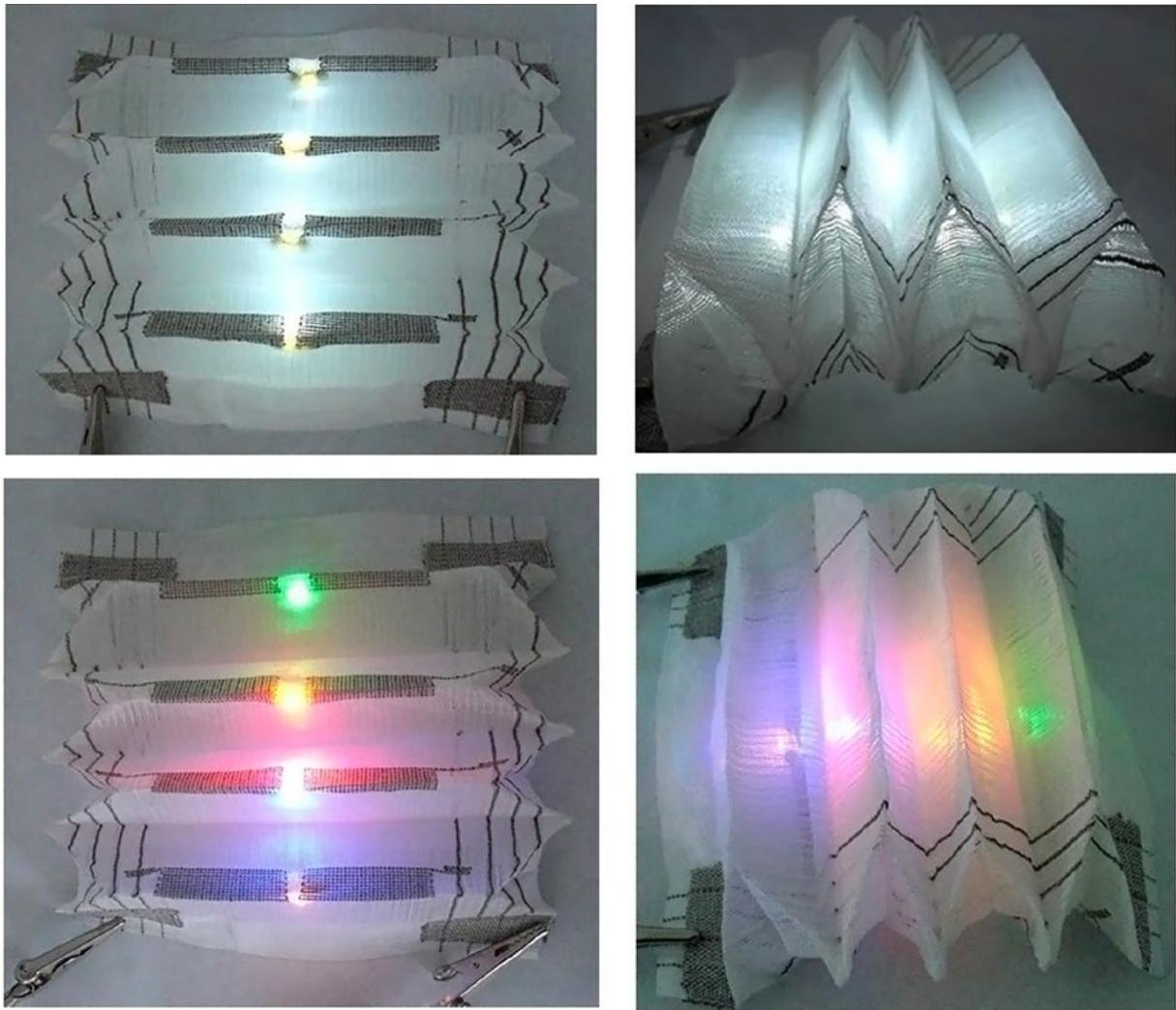


Figure 6: LEDs and supporting interconnections are woven into fabric as a demonstration of e-textile technology potential. (Source: Priti Veja's 2015 thesis, Brunel University London⁵)

has been nurturing, producing, and publishing industry standards for electronic interconnection technologies for seven decades. The standards include materials and end-product requirements as well as guidelines for design and testing of printed circuits, both rigid and flexible, for decades. As evidence of their ongoing dedication to the industry and to keep pace with both ongoing and recent developments such as those described here, the IPC has taken point in the development of standards for the nascent arena of e-textiles just described. In October 2019, the IPC's E-Textiles subcommittee completed its work on IPC-8921, "Requirements for Woven and Knitted Electronic Textiles (E-Textiles) Integrated with

Conductive Fibers, Conductive Yarns and/or Wires." It is the IPC's first international standard for e-textiles, setting the groundwork for other e-textiles standards activities in progress.

Summary

This brief overview of wearable electronics has hopefully provided an appreciation of this branch of electronics technology that we might all agree is both very old and very new. The work of the IPC, as well as NextFlex and its partners and members—founded to promote flex hybrid electronics through its demonstration projects, facilities, and awareness programs—has done much to inspire new and current generations of designers to appreciate

the immeasurable past and future benefits of flexible circuit technology. The future has just begun. **FLEX007**

I would like to express my gratitude to Shelly Stein for her invaluable assistance in researching, vetting and editing the content of this month's column.

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Joe Fjelstad is founder and CEO of Verdant Electronics and an international authority and innovator in the field of electronic interconnection and packaging technologies with more than 185

patents issued or pending. To read past columns or contact Fjelstad, [click here](#). Download your free copy of Fjelstad's book *Flexible Circuit Technology, 4th Edition*, and watch his in-depth workshop series "Flexible Circuit Technology."

Fresh PCB Concepts

The Right Board for the Flex Job



by **Nicholas Marks**

We say we like the board that is the best fit for the job, but what does the right board for your job specifically look like? In this column, I will review the benefits and design types of flexible PCBs.

What is a flex PCB? A flex board is defined as a bendable board with one or more conductive layers. There are different types of flex boards to fit any situation you may have. IPC defines them in five types, all are different constructions. To put it shortly these constructions are as follows: one layer of flex, double sided, multilayer flex, multilayer rigid-flex, and double or multilayer flex without electrically connected layers. Flex isn't too old of a concept considering the history of PCBs. When first introduced these were pretty rare, however, recently the need for them has increased significantly due to the necessity to fit everything into a small package. These types of PCBs bring a number of benefits where rigid PCBs just won't cut it.

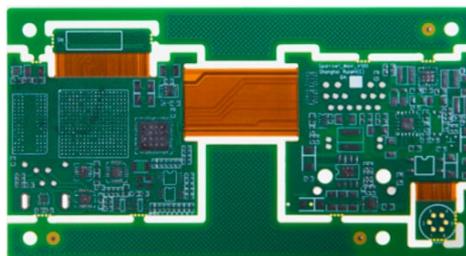
With the right design a flex can offer cost savings on your

assemblies, save space, and cut the weight of your design. Flex are very lightweight PCBs and often very thin as well. Along with specialized FCCL material, this will allow a bend in our circuit. This bend allows us to build and assemble in an extra dimension. These are just some of the benefits that can be reaped from introducing a flex into your system. Flex also allows for a more cost-effective, robust, and reliable connector instead of using wires and cables, which can lead to less failures during and after assembly.

Recently a customer reached out for some help on a wearable sensor product. This design was originally done with a rigid board, however they were looking to move to a flex circuit. With the flex as opposed to the rigid board in this situation, they could inevitably increase the form fit and function. Since this was a wearable device, weight and fit make a world of difference. Lowering the weight and

increasing the number of axes, we can build in yields a better, lighter-weight and overall, more natural fit than any rigid assembly could provide.

To read this entire column, [click here](#).





Flex007 Highlights



Flexible Thinking: Flexible Circuits or Flexible Electronics? ▶

The term “flexible circuit” has been ensconced and accepted in electronic interconnection technology lexicon for several decades. In broad brush strokes, the term has embraced every type of printed circuit produced on flexible base materials, regardless of the nature of the conductors used; metals, such as copper; or conductive inks, such as silver or other conductive particle filled polymers. The latter type of truly printed circuits, have, for many years, been referred to as “polymer thick film” circuits.

Compeq Reports 27% Jump in January Sales ▶

Compeq Manufacturing Co. Ltd, a Taiwan-based manufacturer of HDI, rigid-flex PCBs, and flex PCBs, has reported unaudited net sales of NT\$6.398 billion (\$229.52 million at \$1:NT\$27.88) for January 2022, up by 27% year-on-year, but down by 7.4% from the previous month (December: NT\$6.9 billion).

CIMS Launches Capricorn, Next Generation AVI Solution ▶

CIMS is launching its next generation AVI solution for IC Substrates based on a brand-new platform: Capricorn.

NextFlex Launches \$11.5 Million Funding Round for Flexible Hybrid Electronics Innovations ▶

NextFlex, America’s Flexible Hybrid Electronics (FHE) Manufacturing Institute, released Project Call 7.0 (PC 7.0), the latest call for proposals that seek to fund projects that further

the development and adoption of FHE while addressing key challenges in advanced manufacturing while supporting Department of Defense priorities.

Flexible Hybrid Electronics Design: Reducing Time to Market ▶

Emerging innovations in the flexible hybrid electronics (FHE) domain are enabling new applications across multiple industries due to their highly flexible structures and additive manufacturing processes. The smaller form factor, lighter weight, and conformal capabilities are ideal for IoT edge devices in health and fitness monitoring, military asset identification and tracking, automotive displays and sensors, aerospace radar, and soft robotics. Significant industry research led by NextFlex is optimizing the processes from design through manufacture for FHE products.

Compeq February Revenue Soars 32% ▶

Taiwan-based Compeq Manufacturing Co. Ltd has reported unaudited net sales of NT\$5.06 billion (\$178.5 million at \$1:NT\$28.35) for February 2022, up by 31.7% year-on-year, but down by 20.9% from the previous month (January: NT\$6.39 billion).

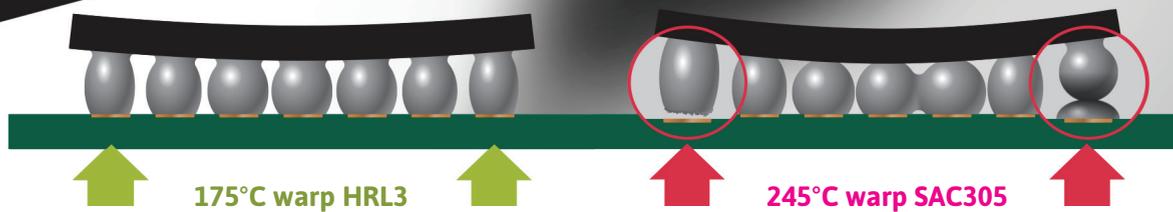
Taiflex Posts Lower February Sales ▶

Taiflex Scientific Co. Ltd, a Taiwan-based manufacturer of flexible printed circuit materials such as flexible copper clad laminates (CCLs) and coverlays, has announced consolidated revenue of NT\$567 million (\$20 million at \$1:NT\$28.35) for February, down by 29% from the previous month and lower by 16.6% year-on-year (YoY).

ALPHA® OM-565 HRL3 Solder Paste

Low Temperature, High Reliability

- **Enhanced** mechanical reliability over traditional SnBi solder pastes
- **Superior** wettability minimizing warpage induced defects
- **Enabling** peak reflow temperature of 175°C
- **Increases** energy efficiency and cost savings



Minimize Warpage Induced Defects to Maximize Assembly Yield.

www.macdermidalpha.com



PCB Talk: SAP—Changing the Way You Look at PCB Design

Which side of these competing aphorisms do you most resonate with: “The only thing constant is change” or “The more things change, the more they stay the same”? I can build a case behind both when looking at these through the lens of someone working in the printed circuit board industry.



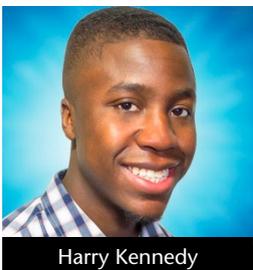
Connect the Dots: The PCB Design Secret Sauce for RF Applications



Design and manufacture of PCBs for radio frequency (RF) technology is a unique animal. RF had been considered a niche, thought of only in terms of television broadcasts, commercial airline phones, and military radar systems. Now, light industrial and consumer applications are just the tip of the RF iceberg.

Designers Notebook: Design for Test, Part 2

Current generations for PCB designs have increased in complexity. The product developer and assembly service provider, whether in-house or outsourced, must consider manufacturing efficiency, throughput, and process yield.



Harry Kennedy



Sarmad Khemmor

AltiumLive 2022: Left-Shifting Modeling and Simulation

Harry Kennedy and Sarmad Khemmor of Altair recently spoke with Andy Shaughnessy about their AltiumLive presentations, which are now available online. They discuss the need for modeling, simulation, and verification in PCB design, and why these actions should be performed as early in the design process as possible.

Digital Transformation: Leveraging Model-based Engineering to Manage Risk



Companies at the forefront of electronic systems engineering understand this basic tenet of

risk analysis. Technology has not only increased the complexity of individual domains, but also the number of domains. And these complexities introduce a lot more risk of failures.

Beyond Design: The Coupling Coup

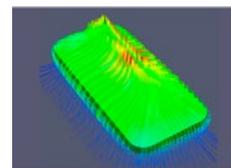
Coupling on a multilayer PCB may be a good or bad thing. On one hand, close coupling of signal traces to reference planes and differential pair signals is the best way to prevent common mode radiation and to mitigate electromagnetic (EM) emission. But on the other, close coupling of unrelated signal traces can bring us grief with unintentional crosstalk caused by overlapping EM fields.

RF and Microwave: No Black Magic

I caught up with Ben Jordan after his class on RF and microwave at IPC APEX EXPO. Ben, an electrical engineer, explained how sitting through previous classes on this topic led to him developing his own class. “I wanted to bridge the gap,” he says, “with a class that makes the material approachable and teaches the intuitive nature of fields and waves and how they work in circuit boards.”

All Systems Go!: Find and Fix Thermal PCB Problems Sooner Than Later

In an earlier column titled “Bridging the Gap Between Design and Analysis with In-Design Analysis,” Brad Griffin discussed how the “shift left” that’s happening with electronic design means it is no longer sufficient for signal integrity (SI) and power integrity (PI) analysis to be performed in isolation.



Lightning Speed Laminates: Prepreg Choices for Millimeter-wave PCB Applications

There are obviously a lot of prepreg choices in the PCB industry. In the past, it was common for the choice of prepreg to be dominated by PCB fabrication concerns.

Target Condition: Livin’ in a PCB Stakeholder’s Paradise

A few months ago, I was offered a unique opportunity to serve as the AltiumLive Connect 2022 show host for the virtual event during the last full week of January. It started with an idea I had during a meeting with Altium last October, to create a musical promo for the annual summit. I love to write songs and I’ve written a few which have been used commercially. But for a technical electronics trade show, I knew that I would have to reach far outside my normal styles of composition.



For the latest news and information, visit PCBDesign007.com

Career Opportunities



Is your team growing?

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For just \$750, your 200-word, full-column ad will appear in the Career Opportunities section of all three of our monthly magazines, reaching circuit board designers, fabricators, assemblers, OEMs, suppliers and the academic community.

In addition, your ad will:

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GOOD FOR THE INDUSTRY



Career Opportunities



Printed Circuit Board (PCB)

Layout Designer (Designer-Drafter 3/4)

Los Alamos National Laboratory
Los Alamos, New Mexico

Los Alamos National Laboratory (LANL) is a multidisciplinary research institution engaged in science and engineering on behalf of national security. The ISR-5 Space Instrument Realization Group is currently seeking an entry level Printed Circuit Board (PCB) Layout Designer. You'll design and develop rigid and flexible PCBs directly supporting the design, prototyping and manufacturing of innovative space satellites for a variety of important scientific and national security missions.

Requirements:

- 3-5 years relevant experience
- Associate's in engineering or technical field (or an additional 2 years related experience)
- Working knowledge of PCB fabrication or electronics assembly requirements
- Familiarity with PCB layout CAD design tools
- Demonstrated commitment to safety, security environment and quality

Desired Qualifications:

- Basic experience using software tools to produce models, drawings, layouts and sketches of components/systems
- Familiarity with PCB design concepts, IPC design and performance standards
- Experience using PCB design software, such as Eagle, Altium or Mentor Graphics

Apply now: [lanl.jobs, search IRC102937lanl.gov/careers](https://lanl.jobs/search/IRC102937lanl.gov/careers)

Los Alamos National Laboratory is an EO employer – Veterans/Disabled and other protected categories. Qualified applicants will receive consideration for employment without regard to race, color, religion, sex, national origin, sexual orientation, gender identity, disability or protected veteran status.

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Printed Circuit Board (PCB)

Technologist (Engineering Technologist 1 / 2)

Los Alamos National Laboratory
Los Alamos, New Mexico

Los Alamos National Laboratory (LANL) is a multidisciplinary research institution focused on solving national security challenges. The Intelligence and Space Research Division is seeking an experienced Printed Circuit Board (PCB) Layout Technologist to directly support the design, prototyping and manufacturing of innovative space instruments for important science and national security missions.

Requirements:

- 2 -5 years related experience
- Bachelor's in engineering technology, science or math (or an additional 8 years of related experience)
- Advanced knowledge of PCB layout CAD design tools/current best practices
- Ability to determine technical requirements/objectives for new PCB designs
- Ability to identify problems, create solutions and effectively navigate institutional systems

Desired Qualifications:

- Experience using Siemens (Mentor Graphics) Xpedition PB design flow software
- Experience interpreting and applying IPC-6012 and IPC-6013 qualification and performance standards
- Experience designing high-speed, controlled-impedance PCBs for digital and RF applications
- Experience designing PCBs for space flight applications

Apply now: [lanl.jobs, search IRC103475](https://lanl.jobs/search/IRC103475)

Los Alamos National Laboratory is an EO employer – Veterans/Disabled and other protected categories. Qualified applicants will receive consideration for employment without regard to race, color, religion, sex, national origin, sexual orientation, gender identity, disability or protected veteran status.

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Career Opportunities



Global Account Manager, e-Mobility & Infrastructure

**Location:
AZ, CA, TX (remote)**

Job Summary:

The Global Account Manager, e-Mobility & Infrastructure is a key position for the sales organization, serving as Indium Corporation's lead sales contact responsible for developing targeted accounts in the e-Mobility and related infrastructure space.

Responsibilities will include:

- sourcing for new global business opportunities
- implementing effective sales strategies
- interfacing with customers' senior management
- execution of action plans through the regional teams
- interaction with internal customers (R&D; Inside Sales; Technical Support; Logistics; Product Management; Operations; Engineering; Quality; etc.) resulting in evaluation, qualification, specification, and maximum customer share for designated customers
- providing risk assessment of the business to senior management

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Director of Operations State College, PA

Chemcut Corp., a world leader in wet processing equipment for the manufacture of printed circuit boards and chemical etching of various metals, is seeking a Director of Operations.

Objectives of the Role:

- Collaborate with the CEO in setting and driving organizational vision, operational strategy, and hiring needs.
- Oversee manufacturing operations and employee productivity, building a highly inclusive culture ensuring team members thrive and organizational outcomes are met.
- Directly oversee manufacturing operations, production planning, purchasing, maintenance & customer service (product support) and partner with the CEO and controller on sales management to budget for sufficient investment capital to achieve growth targets.
- Aggressively manage capital investment and expenses to ensure the company achieves investor targets relative to growth and profitability.

Qualifications:

- Bachelor's degree in mechanical, electrical, or related fields
- 5+ years' experience in leadership positions
- Leadership skills, with steadfast resolve and personal integrity
- Understanding of advanced business planning and regulatory issues
- A solid grasp of data analysis and performance metrics
- Ability to diagnose problems quickly and have foresight into potential issues

Preferred Qualifications:

- Master's degree in business or related field
- International business experience

To apply, please submit a cover letter
and resume to hr@chemcut.net

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Career Opportunities



ventec
INTERNATIONAL GROUP
騰輝電子

Operations Supervisor Elk Grove Village IL, USA

As operations supervisor at Ventec USA LLC, you will have a hands-on and quality-driven approach to coordinating and overseeing the operations in Elk Grove Village, Illinois. You will plan, organize, and implement the day-to-day warehouse activities to ensure customer expectations are met. Tasks will include planning, implementing performance improvement measures, procuring materials and resources, and assuring compliance to the Quality Management System. You will be a mentor to team members, find ways to maintain and improve the highest quality of customer service, and implement best practices across all levels to help the company remain compliant, efficient, and profitable.

Skills and abilities required:

- Proven experience as operations supervisor or similar role
- Knowledge of organizational effectiveness and warehouse management
- Experience with ISO9001 or similar QMS
- Experience in budgeting and forecasting/familiarity with business and financial principles
- Excellent leadership ability and communication skills (English)
- Outstanding organizational skills
- Qualification in distribution, logistics, transportation, or business studies is preferential

What's on offer:

- Excellent salary & benefits commensurate with experience

This is a fantastic opportunity to become part of a successful brand and leading team with excellent benefits. Please forward your resume to HR@Ventec-usa.com and mention (Operations Supervisor) in the subject line.

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ventec
INTERNATIONAL GROUP
騰輝電子

European Product Manager Taiyo Inks, Germany

We are looking for a European product manager to serve as the primary point of contact for product technical sales activities specifically for Taiyo Inks in Europe.

Duties include:

- Business development & sales growth in Europe
- Subject matter expert for Taiyo ink solutions
- Frequent travel to targeted strategic customers/OEMs in Europe
- Technical support to customers to solve application issues
- Liaising with operational and supply chain teams to support customer service

Skills and abilities required:

- Extensive sales, product management, product application experience
- European citizenship (or authorization to work in Europe/Germany)
- Fluency in English language (spoken & written)
- Good written & verbal communications skills
- Printed circuit board industry experience an advantage
- Ability to work well both independently and as part of a team
- Good user knowledge of common Microsoft Office programs
- Full driving license essential

What's on offer:

- Salary & sales commission--competitive and commensurate with experience
- Pension and health insurance following satisfactory probation
- Company car or car allowance

This is a fantastic opportunity to become part of a successful brand and leading team with excellent benefits. Please forward your resume to jobs@ventec-europe.com.

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Career Opportunities



Flexible Circuit Technologies is a premier global supplier providing design, prototyping and production of flexible circuits, rigid flex circuits, flexible heaters, and membrane switches.

Application Engineer/ Program Management

Responsibilities

- Gain understanding for customer and specific project requirements
- Review customer files/drawings, analyze technical, application, stackup, material, and mechanical requirements; develop cost-effective designs that meet requirements
- Quote and follow up to secure business
- Work with CAD: finalize files, attain customer approval prior to build
- Track timeline and provide customers with updates
- Follow up on prototype, assist with design changes if needed, push forward to production
- Work with customer as the lead technician/program manager or as part of FCT team working with an assigned program manager
- Help customer understand FCT's assembly, testing, and box build services/support
- Understand manufacturing and build process for flexible and rigid-flex circuits

Qualifications

- Demonstrated experience: PCB/FPCB/rigid-flex designer including expertise in design rules, IPC
- Demonstrated success in attaining business
- Ability to work in fast-paced environment, on broad range of projects, while maintaining a sense of urgency
- Ability to work as a team player
- Excellent written and verbal communication skills
- Must be willing to travel for sales support activities, customer program support and more.

FCT offers a competitive salary, bonus program, and benefits package. Preferred location Minneapolis, MN area. www.flexiblecircuit.com

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Electrical Engineer/PCB/CAD Design, BOM Component & Quality Support

Responsibilities

- Learn the properties, applications, advantages/disadvantages of flex circuits
- Learn the intricacies of flex circuit layout best practices
- Learn IPC guidelines: Flex circuits/assemblies
- Create flexible PCB designs/files to meet engineering/customer requirements
- Review customer prints and Gerber files to ensure they meet manufacturing and IPC requirements
- Review mechanical designs for mfg, including circuit and assembly requirements, BOM/component needs and help to identify alternate components if needed
- Prepare and document changes to customer prints/files. Work with app engrs, customers and mfg. engrs. to finalize and optimize designs for manufacturing
- Work with quality manager to learn quality systems, requirements, and support manager with assistance

Qualifications

- Electrical Engineering degree with 2+ years of CAD/PCB design experience
- IPC CID or CID+ certification or desire to obtain
- Knowledge of flexible PCB materials, properties, or willingness to learn
- Experience with CAD software: Altium or other
- Knowledge of IPC standards for PCB industry, or willingness to learn
- Microsoft Office products

FCT offers a competitive salary, bonus program, and benefits package. Preferred location Minneapolis, MN area. www.flexiblecircuit.com

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Career Opportunities



R&D Scientist III Orange, CT

Job Description: The scientist will be a leader in technology for plating chemistry development, electrolytes, and additives. The position is hands-on, where the ideal candidate will enjoy creating and testing new aqueous plating processes and materials to meet the most demanding semiconductor applications related to Wafer-Level Packaging and Damascene. The qualified candidate will work as part of the R&D team while interacting with scientists, product management, and application engineers to commercialize new products for the advanced electronic solution business.

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Technical Marketing Specialist Waterbury, CT

This position provides information from the product team to the marketing communications team. It is a multifunctional role that requires some experience within electronics manufacturing supply chain or knowledge of how electronic devices are manufactured, specifically PCBs, semiconductors, and the chemical processes utilized therein. The primary function of this role is to help in the generation of product marketing collateral, but also includes assisting in tradeshow content development, advertising, and launches.

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Regional Manager Midwest Region

General Summary: Manages sales of the company's products and services, Electronics and Industrial, within the States of IL, IN & MI. Reports directly to Americas Manager. Collaborates with the Americas Manager to ensure consistent, profitable growth in sales revenues through positive planning, deployment and management of sales reps. Identifies objectives, strategies and action plans to improve short- and long-term sales and earnings for all product lines.

DETAILS OF FUNCTION:

- Develops and maintains strategic partner relationships
- Manages and develops sales reps:
 - Reviews progress of sales performance
 - Provides quarterly results assessments of sales reps' performance
 - Works with sales reps to identify and contact decision-makers
 - Setting growth targets for sales reps
 - Educates sales reps by conducting programs/ seminars in the needed areas of knowledge
- Collects customer feedback and market research (products and competitors)
- Coordinates with other company departments to provide superior customer service

QUALIFICATIONS:

- 5-7+ years of related experience in the manufacturing sector or equivalent combination of formal education and experience
- Excellent oral and written communication skills
- Business-to-business sales experience a plus
- Good working knowledge of Microsoft Office Suite and common smart phone apps
- Valid driver's license
- 75-80% regional travel required

To apply, please submit a COVER LETTER and RESUME to: Fernando Rueda, Americas Manager

fernando_rueda@kyzen.com

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Career Opportunities



American Standard Circuits

Creative Innovations In Flex, Digital & Microwave Circuits

Wet Process Engineer

ASC, the largest independent PCB manufacturer in the Midwest, is looking to expand our manufacturing controls and capabilities within our Process Engineering department. The person selected will be responsible for the process design, setup, operating parameters, and maintenance of three key areas—imaging, plating, etching—within the facility. This is an engineering function. No management of personnel required.

Essential Responsibilities

Qualified candidates must be able to organize their own functions to match the goals of the company.

Responsible for:

- panel preparation, dry film lamination, exposure, development and the processes, equipment setup and maintenance programs
- automated (PAL line) electrolytic copper plating process and the equipment setup and maintenance programs
- both the cupric (acid) etching and the ammoniacal (alkaline) etching processes and the equipment setups and maintenance programs

Ability to:

- perform basic lab analysis and troubleshooting as required
- use measurement and analytical equipment as necessary
- work alongside managers, department supervisors and operators to cooperatively resolve issues
- effectively problem-solve
- manage multiple projects concurrently
- read and speak English
- communicate effectively/interface at every level of the organization

Organizational Relationships

Reports to the Technical Director.

Qualifications

Degree in Engineering (BChE or I.E. preferred). Equivalent work experience considered. High school diploma required. Literate and functional with most common business software systems MS Office, Excel, Word, PowerPoint are required. Microsoft Access and basics of statistics and SPC a plus.

Physical Demands

Exertion of up to 50 lbs. of force occasionally may be required. Good manual dexterity for the use of common office equipment and hand tools.

- Ability to stand for long periods.

Work Environment

This position is in a manufacturing setting with exposure to noise, dirt, and chemicals.

Click on 'apply now' button below to send in your application.

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Career Opportunities



MACHINES FOR PRINTED CIRCUIT BOARDS

Field Service Engineer

Location: West Coast, Midwest

Pluritec North America, Ltd., an innovative leader in drilling, routing, and automated inspection in the printed circuit board industry, is seeking a full-time field service engineer.

This individual will support service for North America in printed circuit board drill/routing and x-ray inspection equipment.

Duties included: Installation, training, maintenance, and repair. Must be able to troubleshoot electrical and mechanical issues in the field as well as calibrate products, perform modifications and retrofits. Diagnose effectively with customer via telephone support. Assist in optimization of machine operations.

A technical degree is preferred, along with strong verbal and written communication skills. Read and interpret schematics, collect data, write technical reports.

Valid driver's license is required, as well as a passport, and major credit card for travel.

Must be able to travel extensively.

[apply now](#)



SMT Field Technician Hatboro, PA

Manncorp, a leader in the electronics assembly industry, is looking for an additional SMT Field Technician to join our existing East Coast team and install and support our wide array of SMT equipment.

Duties and Responsibilities:

- Manage on-site equipment installation and customer training
- Provide post-installation service and support, including troubleshooting and diagnosing technical problems by phone, email, or on-site visit
- Assist with demonstrations of equipment to potential customers
- Build and maintain positive relationships with customers
- Participate in the ongoing development and improvement of both our machines and the customer experience we offer

Requirements and Qualifications:

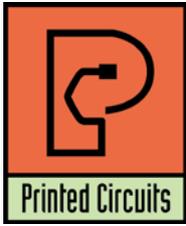
- Prior experience with SMT equipment, or equivalent technical degree
- Proven strong mechanical and electrical troubleshooting skills
- Proficiency in reading and verifying electrical, pneumatic, and mechanical schematics/drawings
- Travel and overnight stays
- Ability to arrange and schedule service trips

We Offer:

- Health and dental insurance
- Retirement fund matching
- Continuing training as the industry develops

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Career Opportunities



Printed Circuits, a fast-growing printed circuit board fabricator, offers:

- Excellent opportunities for advancement and growth
- Dynamic manufacturing environment
- Excellent health, dental and other benefits
- Annual profit-sharing plan
- Signing bonus
- Additional incentives at the leadership level
- Clean facility with state-of-the-art manufacturing equipment
- Highly collaborative corporate and manufacturing culture that values employee contributions

Laminator Technician

Nature of Duties/Responsibilities

- Layup cover lay
- Layup rigid flex
- Layup multilayer/CU core boards
- Oxide treat/cobra treatment of all layers/CU cores
- Shear flex layer edges
- Rout of machine panel edges and buff
- Remove oxide/cobra treatment (strip panels)
- Serialize panels
- Pre-tac Kapton windows on flex layers (bikini process)
- Layup Kapton bonds
- Prep materials: B-stage, Kapton, release sheet
- Breakdown: flex layers, and caps
- Power scrub: boards, layers, and caps
- Laminate insulators, stiffeners, and heatsinks
- Plasma cleans and dry flex layers B-stage (Dry)
- Booking layers and materials, ready for lamination process
- Other duties as deemed necessary by supervisor

Education/Experience

- High school diploma or GED
- Must be a team player
- Must demonstrate the ability to read and write English and complete simple mathematical equations
- Must be able to follow strict policy and OSHA guidelines
- Must be able to lift 50 lbs
- Must have attention to detail

Wet Process/Plating Technician

Position is 3rd shift (11:00PM to 7:30AM, Sunday through Friday)

Purpose

To carry out departmental activities which result in producing quality product that conforms to customer requirements. To operate and maintain a safe working environment.

Nature of Duties/Responsibilities

- Load and unload electroplating equipment
- Fasten circuit boards to racks and cathode bars
- Immerse work pieces in series of cleaning, plating and rinsing tanks, following timed cycles manually or using hoists
- Carry work pieces between departments through electroplating processes
- Set temperature and maintains proper liquid levels in the plating tanks
- Remove work pieces from racks, and examine work pieces for plating defects, such as nodules, thin plating or burned plating
- Place work pieces on racks to be moved to next operation

- Check completed boards
- Drain solutions from and clean and refill tanks; fill anode baskets as needed
- Remove buildup of plating metal from racks using chemical bath

Education and Experience

- High school diploma or GED required
- Good organizational skills and the ability to follow instructions
- Ability to maintain a regular and reliable attendance record
- Must be able to work independently and learn quickly
- Organized, self-motivated, and action-oriented, with the ability to adapt quickly to new challenges/opportunities
- Prior plating experience a plus

Production Scheduler

Main Responsibilities

- Development and deployment of a level-loaded production plan
- Establish manufacturing plan which results in "best possible" use of resources to maximize asset utilization
- Analyze production capacity of manufacturing processes, equipment and human resource requirements needed to produce required products
- Plan operation manufacturing sequences in weekly time segments utilizing production labor standards
- Maintain, align, and communicate regularly with internal suppliers/customers and customer service on key order metrics as per their requirements
- Frequently compare current and anticipated orders with available inventory and creates replenishment plan
- Maintain master distribution schedule for the assigned facility, revise as needed and alert appropriate staff of schedule changes or delays
- Participate in periodic forecasting meetings
- Lead or participate in planning and status meetings with production, shipping, purchasing, customer service and/or other related departments
- Follow all good manufacturing practices (GMPs)
- Answer company communications, fax, copy and file paperwork

Education and Experience

- High school diploma or GED
- Experience in manufacturing preferred/3 years in scheduling
- Resourceful and good problem-solving skills
- Ability to make high pressure decisions
- Excellent written and verbal communication skills
- Strong computer skills including ERP, Excel, Word, MS Office
- Detailed and meticulous with good organizational skills
- Must be articulate, tactful and professional at all times
- Self-motivated

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Career Opportunities

INSULECTRO

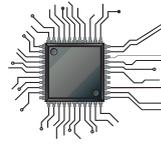


Are You Our Next Superstar?!

Insulectro, the largest national distributor of printed circuit board materials, is looking to add superstars to our dynamic technical and sales teams. We are always looking for good talent to enhance our service level to our customers and drive our purpose to enable our customers build better boards faster. Our nationwide network provides many opportunities for a rewarding career within our company.

We are looking for talent with solid background in the PCB or PE industry and proven sales experience with a drive and attitude that match our company culture. This is a great opportunity to join an industry leader in the PCB and PE world and work with a terrific team driven to be vital in the design and manufacture of future circuits.

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MivaTek

Global

Field Service Technician

MivaTek Global is focused on providing a quality customer service experience to our current and future customers in the printed circuit board and microelectronic industries. We are looking for bright and talented people who share that mindset and are energized by hard work who are looking to be part of our continued growth.

Do you enjoy diagnosing machines and processes to determine how to solve our customers' challenges? Your 5 years working with direct imaging machinery, capital equipment, or PCBs will be leveraged as you support our customers in the field and from your home office. Each day is different, you may be:

- Installing a direct imaging machine
- Diagnosing customer issues from both your home office and customer site
- Upgrading a used machine
- Performing preventive maintenance
- Providing virtual and on-site training
- Updating documentation

Do you have 3 years' experience working with direct imaging or capital equipment? Enjoy travel? Want to make a difference to our customers? Send your resume to N.Hogan@MivaTek.Global for consideration.

More About Us

MivaTek Global is a distributor of Miva Technologies' imaging systems. We currently have 55 installations in the Americas and have machine installations in China, Singapore, Korea, and India.

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Career Opportunities



Rewarding Careers

Take advantage of the opportunities we are offering for careers with a growing test engineering firm. We currently have several openings at every stage of our operation.

The Test Connection, Inc. is a test engineering firm. We are family owned and operated with solid growth goals and strategies. We have an established workforce with seasoned professionals who are committed to meeting the demands of high-quality, low-cost and fast delivery.

TTCI is an Equal Opportunity Employer. We offer careers that include skills-based compensation. We are always looking for talented, experienced test engineers, test technicians, quote technicians, electronics interns, and front office staff to further our customer-oriented mission.

Associate Electronics Technician/Engineer (ATE-MD)

TTCI is adding electronics technician/engineer to our team for production test support.

- Candidates would operate the test systems and inspect circuit card assemblies (CCA) and will work under the direction of engineering staff, following established procedures to accomplish assigned tasks.
- Test, troubleshoot, repair, and modify developmental and production electronics.
- Working knowledge of theories of electronics, electrical circuitry, engineering mathematics, electronic and electrical testing desired.
- Advancement opportunities available.
- Must be a US citizen or resident.

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Test Engineer (TE-MD)

In this role, you will specialize in the development of in-circuit test (ICT) sets for Keysight 3070 (formerly HP) and/or Teradyne (formerly GenRad) TestStation/228X test systems.

- Candidates must have at least three years of experience with in-circuit test equipment. A candidate would develop and debug our test systems and install in-circuit test sets remotely online or at customer's manufactur-

ing locations nationwide.

- Candidates would also help support production testing and implement Engineering Change Orders and program enhancements, library model generation, perform testing and failure analysis of assembled boards, and other related tasks.
- Some travel required and these positions are available in the Hunt Valley, Md., office.

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Sr. Test Engineer (STE-MD)

- Candidate would specialize in the development of in-circuit test (ICT) sets for Keysight 3070 (formerly Agilent & HP), Teradyne/GenRad, and Flying Probe test systems.
- Strong candidates will have more than five years of experience with in-circuit test equipment. Some experience with flying probe test equipment is preferred. A candidate would develop, and debug on our test systems and install in-circuit test sets remotely online or at customer's manufacturing locations nationwide.
- Proficient working knowledge of Flash/ISP programming, MAC Address and Boundary Scan required. The candidate would also help support production testing implementing Engineering Change Orders and program enhancements, library model generation, perform testing and failure analysis of assembled boards, and other related tasks. An understanding of stand-alone boundary scan and flying probe desired.
- Some travel required. Positions are available in the Hunt Valley, Md., office.

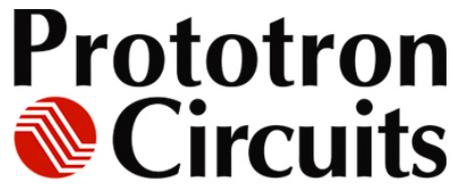
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Career Opportunities



Sales Representatives

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- Production quality quick-turn services in as little as 24 hours
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- MIL-PRF- 31032
- ITAR
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- Engineering consultation
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Call Dan Beaulieu at

207-649-0879

or email to

danbbeaulieu@aol.com

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U.S. CIRCUIT

Plating Supervisor

Escondido, California-based PCB fabricator U.S. Circuit is now hiring for the position of plating supervisor. Candidate must have a minimum of five years' experience working in a wet process environment. Must have good communication skills, bilingual is a plus. Must have working knowledge of a plating lab and hands-on experience running an electrolytic plating line. Responsibilities include, but are not limited to, scheduling work, enforcing safety rules, scheduling/maintaining equipment and maintenance of records.

Competitive benefits package.

Pay will be commensurate with experience.

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Career Opportunities



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Qualifications and skills

- A love of teaching and enthusiasm to help others learn
- Background in electronics manufacturing
- Soldering and/or electronics/cable assembly experience
- IPC certification a plus, but will certify the right candidate

Benefits

- Ability to operate from home. No required in-office schedule
- Flexible schedule. Control your own schedule
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- Training and certifications provided and maintained by EPTAC

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Will deliver technical presentations, conduct product demonstrations and benchmarks, and participate in the development of account sales strategies leading to market share gains.

- PCB design competency required
- BEE, MSEE preferred
- Prior experience with Signal Integrity, Power Integrity, EM & SPICE circuit analysis tools
- Experience with HyperLynx, Ansys, Keysight and/or Sigrity
- A minimum of 5 years' hands-on experience with EM Analysis & Simulation, printed circuit board design, engineering technology or similar field
- Moderate domestic travel required
- Possess passion to learn and perform at the cutting edge of technology
- Desire to broaden exposure to the business aspects of the technical design world
- Possess a demonstrated ability to build strong rapport and credibility with customer organizations while maintaining an internal network of contacts
- Enjoy contributing to the success of a phenomenal team

***Qualified applicants will not require employer-sponsored work authorization now or in the future for employment in the United States. Qualified Applicants must be legally authorized for employment in the United States.*

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Career Opportunities



Arlon EMD, located in Rancho Cucamonga, California, is currently interviewing candidates for open positions in:

- **Engineering**
- **Quality**
- **Various Manufacturing**

All interested candidates should contact Arlon's HR department at 909-987-9533 or email resumes to careers.ranch@arlonemd.com.

Arlon is a major manufacturer of specialty high-performance laminate and prepreg materials for use in a wide variety of printed circuit board applications. Arlon specializes in thermoset resin technology, including polyimide, high Tg multifunctional epoxy, and low loss thermoset laminate and prepreg systems. These resin systems are available on a variety of substrates, including woven glass and non-woven aramid. Typical applications for these materials include advanced commercial and military electronics such as avionics, semiconductor testing, heat sink bonding, High Density Interconnect (HDI) and microvia PCBs (i.e. in mobile communication products).

Our facility employs state of the art production equipment engineered to provide cost-effective and flexible manufacturing capacity allowing us to respond quickly to customer requirements while meeting the most stringent quality and tolerance demands. Our manufacturing site is ISO 9001: 2015 registered, and through rigorous quality control practices and commitment to continual improvement, we are dedicated to meeting and exceeding our customers' requirements.

For additional information please visit our website at www.arlonemd.com

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American Standard Circuits
Creative Innovations In Flex, Digital & Microwave Circuits

CAD/CAM Engineer

Summary of Functions

The CAD/CAM engineer is responsible for reviewing customer supplied data and drawings, performing design rule checks and creating manufacturing data, programs, and tools required for the manufacture of PCB.

Essential Duties and Responsibilities

- Import customer data into various CAM systems.
- Perform design rule checks and edit data to comply with manufacturing guidelines.
- Create array configurations, route, and test programs, panelization and output data for production use.
- Work with process engineers to evaluate and provide strategy for advanced processing as needed.
- Itemize and correspond to design issues with customers.
- Other duties as assigned.

Organizational Relationship

Reports to the engineering manager. Coordinates activities with all departments, especially manufacturing.

Qualifications

- A college degree or 5 years' experience is required. Good communication skills and the ability to work well with people is essential.
- Printed circuit board manufacturing knowledge.
- Experience using CAM tooling software, Orbotech GenFlex®.

Physical Demands

Ability to communicate verbally with management and coworkers is crucial. Regular use of the telephone and e-mail for communication is essential. Sitting for extended periods is common. Hearing and vision within normal ranges is helpful for normal conversations, to receive ordinary information and to prepare documents.

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Career Opportunities



APCT, Printed Circuit Board Solutions: Opportunities Await

APCT, a leading manufacturer of printed circuit boards, has experienced rapid growth over the past year and has multiple opportunities for highly skilled individuals looking to join a progressive and growing company. APCT is always eager to speak with professionals who understand the value of hard work, quality craftsmanship, and being part of a culture that not only serves the customer but one another.

APCT currently has opportunities in Santa Clara, CA; Orange County, CA; Anaheim, CA; Wallingford, CT; and Austin, TX. Positions available range from manufacturing to quality control, sales, and finance.

We invite you to read about APCT at APCT.com and encourage you to understand our core values of passion, commitment, and trust. If you can embrace these principles and what they entail, then you may be a great match to join our team! Peruse the opportunities by clicking the link below.

Thank you, and we look forward to hearing from you soon.

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IPC Instructor Longmont, CO; Phoenix, AZ; U.S.-based remote

*Independent contractor,
possible full-time employment*

Job Description

This position is responsible for delivering effective electronics manufacturing training, including IPC Certification, to students from the electronics manufacturing industry. IPC instructors primarily train and certify operators, inspectors, engineers, and other trainers to one of six IPC Certification Programs: IPC-A-600, IPC-A-610, IPC/WHMA-A-620, IPC J-STD-001, IPC 7711/7721, and IPC-6012.

IPC instructors will conduct training at one of our public training centers or will travel directly to the customer's facility. A candidate's close proximity to Longmont, CO, or Phoenix, AZ, is a plus. Several IPC Certification Courses can be taught remotely and require no travel.

Qualifications

Candidates must have a minimum of five years of electronics manufacturing experience. This experience can include printed circuit board fabrication, circuit board assembly, and/or wire and cable harness assembly. Soldering experience of through-hole and/or surface-mount components is highly preferred.

Candidate must have IPC training experience, either currently or in the past. A current and valid certified IPC trainer certificate holder is highly preferred.

Applicants must have the ability to work with little to no supervision and make appropriate and professional decisions.

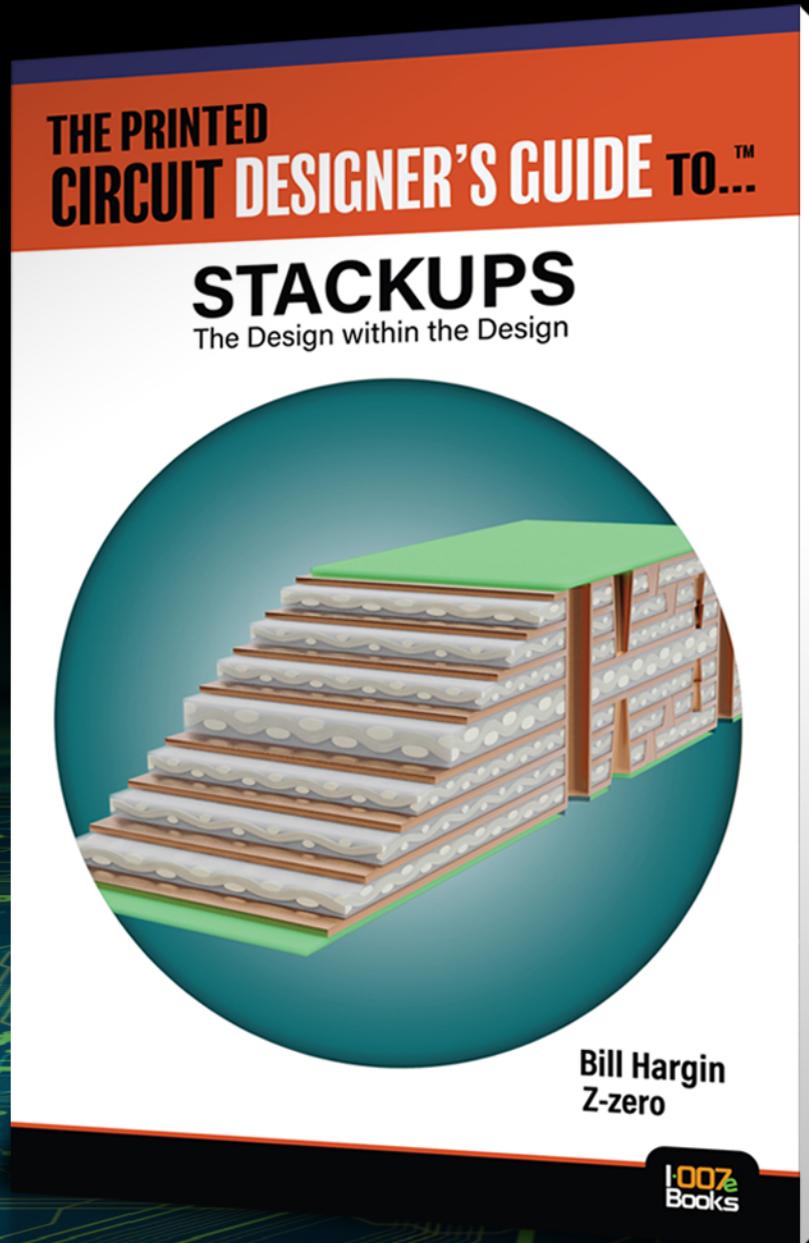
Send resumes to Sharon Montana-Beard at sharonm@blackfox.com.

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by Anaya Vardya, American Standard Circuits

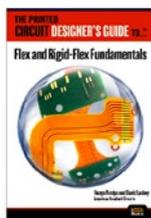
Beat the heat in your designs through thermal management design processes. This book serves as a desk reference on the most current techniques and methods from a PCB fabricator's perspective.



Thermal Management with Insulated Metal Substrates

by Didier Mauve and Ian Mayoh, Ventec International Group

Considering thermal issues in the earliest stages of the design process is critical. This book highlights the need to dissipate heat from electronic devices.



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by Anaya Vardya and David Lackey, American Standard Circuits

Flexible circuits are rapidly becoming a preferred interconnection technology for electronic products. By their intrinsic nature, FPCBs require a good deal more understanding and planning than their rigid PCB counterparts to be assured of first-pass success.

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