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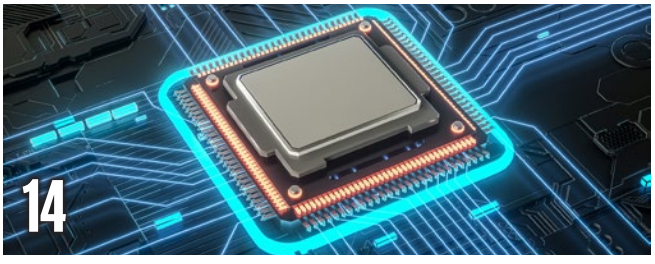
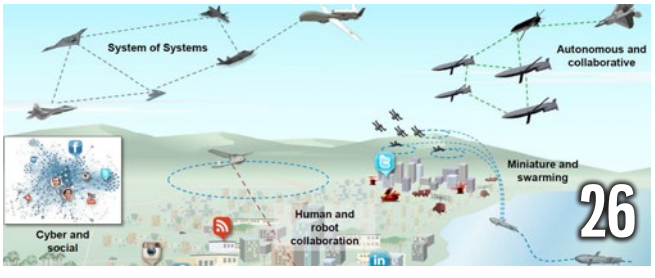
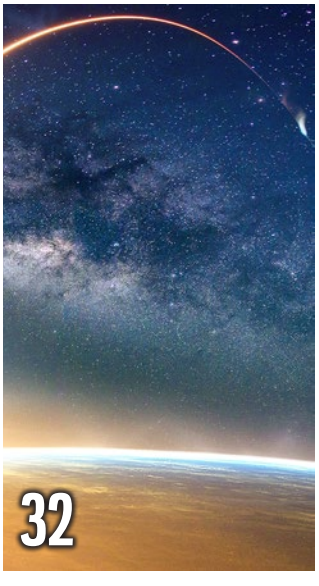
Technology Roadmaps

We reached out to a number of organizations doing roadmap work, as well as industry professionals volunteering during their personal time. What's clear is that creating a technology roadmap is not an easy task. This month (just in time for strategic planning), we talk roadmaps with those who make them and those who use them.







NK Technologies Trades Up with Manncorp

Significant Increase to Manufacturing Capacity - A Top Benefit

NK Technologies recently upgraded their manufacturing without a major economic expenditure. By taking advantage of Manncorp's Trade In, Trade Up Program, another MC389 Pick and Place was added to the production line used to assemble PCBAs for their current-sensing products, including the top-selling AG-series ground fault sensors (right). *Read more*

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Roadmaps: Driving Into the Future

Nolan's Notes

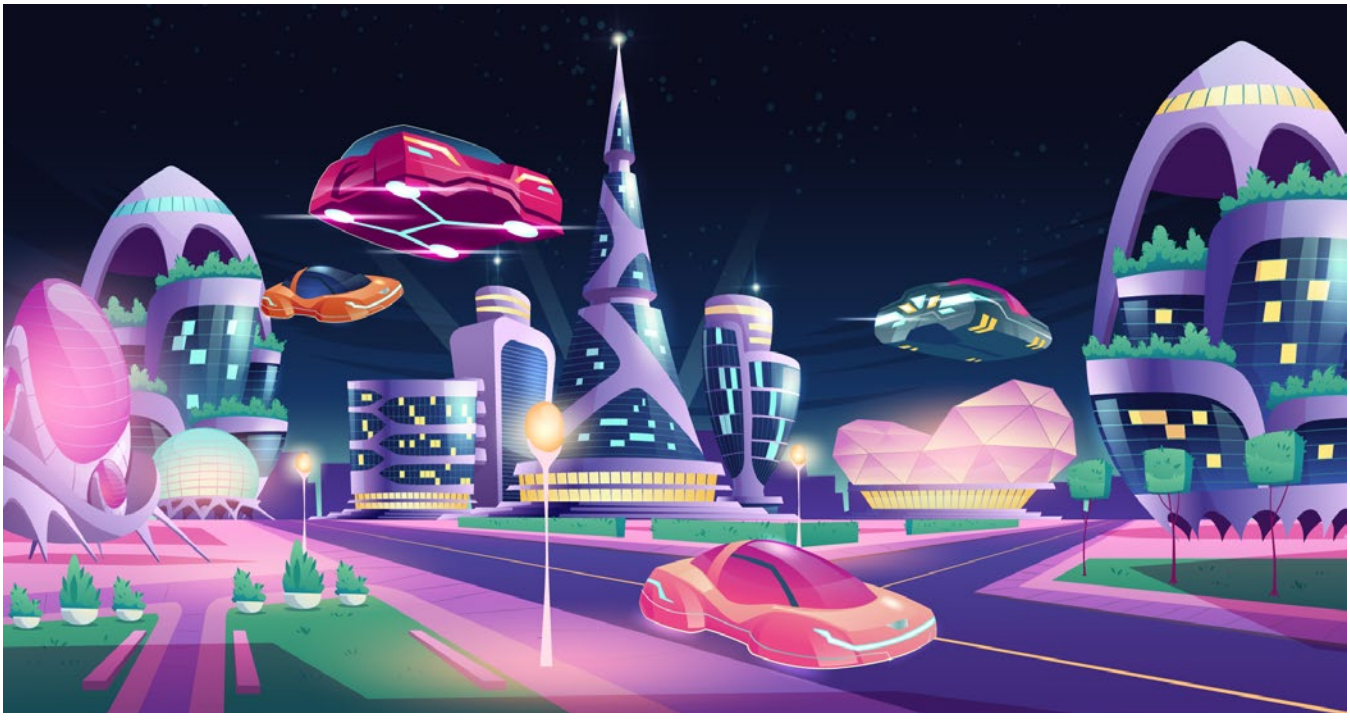
by Nolan Johnson, I-CONNECT007

Show anyone an image of travelers in the middle of nowhere, with a roadmap spread out across the hood of their car, and it's clear that they are lost. It's a universal symbol for a driver off course, consulting a map as a last resort. The implication is that roadmaps are only useful in an emergency.

This conclusion gives roadmaps a bad reputation. Roadmaps are navigational and predictive tools. Sure, they're also critical instruments when we find ourselves lost. But seasoned travelers and navigators use those maps to plan the journey, identify the milestones along the way, and know how to check that everything is still on course and on schedule, even when life throws obstacles in their path.

During a lecture I attended, Edward R. Tufte, a professor of statistical evidence and information design at Yale University [1], shared an observation that Napoleon Bonaparte was so very successful as a military strategist because he had a unique gift for reading maps. Tufte suggested (and I'm paraphrasing liberally, using 20-year-old memories) that Napoleon's ability to visualize the three-dimensional reality of the terrain based on the 2D topographical representation meant that he could march, shelter, provision, and position his armies more expertly than his opponents. According to Tufte, Napoleon was a master of reading roadmaps.

With the unanticipated obstacles and changes in our lives that we've all faced and endured in 2020, I've thought almost daily about roadmaps, keeping a journey on track, and Tufte's anecdotes about Napoleon. If you



had any doubt that you should navigate your business to a roadmap in the same way that Napoleon moved his troops, I'd wager that 2020 has changed your opinion. It's best not to wait until you're lost to check your maps.

iNEMI recently released its 2019 Roadmap, and then IEEE announced the publication of the Heterogeneous Integration Roadmap (HIR). These were followed by an announcement that iNEMI and IPC would be collaborating on roadmap work in the future. We realized that October was the right time to discuss roadmaps across all three magazines.

We reached out to a number of organizations doing roadmap work, as well as industry professionals volunteering during their personal time. It became quite clear that creating a technology roadmap is not an easy task. The key difference between a technology and a traditional roadmap is that traditional roadmaps report on what has already been measured while technology roadmaps gaze into the proverbial crystal ball.

Ultimately, much of our roadmapping discussion came from our conversations with IEEE HIR participants. We start with two excellent overview features from Rita Horner of Synopsys and IEEE's Paul Wesling. Rita provides a conceptual walking tour of future markets with heterogenous integration that was so comprehensive we've broken her presentation into installments for all three October magazines. Paul's conversation detailed the motivations and purpose for the HIR and gave us insight into the process for creating such a futurist document. Then, we dive into detailed discussions with multiple committee members, exploring the details of some key chapters for PCB fabrication and board assembly folks.

There is more gold to mine from the HIR, as well as iNEMI's roadmap and the roadmap work of others. If you aren't already choosing and tracking your route to the future to at least one roadmap, we hope that this month's issue will help you to see why you should.

Further Reading

I highly recommend Edward R. Tufte's books, published by Graphics Press: *The Visual Display of Quantitative Information* (1983); *Envisioning Information* (1990); and *Visual Explanations: Images and Quantities, Evidence and Narrative* (1997). **SMT007**

Nolan Johnson is managing editor of *SMT007 Magazine*. Nolan brings 30 years of career experience focused almost entirely on electronics design and manufacturing. To contact Johnson, click here.

Joint Industry Standard IPC J-STD-006: Electronic Solder Alloys, Part 2

SMT Prospects & Perspectives
by Dr. Jennie S. Hwang, CEO, H-TECHNOLOGIES GROUP

Requirements for Electronic-Grade Solder Alloys and Fluxed and Non-Fluxed Solid Solders for Electronic Soldering Applications

This writing is a follow-up to the Part 1 column published in January 2020 that addressed the questions that had been raised regarding the joint industry standard. The specific questions were related to the lead-free alloy designations (a naming system) adopted in IPC J-STD-006 and the alloy designations expressed in Table A-1 of the standard, entitled "Composition and Temperature Characteristics of Lead-Free Solder Alloys." At the time of the revision, Table 1-A was essentially intended to be dedicated to new and existing lead-free alloys.

As the mid-year IPC Standard Committees meeting (SummerCom) was canceled as a result of the COVID-19 pandemic, I am using this space to address the questions. I will primarily summarize relevant background information, the options for plausible naming systems, and the logic behind the decision to adopt the current naming system.

Background of Alloy Designation or Naming System

The revision J-STD-006B, published in January 2006, was the first industry-wide effort to include lead-free solder alloys in the J-STD-006 document. I was tasked to draft many parts of this revision, including Table A-1, by considering all available test data, opinions, comments, and historical and current information, as well as scientific principles and judgment.

We relied on several fundamental understandings and definitions:

1. A solder alloy is a mixture of elements in which the primary constituent is a metal.
2. The primary metal in an alloy is regarded as the base metal or the matrix.

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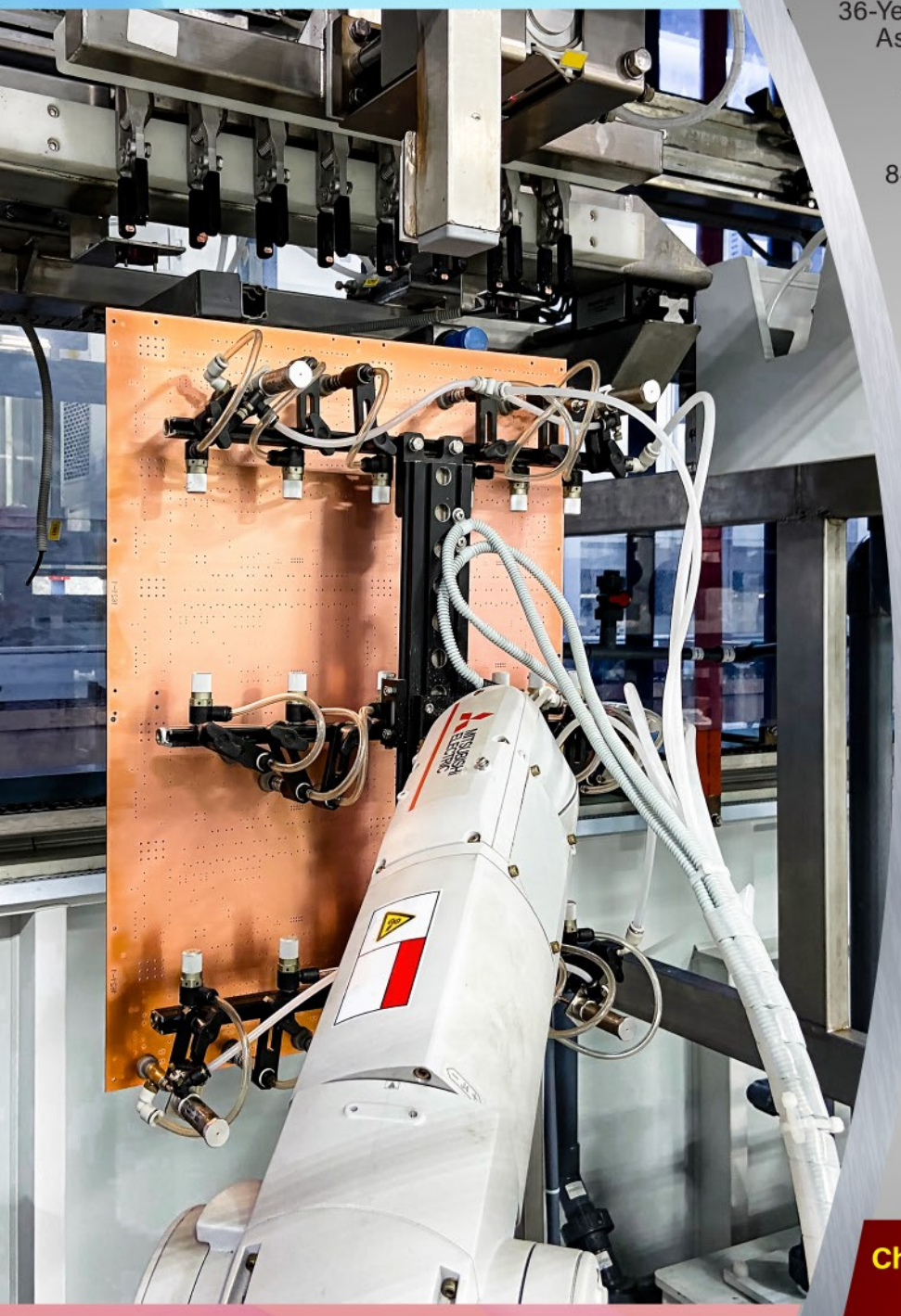

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3. Minor elemental constituents, regardless of metallurgical nature (e.g., solid solution, discrete particulate, doping element, intermetallic compound-forming element), are considered non-base metal.
4. Minor elemental constituents, regardless of metallurgical nature (e.g., solid solution, discrete particulate, doping element, intermetallic compound-forming element), are considered either alloying elements or doping elements.
5. Inevitably, lead-free solder alloys fall in the Sn-based system (at least for the mainstream electronic packaging and SMT assembly industry sector.)
6. Individual companies and entities may have initiated their own naming systems or trademarks at their discretion. It is the companies' prerogative, for commercial purposes, to name solder alloys at their choice, which are formed independently from the list of Table A-1.
7. If needed, military drawings can be accommodated by an additional group of designations as a subset to reflect what have been used in the past in the electronics sector.

Options for Alloy Designation or Naming System

The task group has considered several options that were deemed plausible. Options included:

1. Following academic metallurgy, alloys are designated by element symbols, strictly, in alphabetical order (e.g., AgAuBiCuInNiSbSn).
2. Following the conventional practice or for practicality and convenience, alloys are named starting with the matrix metal, then followed with element symbols that are, strictly, in alphabetical order (e.g., SnAgAuBiCuInNiSb).
3. Some believe that noble metals should be listed first. Noble metals should be in alphabetical order first followed by non-noble metals in alphabetical order (e.g., AgAuPdPtBiCuInSb).
4. List by the order of electromotive force series. Indium is not classified as a noble metal (in electromotive force, In = - 0.336 v; Ag = +0.80 v; Au = +1.42 v; e.g., AuPtPdAgCuBiSbIn).
5. Purely follow an alphabetical order of the name of elements in lieu of element symbols (e.g., antimony, bismuth, copper, indium, nickel, silver, tin).

With considerable deliberations and debates, and in view of the past historical practice and the forward-looking convenience, our task group then reached the consensus to use the naming system starting with the matrix metal (i.e., naming lead-free alloys by starting with Sn elemental metal). This is the genesis of today's lead-free alloy designations in J-STD-006 Table A-1.

Future Work

I hope that clarified the questions regarding the lead-free alloy designations being used in today's J-STD-006. Additionally, I want to take this opportunity to again mention the importance of future work for the task group to take on.

In our recent past meetings, I have challenged the task group to address four questions:

1. As a task group, how can we make the J-STD-006 document more useful, complete, informative, and practical for the industry, including suppliers, users, or other interested parties?
2. Which area(s) should be added?
3. Which area(s) should be expanded?
4. What are the priorities?

To this end, one recurring area that was brought up in our task group meetings was the differentiation and distinction between a dopant and an impurity. As more new alloys are being developed with intentionally added dopant(s) in a small weight percentage of the alloy composition, J-STD-006 bears the responsibility to provide a guide.

As stated before, the framework efforts should include updating solder alloy impurities and differentiating dopants from impurities. I have laid out the skeletal framework that is to be considered in three distinct categories of elements:

1. Current impurities elements (Table 3-2 of J-STD-006): Ag, Cd, Pb, Al, Cu, Sn, As, Fe, Zn, Au, In, Sb, Bi, and Ni.
2. Additional elements to be considered (phosphorus, sulfur, others). It is worth noting that QQ-S-571F (Federal Specification: Solder, Electronic) limits phosphorous (P) at 0.010 wt % and sulfur (S) at 0.005 wt %, but J-STD-006 makes no call on these two elements, which could potentially affect the properties and behavior of a solder alloy.
3. Dopants being used in alloys that are listed in the current impurity table as impurities (e.g., Ni, others).

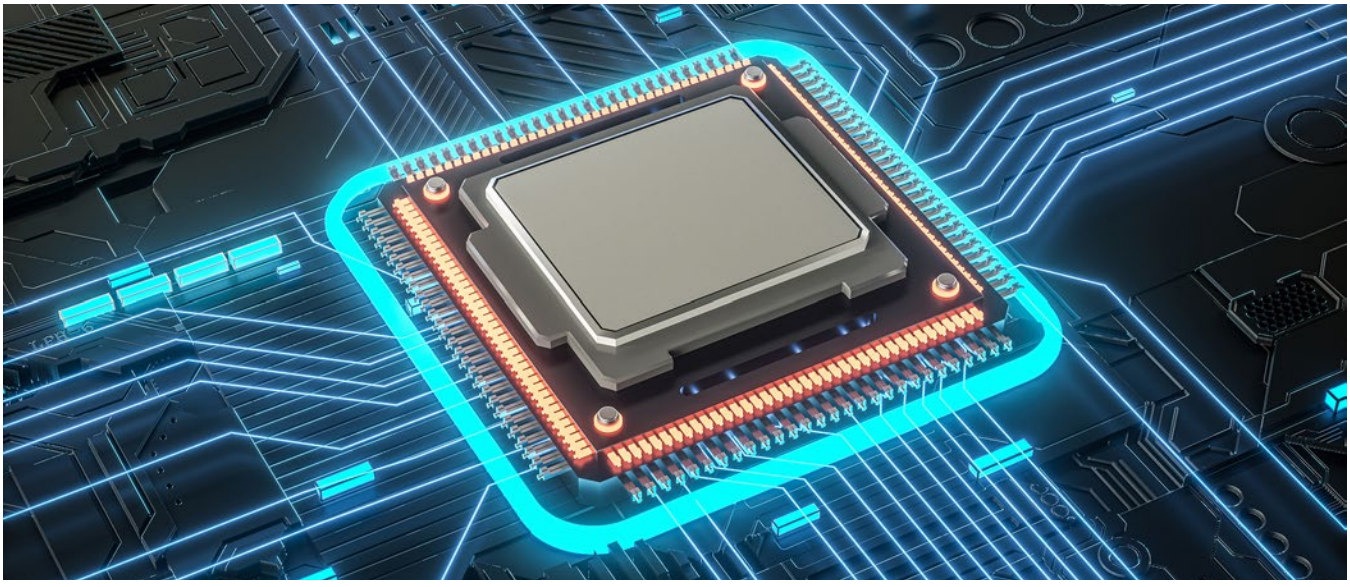
To move forward to the next stage of the development of J-STD-006, these areas are to be addressed, which will call for collaborative efforts from both suppliers and users of the industry, as well as any interesting parties.

I would also like to take this opportunity to invite and encourage the industry colleagues to attend and participate in the task group meetings. The next in-person meeting, if feasible, will be likely held at IPC APEX EXPO 2021 in San Diego, California (time and date to be determined). **SMT007**

Dr. Jennie S. Hwang—an international businesswoman and speaker and a business and technology advisor–is a pioneer and long-standing leader to SMT manufacturing since its inception as well as to the development and implementation of lead-free electronics technology. Among her many awards and honors, she was inducted to the International Hall of Fame-Women in Technology, elected to the National Academy of Engineering, named an R&D Star to Watch, and received a YWCA Achievement Award. Having held senior executive positions with Lockheed Martin Corp., Sherwin Williams Co., and SCM Corp., she was the CEO of International Electronic Materials Corp. and is currently CEO of H-Technologies Group, providing business, technology, and manufacturing solutions. She has served on the board of Fortune-500 NYSE companies and civic and university boards; the Commerce Department's Export Council; the National Materials and Manufacturing Board; the NIST Assessment Board; as the chairman of the Assessment Board of DoD Army Research Laboratory and the chairman of the Assessment Board of Army Engineering Centers; and various national panels/committees and international leadership positions. She is the author of 600+ publications and several books and is a speaker and author on trade, business, education, and social issues. Her formal education includes four academic degrees, as well as the Harvard Business School Executive Program and Columbia University Corporate Governance Program. For more information, visit JennieHwang.com. To read past columns or contact Hwang, click here.

Upcoming Presentations

Dr. Hwang will deliver a professional development course on **"Preventing Manufacturing Defects and Product Failure"** at the virtual SMTAI conference on October 5 (11:30 a.m.–3:00 p.m.). She will also deliver two courses at the virtual IMAPS International Microelectronics and Packaging Symposium on October 7 (3:00–5:00 p.m.) and October 8 (1:00–3:00 p.m.) on **"Packaging/Board Integrity and Solder Joint Reliability"** and **"Prevent Product Failure: Tin Whisker and Intermetallic Compounds,"** respectively.



IEEE's Heterogeneous Integration Roadmap, Part 1

Feature Interview by the I-Connect007 Editorial Team

This expert conversation focuses on the IEEE Heterogeneous Integration Roadmap (HIR)—a document that provides guidance for IC, PCB, and package designers, broken down by industry segment and performance requirements. Rita Horner of Synopsys shares her perspective from the IC side, as well as how the HIR might affect what happens on the PCB design and manufacturing side in the next few years. In Part 1, Rita provides a general overview of the HIR and its impact.

Nolan Johnson: Rita, can you kick us off by summarizing your background? Then, we'll shift into what the HIR means for PCB technologists.

Rita Horner: I have a master's degree in electrical engineering, and I spent about 10 years in circuit design, mainly transistor-level and mixed-signal design. I started with Hewlett-Packard, which spun off into Agilent. I left Agilent and then came back, which became Avago shortly thereafter. I also worked at two start-ups. I have done mixed-signal designs. I was part of the Integrated Circuits Business Division of HP, where we designed the ASICs and IPs that were used by the different divisions within HP.

Then, I moved into marketing. I joined Synopsys about eight years ago. My focus was mainly on the high-speed interfaces until six months ago when I moved to the design group of Synopsys, focusing on the 3DIC Compiler product that we are developing.

Johnson: You have the right mix of background to have a good perspective on what's happening with heterogeneous integration. What trends do you see?

Horner: 3D IC is a hot technology. It's becoming hot because it has two angles: technology and economy. The semiconductor market has reached a point that the smaller technology nodes are not able to meet the required levels of integration with a single die in a single packaged part. The dies are getting so large that they're not becoming manufacturable.

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If you're familiar with the stepper sizes, there's a maximum stepper size that you can physically build a die to; it's about 800 millimeters square, limited by the reticle. When a die gets that large, the yields go down exponentially, which makes the part very expensive. You get only so many parts per wafer because of low yields. To make things worse, that maximum reticle size is not enough for the high level of integration that is needed to bring everything closer together for the performance required by the cutting-edge applications, such as the AI accelerators and high-performance computing needs in the data centers and the high-end networking market. Combining multiple parts together in separate packages is not a practical option for these high-end products.

Rita Horner

Johnson: That makes for an interesting conflict. You need to get all of that functionality onto the silicon, but it's hard to get that much functionality onto the silicon.

Horner: Exactly. High-end computing technology needs reduced latencies. This is becoming very critical because every time you make a hop from one packaged part to the next device to access data, you add latency. A lot of these AI applications require a lot of access to memory. And if you're making so many hops and going back and forth, the turnaround trip costs you a lot of latency, which is not very appealing because it means processing data will be slow. Bringing the memory closer makes more sense. That's why there's a big movement that started with AMD in bringing the DRAM memory much closer. As a result, JEDEC started the high bandwidth memory (HBM) standard a few years ago.

Effectively, there are layers and layers of DRAM that are stacked together, as a block of memory that can be attached to a processing unit. It could be a CPU, GPU, or any SoCs that need high levels of memory access with low latency. By putting those devices close to each other—especially in the same package, where you don't have to go out of the package, across PCB traces to another package to get access to data—you minimize a lot of latency and save power.

As far as the economic aspect of it, a complex design with mixture of lots of dies in a package consists of many layers of complexities that that need to be addressed. If there is a way to communicate information during package floor planning to the SoC or the package designer, or the person who is going to assemble the part on a board, which could be beneficial to further optimize each part of the design, it could be optimized in parallel. Packages have many substrate layers, similar to the PCB layer concept, where having additional layers translates into increased cost. If you know, optimally, where to put the bump connections to the package substrate to minimize the number of substrate layers, or where to place the microbumps to make the most optimal die-to-die connection, to minimize the size of the interposer, these could translate to overall solution cost saving. There needs to be more communication between the package designer, the PCB designer, and the die designer for a cost-effective and optimal solution.

Dan Feinberg: 5G is accelerating that. One of the responses to this issue that you're discussing is the use of chiplets in CPU manufacture. Do you see that?

Horner: In many applications, it's not just because the die size is getting larger; it's also about when you have lots of parallel processing. At times, there are 40+ cores being processed in parallel inside a part. Looking at a few of AMD's designs, there are dies with four cores that are combined with four others of its own copy. That made it into four times four, so there are 16 cores within a package. When a large die is partitioned into smaller parts or for aggregating multiple cores, one has to decide on how to partition a die and what interfaces to use.

Feinberg: I just got through doing a build a few months ago with one of the new AMD chips, which is 24 threads. The challenge that I have, as a chiplet user, is temperature control. I had to go liquid cooling; it was not even a choice.

Horner: There are many challenges in multi-die package integration. Integrating multi-die in a package is not a new thing. It has been around for decades. In the past, there were very few devices that we were integrating, with very few connections between them. These were small designs compared to the multi-die systems in a package product that we see today. As more devices are included in a package, solution yield is reduced by the yield of each device multiplied. A single die in a package may have 99% yield, but then when you add one more device in the package, which may have 80% yield, you're talking about 80% times 99%, and your yield goes further down. By adding more devices, you're not helping the yield in that angle.

Different applications have various needs. That's why there are so many different types of interfaces. There are I/Os that require thousands of wires for one link connection. With the HBM interface for connection to the HBM memory stack, there needs to be 1,000+ die-to-die connections to one memory stack. In addition, these signals need to be shielded, which adds another level of complexities.

Feinberg: AMD is a leader in that area. I've always been kind of an Intel fan, but AMD seems to be leading. They seem to have gotten a good grasp on seven-nanometer geometries, where Intel is still struggling with anything smaller than 10 nanometers.

Horner: AMD no longer has their own internal fab. They depend on all their foundry and packaging partners. **SMT007**

Editor's Note: Stay tuned for Parts 2 and 3 in the October Design007 and PCB007 Magazines, respectively.

Real Time with... SMTAI: Aegis Software

Andy Shaughnessy speaks with Michael Ford, senior director of emerging industry strategy for Aegis Software, about its newest concept—Ontology—which the company will discuss during SMTAI. He also explains how Ontology relates to the company's existing MES products, as well as how it dovetails with the digital twin process. (View more at Real Time with... SMTAI 2020 virtual.)

How the HIR Impacts Design Through Assembly

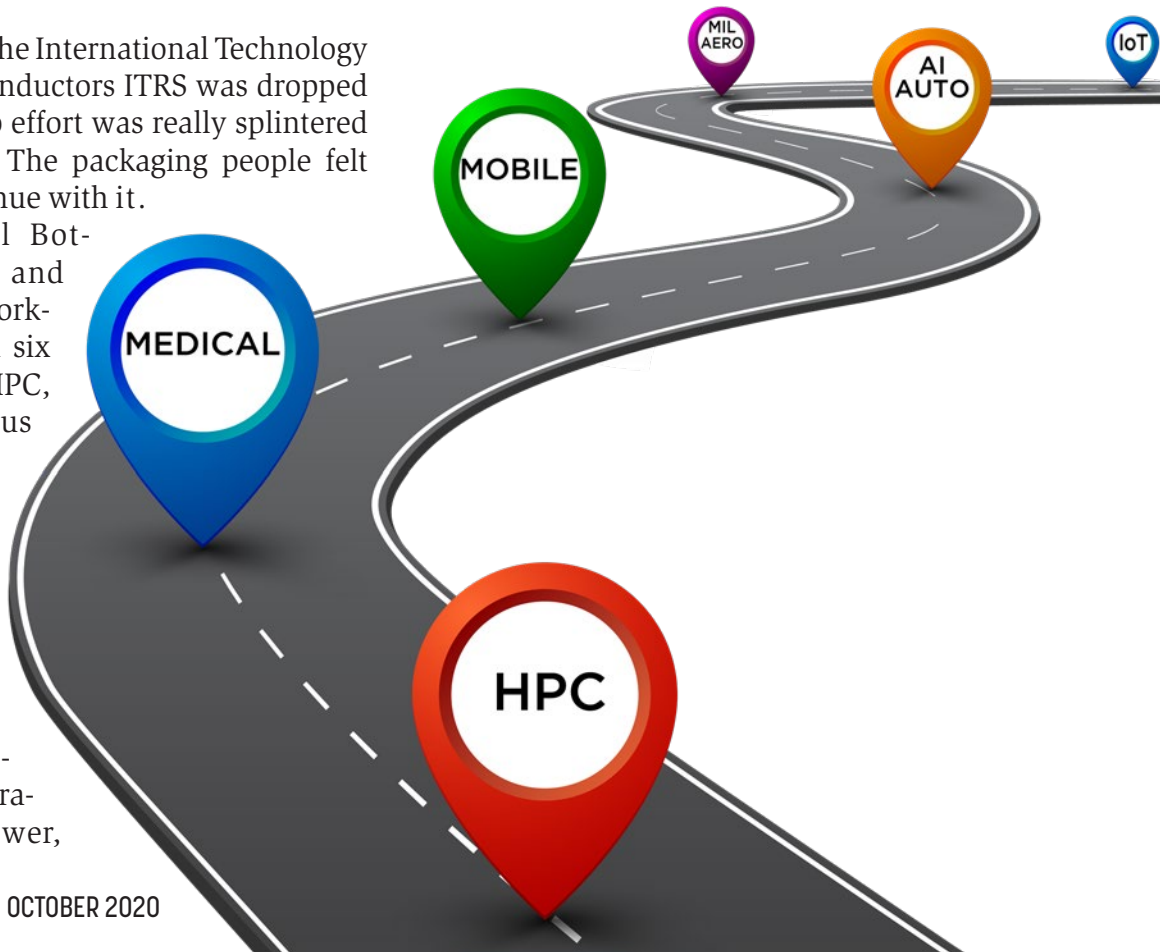
Feature Interview by the I-Connect007 Editorial Team

In this experts meeting on the Heterogeneous Integration Roadmap (HIR), the I-Connect007 editorial team met with Paul Wesling of the IEEE Electronics Packaging Society (EPS) to discuss what's in the HIR, where the organization is going with it, what the path is for the industry to have a roadmap like this, and how to use it in a practical sense.

Nolan Johnson: There is quite a lot of future technology in the HIR that will affect PCB design, fabrication, and assembly. Could you fill us in on how the HIR project began and provide us with an overview?

Paul Wesling: When the International Technology Roadmap for Semiconductors ITRS was dropped in 2016, the roadmap effort was really splintered into different areas. The packaging people felt that we should continue with it. Bill Chen and Bill Bottoms led that task and set up a bunch of working groups. We took six application areas: HPC, medical, autonomous automotive, mobile, aerospace and defense, and IoT. We have a chapter on each of these markets. Then, we have chapters on the various building blocks: single- and multi-chip integration, photonics, power, MEMS and sensors, and all of the 5G, analog, and mixed-signal stuff.

For the underlying technologies, we have a chapter on each of these, such as research materials and devices. A large section on future devices, such as carbon nanotubes, is from the Electron Devices Society (EDS). There are also small sections on supply chain and security. These are big issues across much of our IP, especially when there are various breakthroughs in the supply chain companies around the world, doing different things with PCB design, testing, integration, etc. We also cover thermal management, co-design, and simulation. How do we find CAD/EDA systems that will integrate from the transistor model all the way up to the PCB and the system level and pass information



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back and forth, as opposed to doing it in silos today? We still have the same problem there.

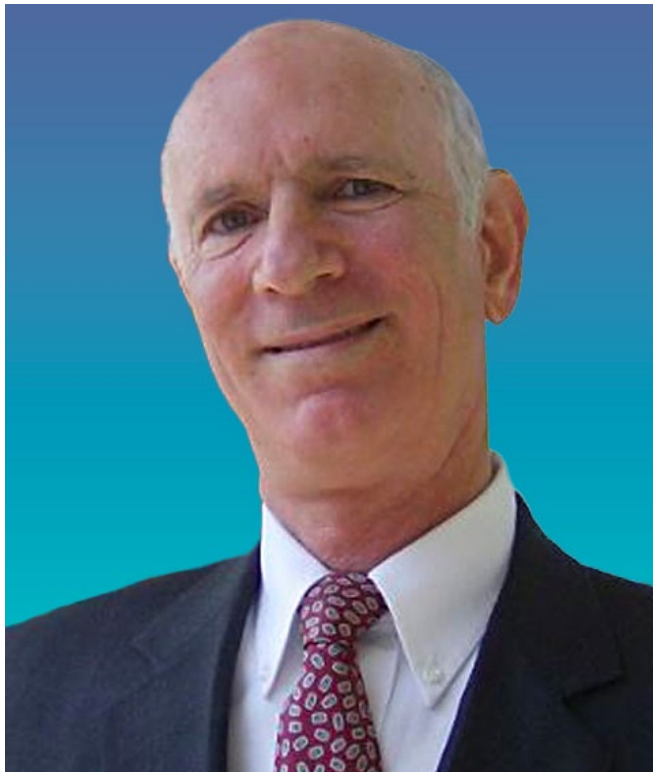
Finally, there are three technological areas. Perhaps the biggest focus areas are system-in-package (SiP) options, and where that's going over the next 10–15 years: 3D and 3D interconnect, and wafer-level packaging at the wafer-level, fan-in, and fan-out. It also covers module system integration and different substrates. That's my quick overview.

Johnson: How can people access it?

Wesling: On our website at pwesling.com/hir, you can pick out any chapter. In addition, there is a PDF of the full roadmap (>600 pages), or you can unzip it on your machine and have it locally with a full text search, which is kind of handy. It's the way I structure conference proceedings. You can also find a video overview that was prepared for ECTC and broadcast in June; it's a six-hour webinar with an index. For example, if you want to see what's going on with single- and multi-chip packaging, you can skip to the 176th minute, which will show a 10-minute summary by the head of that working group. We also have nine one-hour video overviews of many of the chapters that are more in-depth, and we're still working on similar videos for the other chapters.

Johnson: Some portions of the HIR directly apply to PCB fabrication; not all of them do, but some come pretty close. How is this roadmap intended to be used by the industry?

Wesling: There are four different groups that we see using this. First, research labs that need to look into the 10-year or 15-year period could use it. As we find out what they're doing, then we can reflect it every year or two in the roadmap and see what's integrating with other stuff. Second, the academic community could review it as well, such as Ph.D. students, depending on the projects on which they're working. Third, corporations that are either suppliers to this or users of it will want to keep an eye on it. They don't want to end up down a blind alley somewhere, working on a technology that does not seem to be getting support. Fourth, technologists can use it to ask, "Where should my career go in the next 10 years? If I'm working on high-level PCBs or things like that for power electronics, where do I see that integration for automotive electronics and 400-volt power distribution? Where is that going?"



Paul Wesling

We monitor these four communities because that's who could use this roadmap. Our next roadmap is supposed to come out soon. This is a large group of volunteers. But the idea is that we'll take the pre-competitive information that we can glean from our 400 or so volunteers and put it into updated roadmaps with, for example, new projections and issues with line width, or whatever it is we're tracking, and where it's going. We see it working for those four communities and being an interactive resource that's freely available, so we hope it gets passed around.

Johnson: A lot of information on the roadmap tends to be related to integrated circuits (ICs), which makes sense since much of the technology is now inside the packaging.

Wesling: It involves the chiplets and higher levels that are up and down the stack (Figure 1).

Johnson: Since our readers are primarily attuned to PCB manufacturing, how is the technology in the HIR going to change what happens on the PCB?

Wesling: First, I want to address co-design and simulation. We expect that instead of finding local maximums or optimization for IC layout and then having to have a lower level of optimization at the board level and system level, we hope to trade off across the whole stack of technology. We expect PCB people to be working backward with the IC and chiplet design. It will be a challenge for CAD/EDA companies to provide the tools.

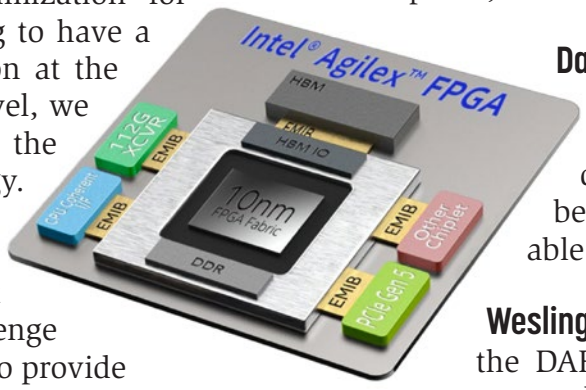


Figure 1: Intel Agilex FPGA Chiplet application. (Source: Intel)

Andy Shaughnessy: That's a fundamental change in how you do your job, who you communicate with, and what you communicate to them.

Happy Holden: We can't depend on Moore's Law any more. With five to seven nanometers for gate geometry, we're not getting all of our future gains by going to one nanometer, 0.1 nanometers, and 0.001 nanometers. The alternative would be putting multiple chips together in a different material, in some fashion, to make these future gains in performance and lower cost. It's not going to just be the single chip with all the horsepower of that single chip.

Wesling: We expect single chips to keep picking up more parts of the system, but the thermal and design and interconnect limitations aren't going to make that possible—except for special cases, high volume, or something like IoT. We expect to see better optimization. The board-level people must have models that can be extracted and pushed down to the chiplet level and the interconnects and the wafer-level processing stuff. There may be better models needed at the PCB level.

Testing is likely to change a lot. We hope to have a lot of known good die since it will be difficult getting access to things without having to scan in or scan out for all the parts at the board or the system level. There's going to be a testing issue, which is covered a lot in the test chapter. It may prove difficult for the board-level people to move to new materials, different interconnect speeds, different intra-process testing, etc.

Dan Feinberg: You mentioned chiplets quite a bit, which is relatively new. When do you recall chiplets first becoming commercially available in relevant places?

Wesling: Two years ago, I remember the DARPA thrust on chiplets. We would call them individual chips or subsets. Our roadmap covers both. We've adopted the idea that you have a bunch of chips and a bunch of passives, such as inductors and capacitors, and then make your system with interconnects.

Feinberg: Advanced Micro Devices (AMD) was the one that made great use out of it. They went from a lap behind Intel to a totally different racetrack because of chiplets. There are a lot of other uses for it, but what would you think is the driver? For me, the driver of chiplets has been the move toward 50- and 100-thread CPUs.

Wesling: Lisa Su, AMD's CEO and president, highlights that. It was their earlier generation, which we cover in the roadmap, that split that big chip into four chiplets to spread the power to make interconnect better and hook it up to memory better. That was an excellent application and probably the first major one we saw.

Aerospace and defense think chiplets will be their salvation for building systems because they can't build SOCs; they may only build 200 of their design. They need to use commercial chiplets and make their systems using your inter-

connects. Chiplets may become a moderately-used term, but we may also call it other things.

Holden: For me, this is an old topic because by 1972, we were putting multiple gallium arsenide LED dies on a PCB and wire bonding them over for second-generation calculators and things like that. Everybody thinks this is a 21st-century technology, but most of them aren't aware that back in the early '70s, we were doing a lot of chip-on-board and multiple chip-on-board.

Wesling: If you read chapter eight, you'll see that we still see wire bonding as a high-use application for bonding chips, three- and four-layer tiers, etc. Wafer-level packaging and flip chip may be coming in, but there's still going to be a lot of wire bonding.

Johnson: Happy's comments harken back to a time when all manufacturing took place at the same company. And because it was all under one roof, you could develop your own protocols and communications. It's different now. The various functional roles are fulfilled by third-party specialists. The need to communicate with multiple OEMs at the manufacturing level about this very detailed information is critical. For the PCB manufacturers, this technology could be the point where, no matter how well our systems work, they're going to break.

Wesling: That's why we've put in a supply chain chapter, which is not too developed, but we'll soon have one that's more extensive. One pain point is when only one company follows a standard. If we look back in five years to what we've published now, part of what we publish will not have been adopted. These are not standards; these are options for companies, consortiums, and university teams to get together and see if it works. Consequently, you'll see lots of potential solutions. Probably only a few will get implemented.

The other thing is in the supply chain. Our supply chain is spread out. Somebody does design, somebody does fabrication, and somebody else does assembly. This becomes a challenge in both supply chain and security. Looking into the crystal ball and knowing what will happen is the tough part. That's why this roadmap extends to about 600 pages because it covers lots of possibilities—not all of which are going to happen—that can keep people in jobs for the next 10 years, for example.

You want to look at how it affects what your focus is, which is substrates and PCBs, and—more specifically—do they go away and get replaced by some other multi-chip substrate? Does polymer end up going somewhere? Does low-temperature processing start coming in here? What kind of things do you see that you can pull out of here that might be interesting? Once you get some draft ideas, you might kick them back to the people in the working group—because they're all listed at the end of the chapter—and say, "I'm thinking this. Is that still what you're thinking?"

This morning, I thought, "This is going to be about setting the ground rules and projections, and then every few months, coming up with something else—either digging more deeply into something that wasn't covered before to say what could happen or correcting what you thought earlier." Over the next months, we hope to have many of the updated chapters out for the 2020 version. Several of the chapters are being fully rewritten, but most of them are just being updated.

Johnson: The change to heterogeneous integration and the use of chiplets really is based on using an interposer, which ties together unpackaged chips into a system. Is that basically a PCB inside the system-in-package (SiP)?

Wesling: Yes. It's between silicon and the next level—the interposer (Figure 2).

Johnson: The interposer employs an interconnect design methodology—more than you would normally use in an active piece of silicon. Does that mean that PCB designer experience is going to be valuable on the wafer design side? Do the design tools need to change?

Wesling: Things like that are analogous to what PCBs have done in the past but at much higher

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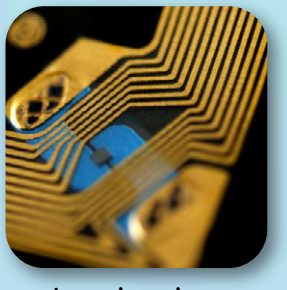

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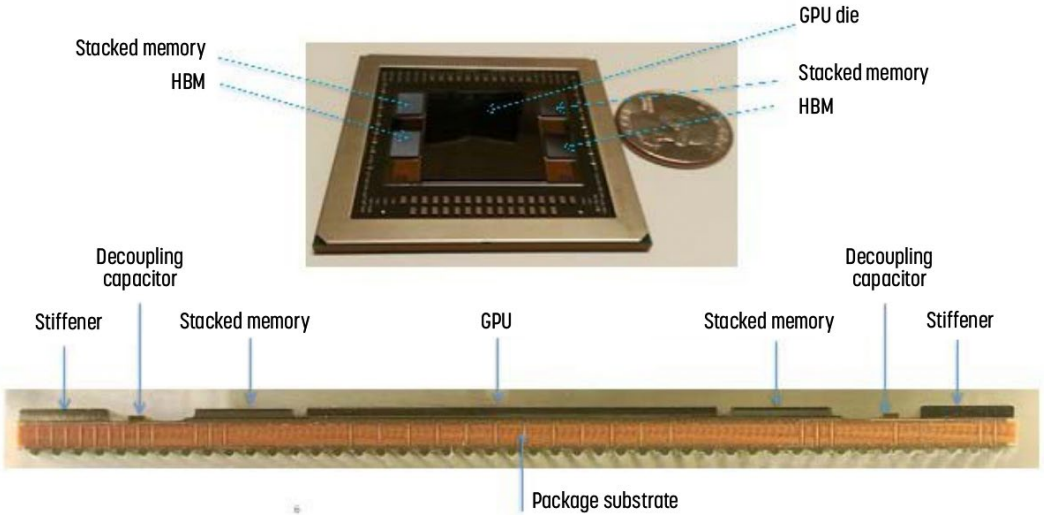

Figure 2: AMD Fiji GPU-HBM Si Interposer 2.5D Package. (Source: ASE)

densities. My guess is that the design function is going to be subsumed by the system-level packaging and substrate people rather than the PCB industry.

Holden: We don't have a roadmap, but it is also important to emphasize the other end of the spectrum. I believe in disposable electronics and printed electronics, such as a wristband that you can throw away when you're done using it. It would be made out of paper but designed with a five-cent chip to communicate with my smartphone and collect the information my doctor wants. Then it would upload data to AI that makes conclusions and tells my doctor to give me a call to come in if it doesn't like what it's seeing.

Wesling: It's printed roll to roll and extremely cheap, almost like a newspaper.

Holden: That's where some of our people in PCB manufacturing or flex will decide to invest in that part of the developing market.

Johnson: Thank you for your time, Paul. I hope you had a great time.

Wesling: This has been fun. **SMT007**

Lean Digital Thread: DFM Is Now as Easy as Spellcheck

by Sagi Reuven
SIEMENS DIGITAL INDUSTRIES


Sagi Reuven

In past columns, I've written about topics mostly related to the shop floor, including (1) data collection and the basic questions you can answer, (2) material management and its impact, and (3) data-driven decisions and micro-solutions in manufacturing.

In my September column, I planned to present a few micro-solutions for electronics manufacturing, but I've decided to "swim upstream" or simply to shift left. It is clear to everyone in the Industry 4.0 era that the holy grail is to close the loop between design and manufacturing. Mergers and acquisitions of billions of dollars were initiated to support this vision. In this column, I will talk about design for manufacturing (DFM).

To read the full column, click here.

Sagi Reuven is a business development manager for the electronics industry, Siemens Digital Industries. Download your free copy of the book *The Printed Circuit Assembler's Guide to… Advanced Manufacturing in the Digital Age* from Mentor, a Siemens Business, and visit I-007eBooks.com for other free, educational titles. You can also view Siemens' free, 12-part, on-demand webinar series "Implementing Digital Twin Best Practices From Design Through Manufacturing."

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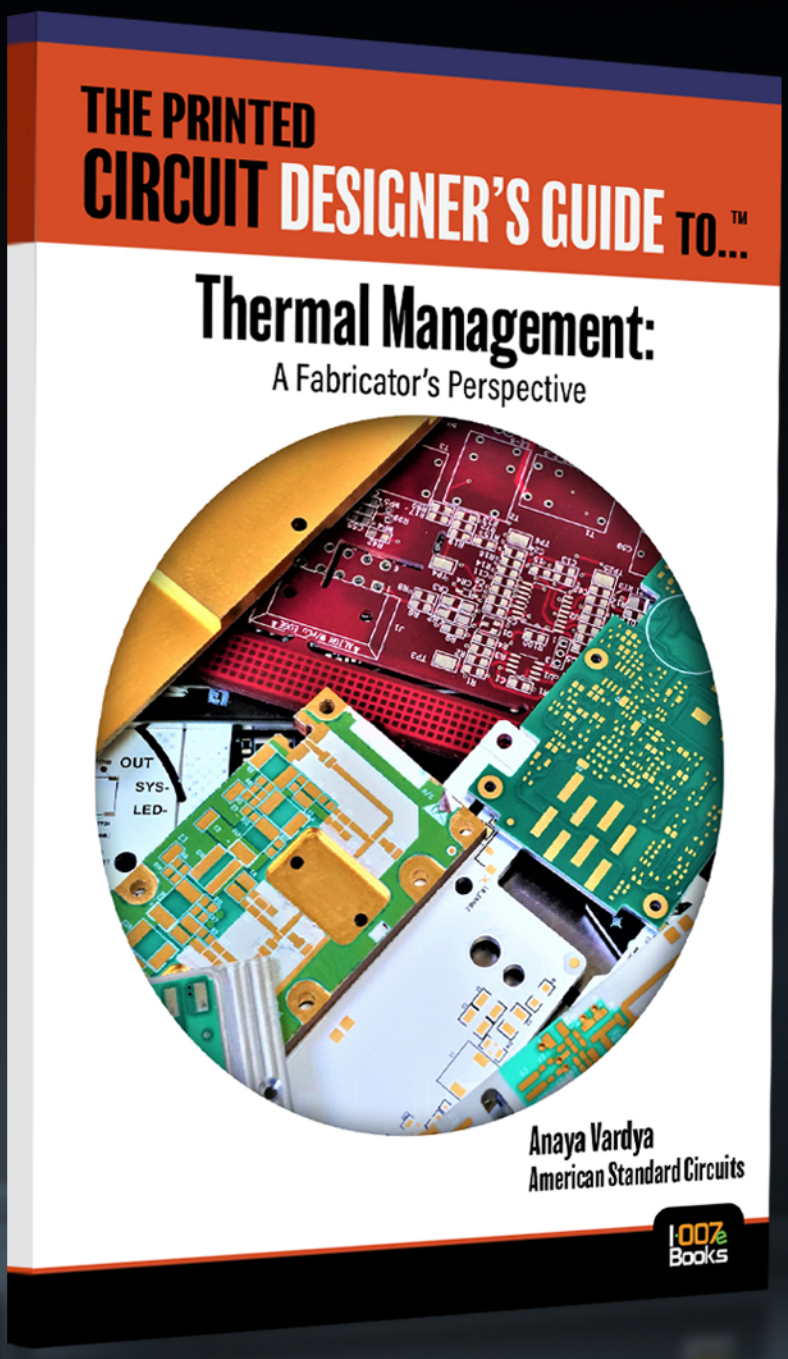

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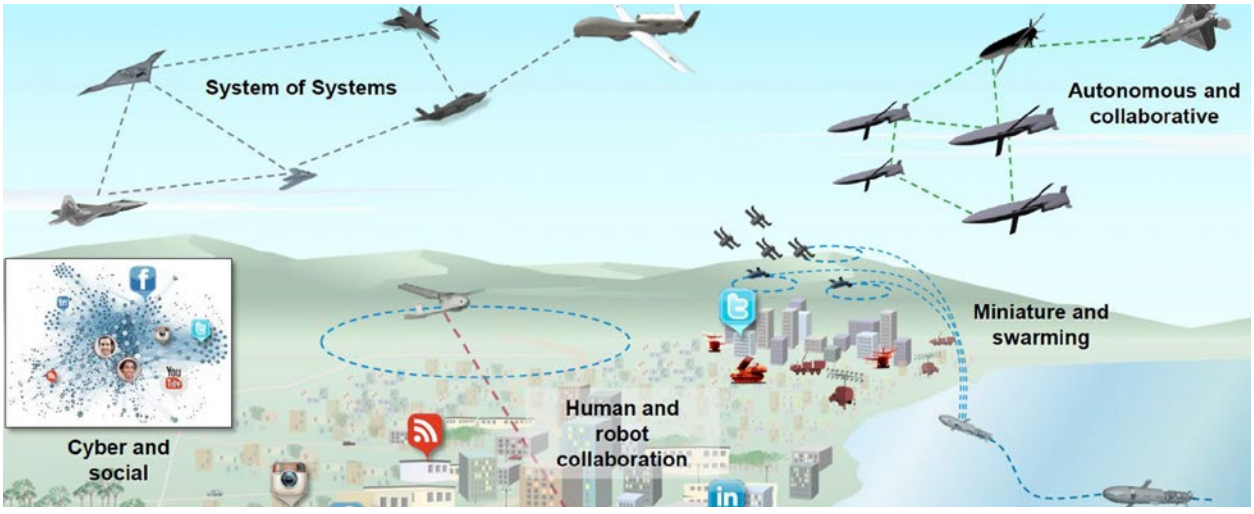

The Aerospace and Defense Chapter of the HIR

Feature Interview by the I-Connect007 Editorial Team

Nolan Johnson and Andy Shaughnessy recently spoke with Jeff Demmin of Keysight Technologies, who breaks down the work his team has done on the Aerospace and Defense Chapter of the Heterogeneous Integration Roadmap (HIR).

Nolan Johnson: Jeff, IEEE pointed us in your direction to discuss your chapter of the HIR. What's your background and involvement with the HIR?

Jeff Demmin: My background is broadly in semiconductor packaging. From 2015 to 2019, I worked for a company called Booz Allen Hamilton, which is a major government contractor. In that role, I supported leading-edge technical research related to packaging and heterogeneous integration, primarily at DARPA. I also have some background in the publishing world.

With my long career in packaging and my more recent experience specifically in the military and aerospace arena, I got tapped to work on the Aerospace and Defense Chapter of the HIR. I know most of the people involved in it, and I like to participate in industry activities, so it was an obvious match. Also, I want to be clear that my involvement is as the co-chair of this committee on the HIR and is not associated with my work for Keysight Technologies, nor does it represent the company's thoughts. I do this mostly in my spare time, which is probably true of many of the people participating.

I jumped in relatively early a few years ago, shortly after the HIR effort was begun. It was created to continue the work of the broadly used International Technology Roadmap for Semiconductors (ITRS), which had been around for a couple of decades, driving the node-based metrics for how the semiconductor industry should move ahead. But with Moore's Law running out of steam, mostly meaning that it's too expensive to keep it going, the HIR was one thrust that arose from the demise of the ITRS.

Johnson: The rationale makes sense. There may be a portion of your overall design that requires cutting-edge fabrication technologies but forcing your entire design to adhere to that

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Jeff Demmin

just because you need it in one key section has always been onerous. This does give you the opportunity to flex with what's inside the package.

Demmin: The most obvious example of that, which has been recognized for a long time, is memory and processors. They use different fabrication processes. It's still silicon, digital, etc., but they're different processes just because of the nature of how they function. Splitting memory off from processors has been common for quite a while.

But all the other functions that end up in a big system-on-chip piece of silicon makes it quite inefficient to do it that way. Designers do everything they can to minimize the area's silicon usage. And if you can carve out something that doesn't need that leading node, that's a smart thing to do, but you need to put it all back together after you carve it up. That's the heterogeneous integration angle need that arises from this partitioning.

Johnson: Your target audience and the industry you're writing about have a reputation for being fairly conservative. What would be the motivation for the mil-aero industry to jump into this technology?

Demmin: It's different depending on what industry you're in. One of the challenges is that the HIR effort covers everything from consumer to military. Companies that are on the digital high-volume side that are very supportive of this—such as Intel, AMD, and NVIDIA—can save a lot of money and create new capabilities if they can divide up their functions and then integrate them after the optimized manufacturing of each.

Xilinx was the first to divide up one of their big FPGAs, and they split it into four slices and put them on a silicon interposer that connected them together. Nowadays, that's pretty common to do something like that; companies like Intel are integrating different kinds of devices—not just the same device divided into more manageable chips. There's a lot of interest in heterogeneous integration of processors, data converters, memory, ASICs, and even optical components now.

On the military side, in spite of what people might envision as unlimited funding for military stuff, that's not really the case—especially when the volumes are low, and you don't have the total volume driver as you do in cellphones to amortize design, mask, and fab costs. Having those same kinds of savings, while still mixing and matching the best types of devices for different functions, offers that benefit for the aerospace and defense world.

It has even more challenging because there would commonly be a wider variety of devices potentially in a radar system or defense communication or electronic warfare where you need to be able to put together silicon, gallium arsenide, indium phosphide, and gallium nitride, among other device types to get the best possible performance. Challenges are conceptually similar in military and aerospace, but there are typically more types of devices for these specialized applications.

Johnson: What was your team's process for putting together the chapter?

Demmin: Tim Lee of Boeing is the other co-chair, and he started on this before I did. The roadmapping process is especially tricky for heterogeneous integration, where there are so many variables. It doesn't always work to have the node-drive tables and metrics as had been in the ITRS. There are different types of devices, applications, design processes, and materials. There are so many more variables that couldn't replicate what had been done before on roadmaps.

The aerospace and defense chapter starts with a landscape of what people are doing. That meant compiling information on government efforts in this area, as well as some industry capabilities. Step zero of a roadmap is to have a starting point. The initial release of the chapter last year was more like a landscape, such as, "Where do things stand now? What are some of the activities underway?" It wasn't as much of a prescriptive roadmap of what we're projecting to be in place, but we will be working toward that in future editions. The process moving forward will follow the same practice as the ITRS, with alternating years of totally new versions and more modest updates in years in between. We're due for an update with some changes.

For the 2020 update after the inaugural 2019 edition, we put together a high-level table that looks more like a roadmap but still needs input to populate the various topics into the future. We broke it up into some different areas of performance, metrics, design processes, integration technologies, and segments of reliability. For these heterogeneous systems, reliability has not been thoroughly thought out and captured. There are all kinds of standards for single chips and packaging. There are different approaches that are still in the works.

One example that highlights how A&D is different from commercial and consumer products is the supply chain. That's one of the big differences between aerospace and defense compared to the product areas covered in the HIR. It's just a matter of security requirements throughout your supply chain, but it also requires obsolescence management in A&D because product lifetimes are often longer than the typical lifetime of devices within it. That's much less of an issue for commercial products where there are multiple suppliers, and you are churning new designs routinely that incorporate whatever the latest available devices are.

One new development that we expect to help the HIR is high-level interest and funding in semiconductor manufacturing from the U.S. Government. You've probably seen a couple of different bills in Congress and the Senate. They represent an enormous level of funding—at least $25B—for the semiconductor industry in the U.S. Clearly, it's focused on manufacturing, which is a notable change and a good addition to the DARPA-style research targeting breakthrough technologies. Also, it's very broadly based, with funding via the NSF, Department of Energy, and Department of Commerce—not just the DoD. There are efforts to create interposer-based heterogeneous integration facilities in the U.S., for example, rather than relying on off-shore capabilities.

One example that highlights how A&D is different from commercial and consumer products is the supply chain.

Johnson: You do have a bit of interposer design and manufacturing required for heterogeneous integration.

Demmin: It's just interconnect on the interposer, so theoretically, it's easier than fabricating leading-edge devices. People have even tried things like having just a layer or two for customization in your interposer design above standard pre-fabricated power and ground planes. It's not quite as efficient for performance or design, but you can do it faster. As volumes increase, I can see some novel approaches like this facilitating adoption by reducing cost and turnaround time.

In DARPA's CHIPS program, part of the output was some very advanced designs and integration schemes, but getting those interposers manufactured and devices assembled was difficult because those capabilities aren't really available on a merchant basis in the U.S. Another output from the CHIPS program was a "wish list" for a national capability for interposer-based assembly.

This was input into the SHIP program. SHIP is a Naval Surface Warfare Center program for "State-of-the-Art Heterogeneous Integrated Packaging." This program is underway, and all of the detailed specifications and metrics for the SHIP program will be very helpful for the HIR.

Johnson: There is a lot of implied impact on PCB fabrication and assembly down the line as heterogenous integration becomes more prevalent.

Demmin: Definitely. All the advanced R&D like at DARPA is necessary, but a lot of it comes back to the PCBs for the advanced package substrates. That's where the rubber hits the road. The large volume of everything depends on the circuit board.

DARPA frequently uses a slide that shows that the PCB is the original heterogeneous integration platform, and it arose out of the need during World War II for a proximity fuse. They needed to get a lot of functionality within the small device, and the first high-volume PCB was the answer. The most advanced packaging substrate is conceptually no different from that PCB from 75 years ago.

Johnson: Do you have some specific feedback you'd like to hear from industry participants?

Demmin: We have a few others besides Tim and me, but we'd appreciate anyone who can help with informed input. To provide some focus, I've sent them this table, asking them to provide inputs on whether there should be other rows and get their input on what they think is state of the art, what they think it should be, and where it's headed. We're theoretically doing a 5-, 10-, and 15-year outlook, and it might be useful to have more granularity. Feedback on this table is the main thing I've asked for from other volunteers and the audiences of these presentations.

Johnson: Thank you very much, Jeff.

Demmin: Thanks. SMT007

Editor's note: To learn more, read Demmin's article "The Heterogeneous Integration Roadmap for Aerospace and Defense" on page 32 of this issue.

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The Heterogeneous Integration Roadmap for Aerospace and Defense

Feature by Jeff Demmin
KEYSIGHT TECHNOLOGIES

1. Summary

Semiconductor Roadmap History

Most people in the semiconductor industry are familiar with the International Technology Roadmap for Semiconductors (ITRS), which provided guidance for the industry starting in 1991 (as the National Technology Roadmap for Semiconductors). As the benefits of Moore's Law became more difficult and more expensive to achieve, the organization decided to publish a final version in 2016. The baton was handed to the Heterogeneous Integration Roadmap (HIR), with the realization that heterogeneous integration—assembling different types of devices rather than monolithic fabrication—is an important enabler for continued progress in the semiconductor industry [1].

The aerospace and defense segment of the semiconductor industry has unique needs in terms of technology, security, supply chain, and lifecycle. Heterogeneous integration is a critical technology that intersects all of these challenges, so the HIR organization identified aerospace and defense (A&D) as one of the topics to have a chapter and a technical working group (TWG) that specifically targets the unique requirements of aerospace and defense. The HIR identifies challenges in 5-, 10-, and 15-year horizons and provides guidance on how to meet those challenges. This is, of course, a perpetual work-in-progress and will be updated as capabilities move forward and new requirements arise.

Initial Scope

The initial version of the A&D chapter published in 2019 is focused largely on challenges and requirements for the U.S. Aerospace and Defense Industry. The intent of the HIR is to create a document that provides guidance that is useful to the semiconductor community around the world, so the U.S.-centric viewpoint should be seen as just the starting point for this work. There are certainly many technical challenges that are pervasive throughout the international A&D industry, such as reliability, bandwidth, thermal management, radiation hardening, long product development cycles and lifetime, and supply chain security, so much of the content can be generalized beyond the U.S. aerospace and defense industry. Future revisions of this chapter will reflect that broader scope.

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2020 Update

The 2020 updates to the A&D chapter in the 2019 edition include: (1) updates on government-funded heterogeneous integration programs, (2) recent relevant market data, and (3) the 0.1 version of the A&D Roadmap table. Populating and refining the table in Figure 10 will be the focus of the 2021 edition of the HIR.

2. Government Investment in Heterogeneous Integration

DARPA's DAHI Program

The U.S. Government, and DARPA specifically, has a long history of investing in heterogeneous integration. Figure 1 shows a timeline of these investments, which were often focused on specific applications and structures. The recent Diverse Accessible Heterogeneous Integration (DAHI) program was a large effort that demonstrated HI for a wide range of devices, with fine-pitch interconnect for breakthrough performance and capabilities. Figure 2 shows the progression during the DAHI program. This work helped to shape initial thoughts for the HIR A&D effort, and the metrics tables for DAHI and other programs provide useful inputs for roadmapping efforts.

DARPA's CHIPS Program

Following DAHI, DARPA's Common Heterogeneous Integration and Intellectual Property Reuse Strategies (CHIPS) program worked to establish a standard interface and promote IP reuse in a "chiplet" ecosystem designed to make heterogeneous integration more practical. This vision is shown in Figure 3, and the program metrics are shown in Figure 4. One significant outcome of CHIPS was a demonstration by prime contractor Intel and its partners of an Intel FPGA integrated with leading-edge data converters, an optical device, and other chips using its Advanced Interface Bus (AIB), the interface standard selected in the CHIPS program.

One outcome of the CHIPS program was the quantification of the interposer-based heterogeneous integration manufacturing requirements, which have been lacking on a merchant

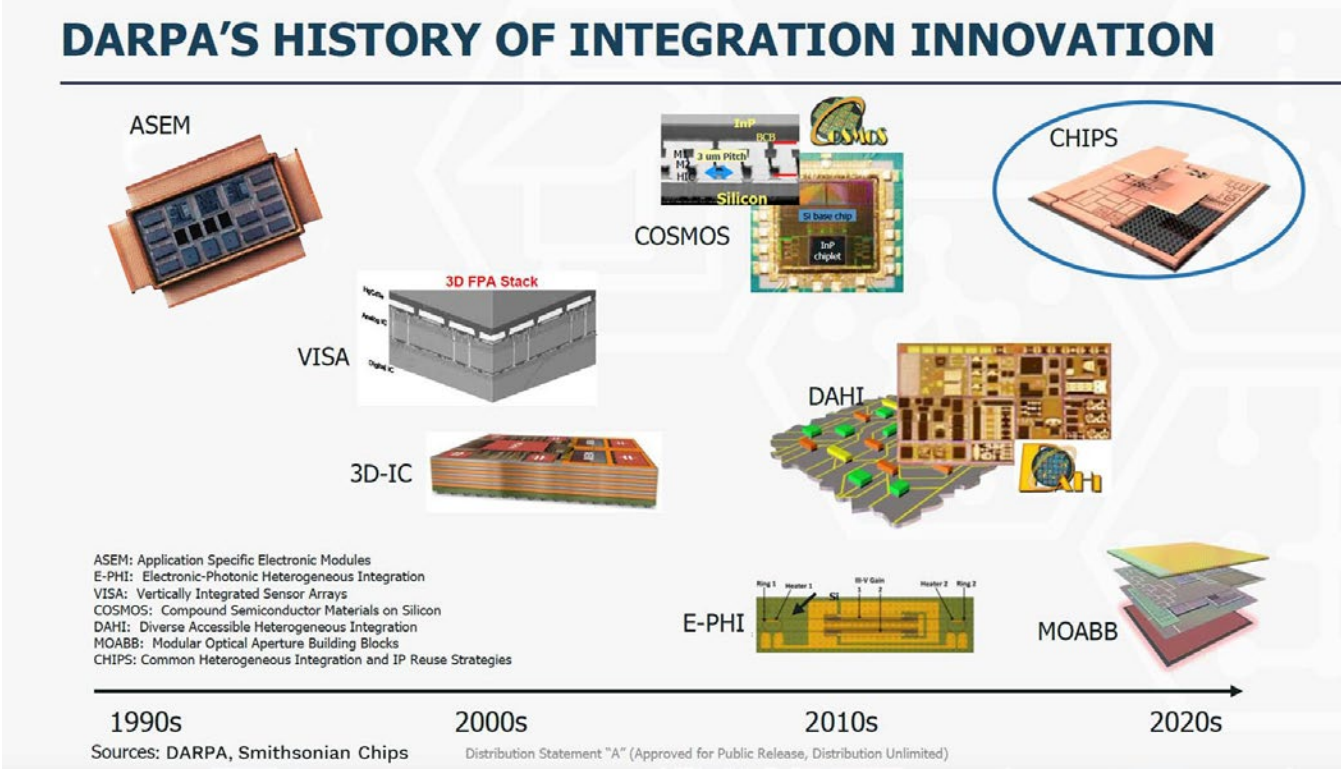


Figure 1: DARPA has a long history of guiding and investing in heterogeneous integration [2].

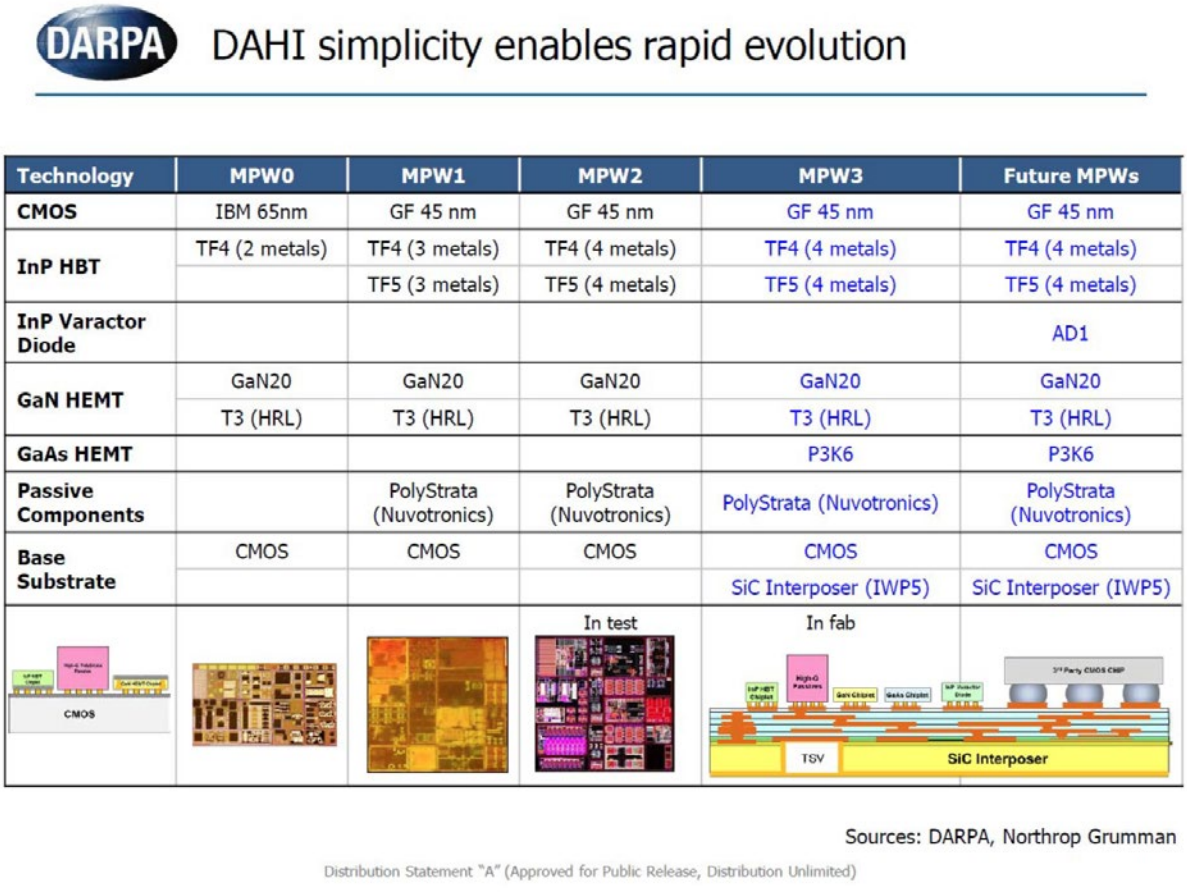


Figure 2: DARPA's DAHI program has produced increasingly sophisticated multi-project wafers (MPWs) with compound semiconductor devices integrated on a CMOS silicon interposer [2].

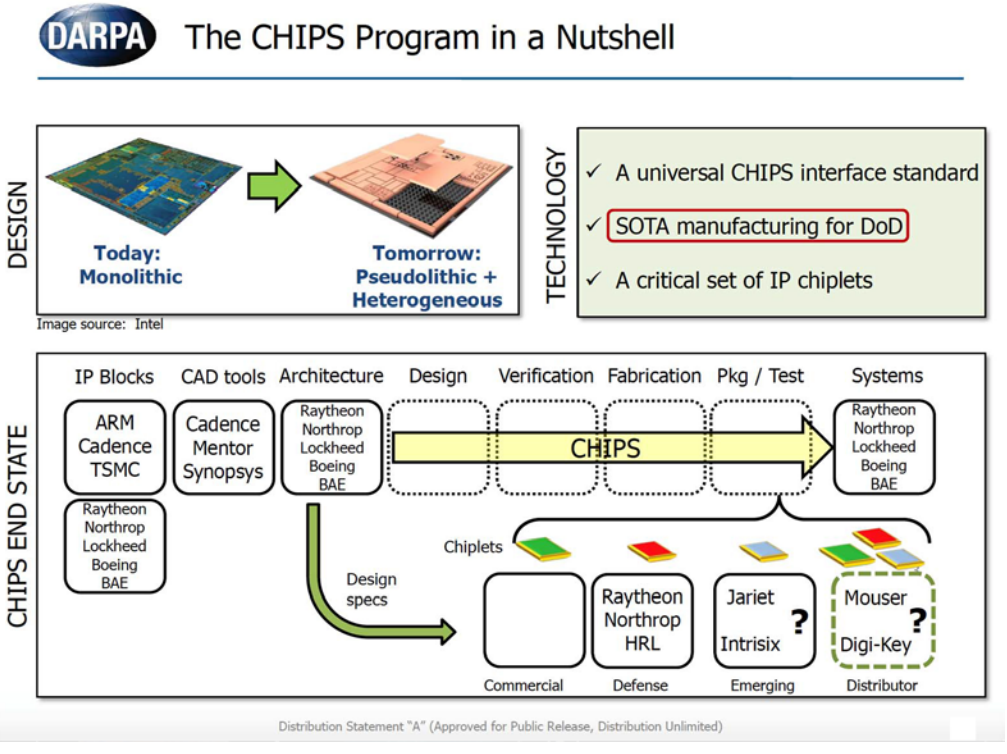
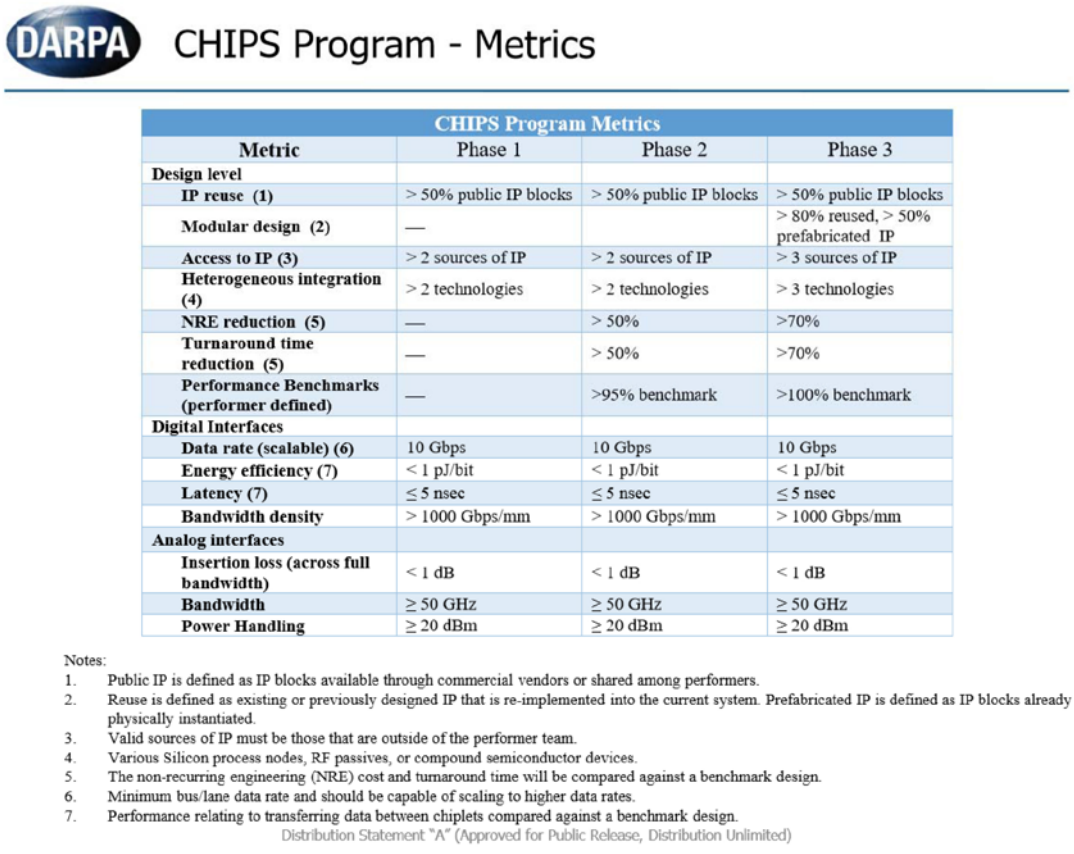


Figure 3: DARPA's CHIPS program envisions a chiplet ecosystem that simplifies heterogeneous integration [3].



CHIPS Program Metrics			
Metric	Phase 1	Phase 2	Phase 3
Design level			
IP reuse (1)	> 50% public IP blocks	> 50% public IP blocks	> 50% public IP blocks
Modular design (2)	—		> 80% reused, > 50% prefabricated IP
Access to IP (3)	> 2 sources of IP	> 2 sources of IP	> 3 sources of IP
Heterogeneous integration (4)	> 2 technologies	> 2 technologies	> 3 technologies
NRE reduction (5)	—	> 50%	>70%
Turnaround time reduction (5)	—	> 50%	>70%
Performance Benchmarks (performer defined)	—	>95% benchmark	>100% benchmark
Digital Interfaces			
Data rate (scalable) (6)	10 Gbps	10 Gbps	10 Gbps
Energy efficiency (7)	< 1 pJ/bit	< 1 pJ/bit	< 1 pJ/bit
Latency (7)	≤ 5 nsec	≤ 5 nsec	≤ 5 nsec
Bandwidth density	> 1000 Gbps/mm	> 1000 Gbps/mm	> 1000 Gbps/mm
Analog interfaces			
Insertion loss (across full bandwidth)	< 1 dB	< 1 dB	< 1 dB
Bandwidth	≥ 50 GHz	≥ 50 GHz	≥ 50 GHz
Power Handling	≥ 20 dBm	≥ 20 dBm	≥ 20 dBm

Notes:
1. Public IP is defined as IP blocks available through commercial vendors or shared among performers.
2. Reuse is defined as existing or previously designed IP that is re-implemented into the current system. Prefabricated IP is defined as IP blocks already physically instantiated.
3. Valid sources of IP must be those that are outside of the performer team.
4. Various Silicon process nodes, RF passives, or compound semiconductor devices.
5. The non-recurring engineering (NRE) cost and turnaround time will be compared against a benchmark design.
6. Minimum bus/lane data rate and should be capable of scaling to higher data rates.
7. Performance relating to transferring data between chiplets compared against a benchmark design.

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Figure 4: The CHIPS program metrics provide useful inputs for the HIR A&D Roadmap [3].

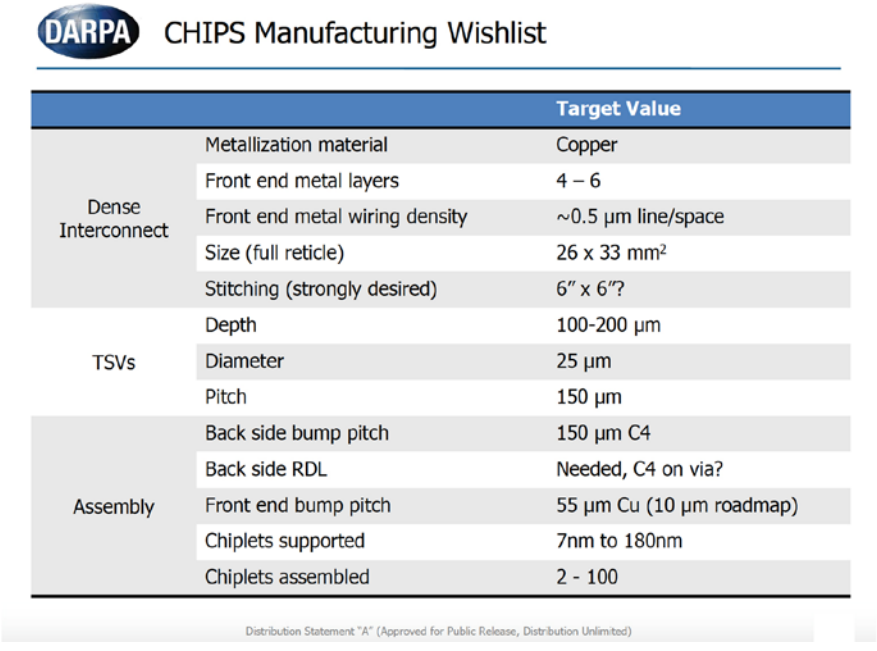

Figure 5: CHIPS wish list for interposer-based manufacturing in chiplet ecosystem [4].

or foundry basis in the U.S. These requirements and the vision of how to address this for A&D applications are summarized in Figures 5 and 6.

NSWC's SHIP Program

With the lack of an established domestic manufacturing base for interposer-based HI, as noted previously, the State-of-the-art Het-

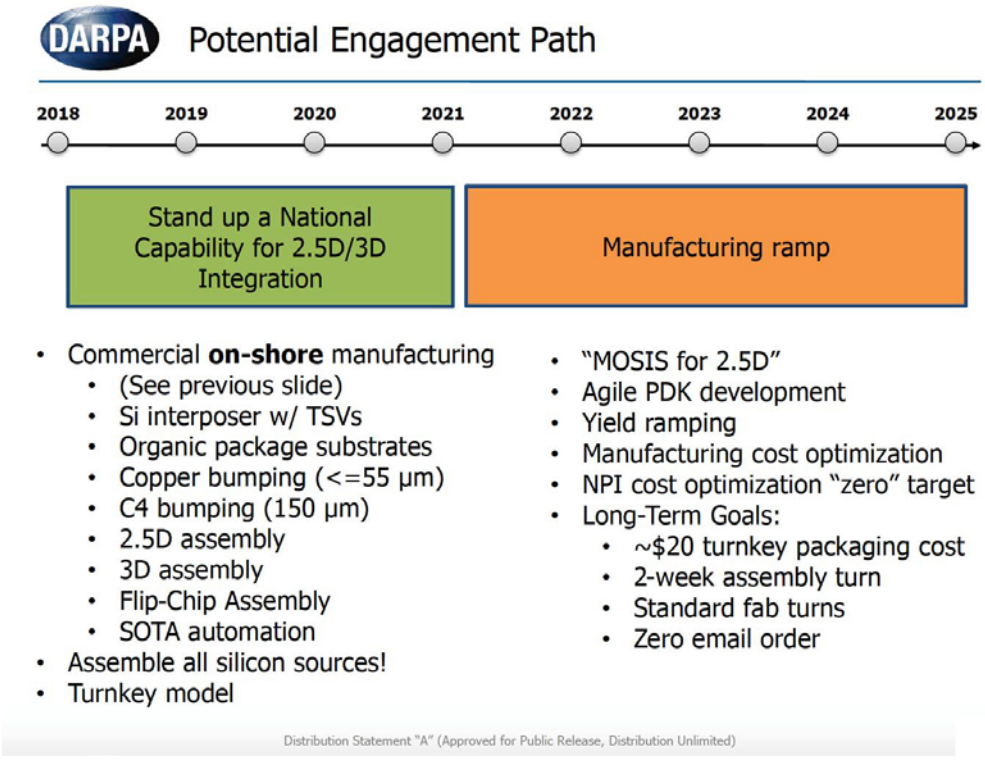

Figure 6: Timeline for the CHIPS manufacturing vision [4].

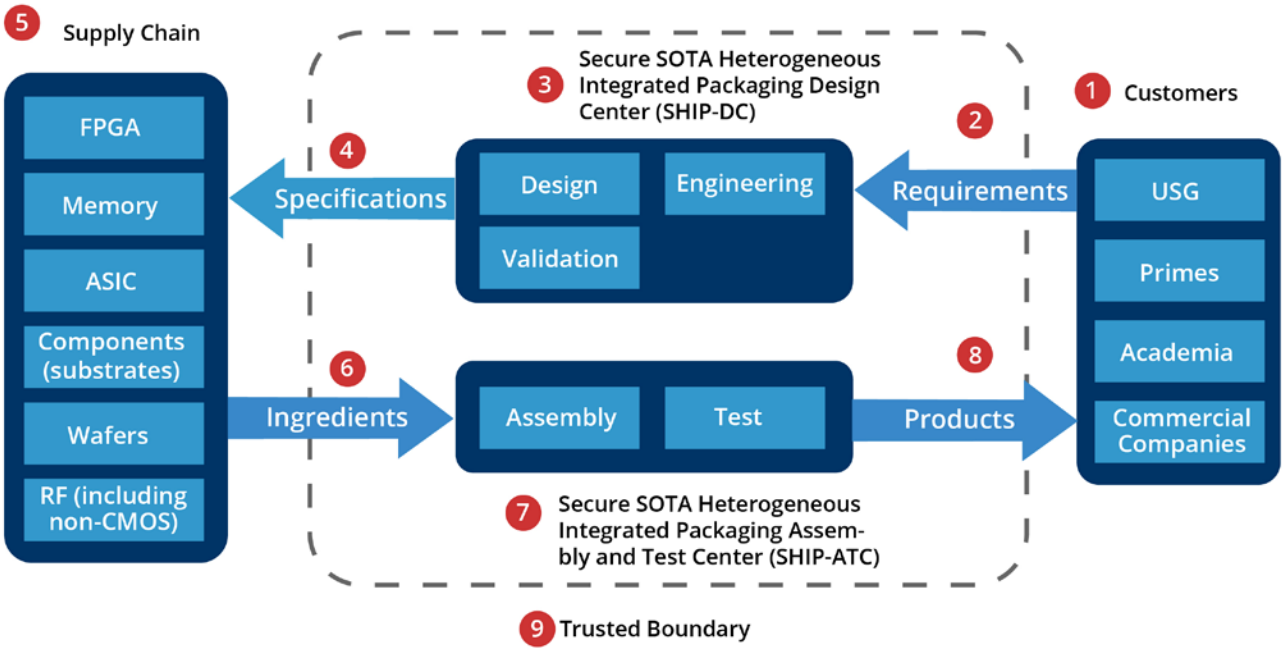

Figure 7: The SHIP program will create secure design, assembly, and test facilities for heterogeneous integration, as illustrated here [5].

erogeneous Integrated Packaging (SHIP) program was created by the Naval Surface Warfare Center (Crane, Indiana). The vision is shown in Figure 7, and some high-level metrics are shown as well (Figure 8). The program is divided into SHIP-Digital and SHIP-RF, with Intel and Xilinx selected for Phase 1 on the digital side, and Northrop Grumman, Qorvo, GE

Table 3: General Capacity and Capability for the SHIP-ATC.

Category	IOC	FOC	Scale
Capacity: Volume (annual)	1k+	10k+	100k
Silicon interposer	Required	Required	Required
Organic interposer	Preferred	Required	Required
Utilize SOTA COTS FPGA[1] and programmable devices	Required	Required	Required
Structured ASIC	Preferred	Preferred	Required
Security	ITAR	ITAR	Classified
Number of chips/package[2]	4	8	12+
Supply chain target	>50% US	>75% US	>90% US
Can process singulated die	Required	Required	Required
Can process up to 300mm wafers	Preferred	Required	Required
Can process 200mm wafers	Preferred	Preferred	Required

[1]Must include ability to integrate and test SOTA FPGA (<14nm), not required for RF-centric applications.
[2]Could include, but not limited to, memory, ADC/DAC, transceivers, optical couplers, ASIC, structured ASICs, etc.

Figure 8: High-level metrics for the SHIP program are useful for the HIR A&D Roadmap. There are more detailed metrics in the SHIP solicitation [5].

Research, and Keysight Technologies selected for RF. Each of those teams created a plan in Phase 1 to establish a self-sustaining HI manufacturing capability as a commercial entity, for either digital or RF applications. The government is willing to make a significant initial investment, but the primary goal is for that capability to be self-sustaining. We expect to include an update on the continuation of the SHIP program in the 2021 edition of HIR.

New Government Investments

It is notable that domestic semiconductor manufacturing is getting significant visibility with the proposed "CHIPS for America Act." These incentives and investments are substantial—on the order of $25B—and it is clear that the focus is on manufacturing. It is called out specifically in each top-line bullet (Figure 9). There is also $5B for Advanced Packaging,

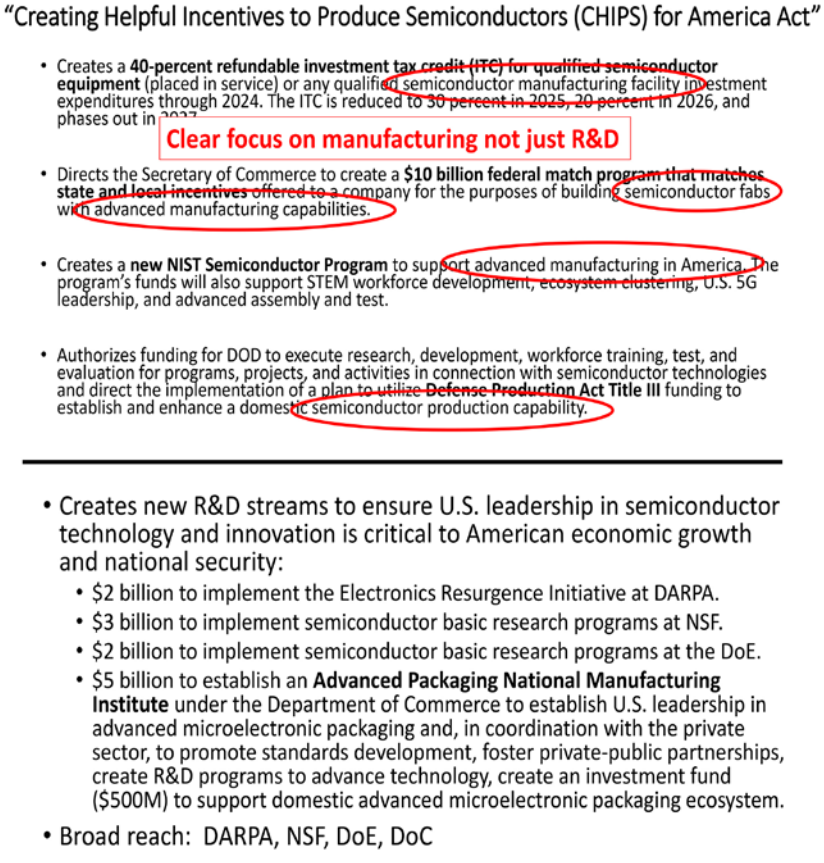

Figure 9: Proposed investment by the U.S. Government in semiconductor manufacturing [6 & 7].

Area	Metric	SOTA 2020	2025	2030	2035	comment
Performance	Frequency	Higher freq., lower P				
	Power	Higher freq., lower P	Up through X-Band			
	Thermal					
Design	Tools	Point solutions				
	Interfaces	CHIPS AIB (early traction)	Broad adoption + roadmap			
	IP reuse	Chiplets (broad interest)	Business model adoption			
Integration	RF + digital	Separate solutions (e.g., SHIP)	RF + FPGA/GPU/CPU in production			
	3D	HBM, 3D layered NAND	True HI in 3D			
	Photonics	R&D (e.g. DARPA PIPES)				
Reliability	HI standards	DoD discussions	Power (GaN) & high V			
	Rework / redundancy	Custom solutions	Strategy based on standard analysis			
Supply Chain	Components	International ad hoc	"Zero trust" solutions			
	Assembly	US-only, lagging and/or proprietary tech	On-shore HVM-like interposers, FOWLP	Flow accommodates any volume, price, TAT		
	Security	Trusted facilities	"Zero trust" (data-based; need metrics)			
	Obsolescence	Lifetime buys				

Figure 10: The first version (Rev 0.1) of the HIR A&D Roadmap is qualitative at the start. The A&D TWG will seek inputs to populate it further in the 2021 edition of the HIR.

in the form of a National Manufacturing Institute. This is where the HIR could help frame what is needed there, and we expect to explore this collaboration in 2021. An additional point is the broad reach of the investments—DARPA, NSF, Department of Energy, and Department of Commerce. That is an indicator that these manufacturing needs are not just for defense purposes. National security in electronics reaches beyond those traditional defense-specific requirements.

3. HI Roadmap A&D Status

The 2019 version of the HIR A&D Chapter provides a landscape of HI in defense electronics, with a focus on government programs driving much of the progress to date. Moving forward, the A&D TWG will continue to gather data and add to the chapter for the 2021 version.

Figure 10 is the first high-level roadmap table for HIR A&D. This is more qualitative than quantitative at this point, but we expect that to evolve somewhat as we drill down with more specifics. There will also be links to other HIR chapters with more details on certain topics, such as photonics, thermal management, and 3D interconnect. The A&D TWG will work on gathering inputs for the Rev 1.0 version that will appear in the 2021 update. People interested in contributing to this effort should contact the author or Dr. Tim Lee at Boeing, the other co-chair of the A&D TWG. **SMT007**

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Jeff Demmin is a semiconductor and defense project manager at Keysight Technologies, as well as the co-chair of the HIR Aerospace and Defense Technical Working Group.

MilAero007 Highlights

Defense Speak Interpreted: Unpacking the NDAA ▶

What is this NDAA stuff you keep hearing on the national news all the time, and why is it important to PCBs? Denny Fritz explains what is going on with the National Defense Authorization Act, which authorizes programs and lays out the priorities and policies for the U.S. Department of Defense.

Just Ask Joe: The Land Warrior Project ▶

Inventor, columnist, instructor, and founder of Verdant Electronics, Joe Fjelstad has been involved with rigid PCBs and flexible circuits for decades, and he's ready to share some of his knowledge with our readers.

Beat the Heat With New Book on Thermal Management Design Processes ▶

Learn how to beat the heat in your designs with *The Printed Circuit Designer's Guide to… Thermal Management: A Fabricator's Perspective*—the latest title in the I-Connect007 educational library.

AVX Supplies the First ESCC QPL Approved Polymer Electrolytic Multianode Capacitors ▶

AVX Corporation—a manufacturer and supplier of advanced electronic components and interconnect, sensor, control, and antenna solutions—is the first manufacturer qualified to supply polymer electrolytic multianode capacitors for use in European Space Agency (ESA) programs.

New BAE Systems Aircraft Power Sources Clear Path to Electric Flight ▶

We need smarter, cleaner travel now more than ever. Greenhouse gases are on the rise, and populations are growing at a rapid pace. This has cities turning to cleaner forms of public transportation on the ground, in the water, and—soon enough—in the air. The first of these next-generation electric flights are set to take off in just a few years with urban air mobility aircraft.

NASA to Highlight Artemis Booster Test with Live Broadcast ▶

NASA was scheduled to broadcast a Space Launch System rocket full-scale booster test at 2:40 p.m. EDT Wednesday, September 2, on NASA Television and the agency's website, followed by a media teleconference.

Sanmina Bolsters Backplane Testing Capabilities in California and Mexico ▶

Sanmina Corporation, an integrated manufacturing solutions company, announced that it bolstered its backplane testing capabilities with new technology from RoBAT, a provider of automated testing solutions.

Boeing, Salt River Project Sign Renewable Energy Agreement for Mesa Site ▶

Boeing and the Salt River Project (SRP) utility signed a multi-year agreement to power Boeing's Mesa site with renewable solar energy.

300 Below Selected as Top Team for U.S. Air Force Manufacturing Olympics ▶

300 Below Inc., recipient of 2019's Innovation of the Year in Manufacturing Technology, was announced as one of the top 92 participating teams selected from across the globe competing in AFWERX's Base of the Future Challenge, as a catalyst for fostering innovation within the U.S. Air Force by using its technology to triple the life of at-risk metals for ~20% cost of the item.

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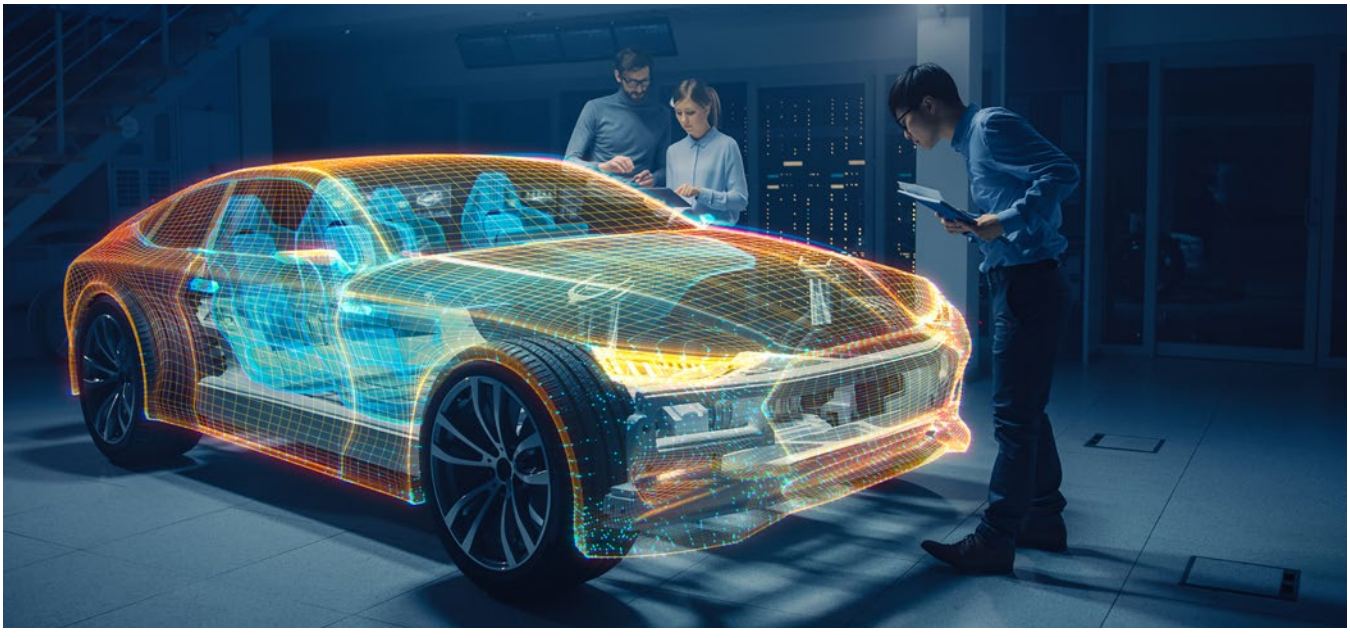

The HIR Hits the Road With the Automotive TWG

Feature Interview by the I-Connect007 Editorial Team

Nolan Johnson and Andy Shaughnessy met with Rich Rice of Advanced Semiconductor Engineering to discuss the automotive chapter of the IEEE HIR. Rich describes how the automotive technical working group (TWG) put together the chapter, including what they found to be critical for the automotive segment.

Nolan Johnson: First, tell us about your background and involvement with the automotive chapter of the HIR.

Rich Rice: My current job is with Advanced Semiconductor Engineering (ASE). I worked on the packaging assembly and test side for 17 years. Before that, I worked at Amkor, National Semiconductor, and a couple of other gigs. Primarily, my background has been in IC packaging. I'm involved with the automotive TWG.

Johnson: Automotive is a big market driver for PCBs. Perhaps you could give us an overview of the automotive chapter, as well as some observations or analysis. For example, what are the key factors of interest to the PCB manufacturing community?

Rice: When it applies to the circuit board industry, it's probably more inference than a direct reference in our chapter because we talk mostly about semiconductor packaging and its derivatives, which could be considered system in package (SiP).

Johnson: One of the things that struck me, for example, is the discussion about interposer design, which is rather new to the semiconductor segment. It's a sort of PCB inside the package.

Rice: To a certain extent, yes. But it's super high density. It's almost silicon scaling level or at least silicon back-end metal scaling.

Johnson: That raised the question for me whether there is a lateral career opportunity for a PCB designer. What are the interactions here?

Rice: In general, the electronic architectures in automobiles are changing because of a couple of things. One is the increase in autonomy, or at least partial autonomy, being designed into

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cars through sensors and increased data intake. Those sensors produce a lot of data. You're using computers to make decisions about what the car sees, if not eventually what the car does. There are a lot of architectural changes that are happening in the automobile. As a result, PCBs are going to get more complex.

Johnson: While they're getting more complex, it's also true that automotive as an industry is driving PCB manufacturing to do two things at the same time. One is to get two orders of magnitude more field reliability and accuracy than we currently produce in the PCB fabrication industry and as much as two orders of magnitude more volume. Those two things often go in opposite directions. While things get more complex and smaller dimension size to fit these things into a mobile platform and better handle environmental extremes, all of this is going on, and there are a lot of dynamics for the PCB fabricators, which circles back to around to why this is a great conversation for us to have.

Rice: The second part of what I see as a big driver is the electrification of cars in general and electric drives. All of the electrification drives circuits for motors, which drive the car, as well as the tons of different fans and other things for cooling. Those items are going to drive up a lot of semiconductor, electronic, and PCB content.

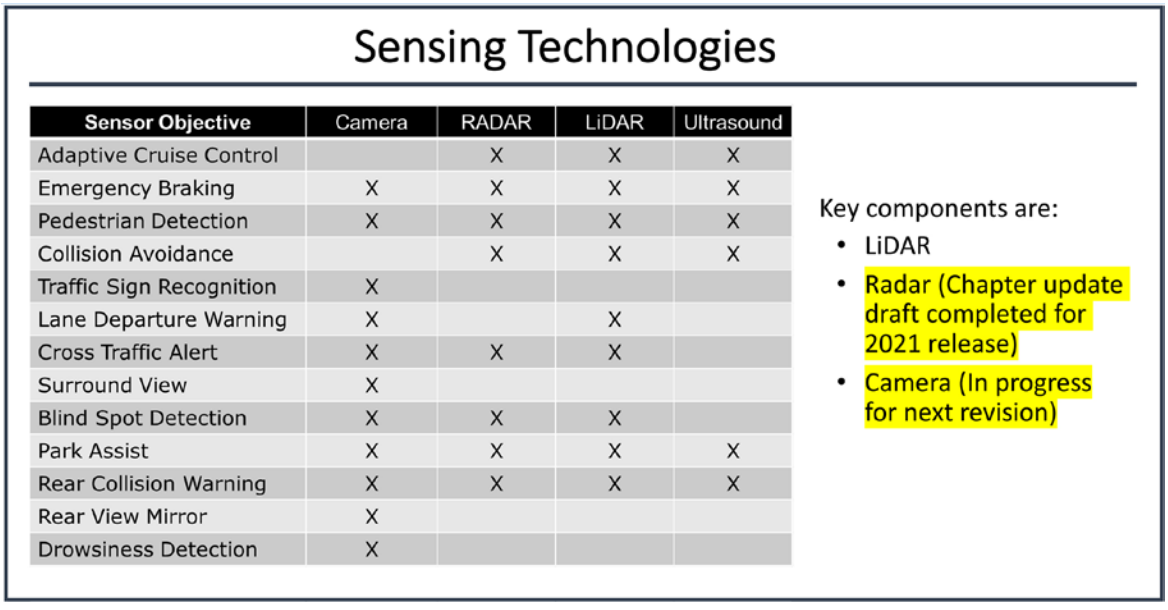
Andy Shaughnessy: I'm curious about the approach to writing the chapter. A whole group contributed to this automotive chapter. It sounds like you had a lot to tackle, especially to get down into the vehicle to vehicle communications. A lot of it has to do with sensors to make all this work.

Rice: Urmi Ray worked with a different co-chair to start this process. I caught the ship while it was moving already, but I know how we got here. Our process was first to look at all the areas in the automobile. There are a lot of reports available that talk about how automation and electrification of cars are going to increase semiconductor content. Then, we identified the areas that will require a lot of semiconductor content and innovation to achieve particular long-term goals that the automotive industry wants to tackle. For instance, in the area of autonomy, it's going to require a huge computing resource and a data-crunching resource. And it's also going to require a certain level of conductivity and data communication.

We tackle those couple areas by looking at the communication processes or roadmaps to understand the differences between computing or mobile applications, or maybe cellphones, versus what automotive is going to require. Of course, we had to delve into not only high-performance computing and how to deliver it in an environment that's not in a data center or your office. It's a mobile platform that's exposed to temperature excursions and humidity. It has to be robust and reliable, and it has to last longer than your home computer laptop.

We researched those areas, and sensors are an important part. We saw that radar continues to evolve. We didn't have radar in the first revision of our chapter, but the second revision—which we're working on basically as we speak—will have a pretty large section as far as radar systems and how they're evolving. LIDAR is something that's on a future roadmap. We have a work group member from Velodyne, for instance, who is a developer and provider of LiDAR. We get their perspective as a contributor to the chapter. On the electrification front, if you look at all the power circuits out in the world, about 50% of them go into cars. The other 50% supports all other applications, including industrial, home appliances, etc.

Automotive represents a big power requirement that is only going to get bigger as the penetration of electric cars goes from 4% of all cars today to the projection that by 2030 fully 50% of all cars will have some type of electric drive in them. That might be a hybrid electric vehicle, but they'll still have an electric drive. We're relying on the power group in the HIR to also provide a lot of insight on things like wide bandgap materials, such as silicon carbide and gallium nitride, that allow power transistors to function faster and more efficiently. We've had to just look at those different areas where we



thought where development was needed, and we focused on that.

Shaughnessy: When did you start working on this?

Rice: The latest edition of the International Technology Roadmap for Semiconductors (ITRS) was in 2014, and a lot of it had to do with the semiconductor fab side of things. That's when Bill Chen and Bill Bottoms decided to lead this effort to create the packaging portion of this current HIR roadmap. As semiconductor technology started to become less available to the mass market because the expense of fabs was going way up, only the richest companies could really afford it. Everyone saw that packaging would be increasingly used to integrate the various IP blocks inside of a subsystem. It's not just the integration on a PCB; it's driving it closer and closer in proximity inside a package.

Johnson: What can you tell us about your presentation?

Rice: Urmi Ray and I are co-chairs. We have contributors from Intel, Bosch, Fraunhofer, as well as Frank Bertini for Velodyne, Professor Yu from Arizona State, and Klaus Pressel from Infineon. Our new members are Veer from NXP, Vikas also from ASE, and Andreas Grassmann from Infineon. You can see it's very focused around semiconductor to a certain extent, and there's a little bit into the Tier 1 area like with Bosch. That's the scope of the inputs we've received so far.

Our chapter is organized into five sections. It's connectivity and communications, in addition to the processor roadmap, which includes ADAS, infotainment, MCU, and autonomous driving sensors. It's really three main areas: functional safety, reliability—which the people from Bosch did a great job at contributing—and electric powertrain. This is what I talked about before as far as the growth drivers, autonomous driving, or ADAS systems, as well as powertrain and electrification of the powertrain specifically.

Regarding our executive summary, it's a high-growth market. We're all interested in it. Autonomous driving and electric powertrain are causing a lot of disruption for system architecture and even the physical drive architecture of the car going from internal combustion to electric powertrains.

As we've talked about what impacts the system architecture, we've also introduced highly complex packaging for processors because the speed at which some of the new fab nodes that are coming in is unprecedented in the acceptance in automotive systems. Typically, they wanted to see fab notes that were mature and completely wrung out from a reliability standpoint.

Now, because of the processing challenges, you see much more of an open mind

to introducing not only 28-, 20-, and 14-nanometer technologies, but even seven-nanometer technology. TSMC just had their technology symposium last week and talked about getting their seven-nanometer qualified for automotive applications. That's a big driver. There has been a lot of talk about advanced communications and 5G coming into cars. We're going to have to require all these data communications with extremely low latency.


Rich Rice

In recent months, there has been some rethinking about that. However, a lot of the processing for autonomy and decision making really is going to be centered inside the car with a little less burden on the outgoing and incoming communications; it's still going to be an important part of the overall architecture. Then, there are high levels of reliability on all components. The sensors are changing, and the powertrain electrification, especially in high voltage management, is a big part of dealing with these power transistors. On the processor roadmap, you can see some of these as you look out forward in the 5-, 10-, and 15-year horizon. Part of the HIR roadmap is we want to go out 15 years and get out into the pre-competitive area to set some vision for what people need to develop.

Typically, we see wire bond and some flip-chip today, such as flip-chip with the heat spreader and automotive applications. As we go forward, there's going to be a lot of SIP or multi-chip integration. There's also going to be a very high-density integration platform that integrates these chips together that require high speed and high data interconnects between the chips, silicon interposer, etc. And then longer term, we even see the potential for optical I/O inside of these heavy-duty processors that go into these automotive applications. With the silicon nodes, we might even put seven-nanometer over in the five- to seven-year horizon. Five-nanometer might go out because we see a huge acceleration in the use of silicon nodes inside the automotive applications.

These are all the various different attributes of the interconnect inside the package that gets finer and finer as you go along. As you go out, there's more and more functional integration inside the package. Onto sensing technologies, there's a lot of different sensors, but if you take a look at all of these different types of sensors, they typically use four different types of technology. Seamless image sensors, radar sensors, or ultrasounds are very common for close quarters, like backup sensors and things like that in cars. We don't see much development going on in the ultrasound area, but we do see a lot of development going on in these first three. Our first chapter included LiDAR. We just mentioned radar and camera, but we've had a pretty significant contribution to radar. Our next update is going to include radar and a more extensive discussion on the camera side of things.

On the reliability side, that is an overreaching thing for automotive applications; sometimes, it changes the physical architecture of a package if you compare it to lower reliability requirements for cellphones or laptops. This section was contributed by our friends from Bosch; they had a lot of good inputs on various different attributes of how you designed for reliability, including much more extensive use requirements of FMEA, physics of failure, and even things like data fusion for health assessments and then digital twins. A lot of that reliability had to do with upfront modeling and analysis of what you're designing before you even make something physical out of it.

On the electrification side, there are a lot of different applications. I referred to that before—things as simple as compressors and electric steering. There are very high voltages used for the drive motors, but then there are intermediate voltages, like 48 volts, used for a lot of the other circuitry and smaller motors inside the car.

When you deal with conversion, you need converters and PCB technology to platform all of that. As you get up into the higher kilowatt areas, you have a hybrid electric inverter and the fully electric drive motors for electric vehicles. We make the statement that the primary impact will be on batteries because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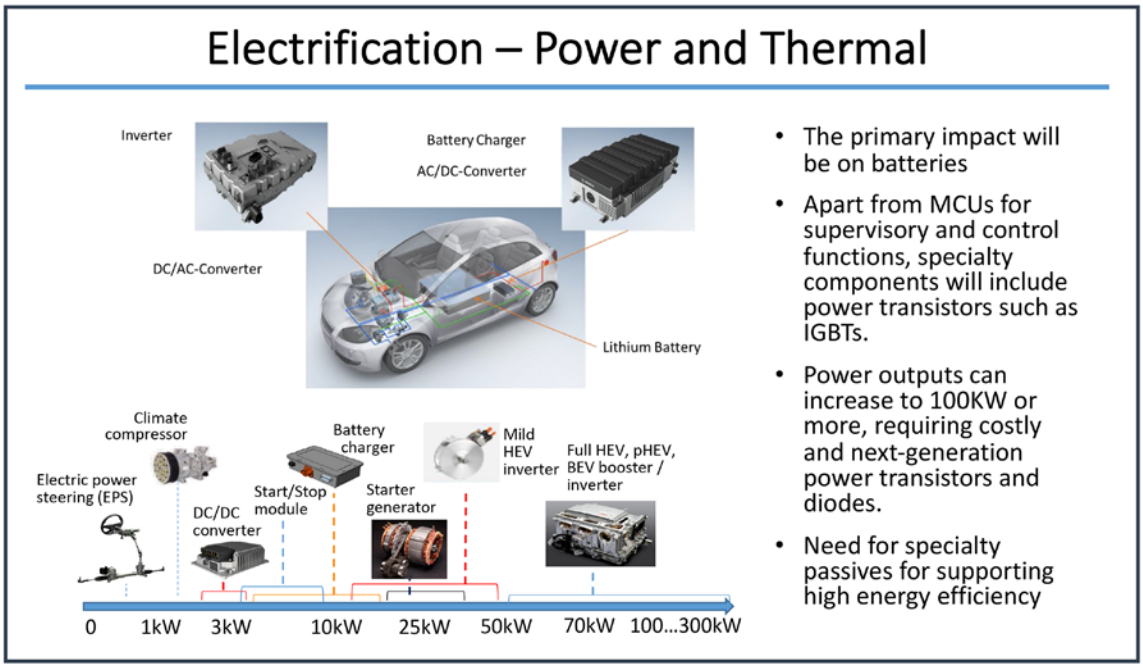

that's probably the case. Batteries are not necessarily semiconductor packaging attributes. We don't really cover that. We'll increase our content on this going forward, and we're going to leverage what the power people do in their section of the HIR roadmap in a different chapter.

Overall, we collaborate with people from other chapters, such as power and security, for when we get into things like vehicle-to-vehicle communications and general outside communications going in and out of the car. Security is a huge issue, and we do have a pretty nice writeup on that already. We also collaborate with the people who wrote about sensors because there are so many in cars: pressure sensors, motion sensors, and crash or g-force sensors for collision and setting off airbags. However, in our section, we focus on things that are critical to the car.

Internet of things (IoT) is really about how the car communicates with the outside world. We've had some communication with them, but not a whole lot so far. The automotive supply chain is very different than most of the others in the world. I could probably talk about the automotive supply chain over another 25 pages, and I don't want to do that. I'm trying to convince the supply chain people to do it.

The automotive chapter is unique; it's designed for robustness and reliability. It's not designed to move quickly. The automotive supply chain is being challenged right now. You have automakers that are jumping over Tier 1s and making relationships directly with semiconductor companies so that they can get a head start on some of the autonomous capabilities that they need to integrate into their cars over the next few years. You've seen the effort companies like Google have put into this, and their approach is completely different as well.

The supply chain is going to be under forced change as we go forward in quite a few different ways. For our planned revisions, we're adding content for radar and camera. We're cross-referencing with power people. We're going to update and refresh our marketing information, and we're also going to be reading through the other technical working group chapter areas for enhancements.

That's why we do this. We want to generate more interest in it and exposure about it. We love it when people challenge our ideas because then we say, "Okay, maybe you can contribute."

Johnson: Rich, this has been awesome. Thank you.

Rice: Thanks. Take care. SMT007

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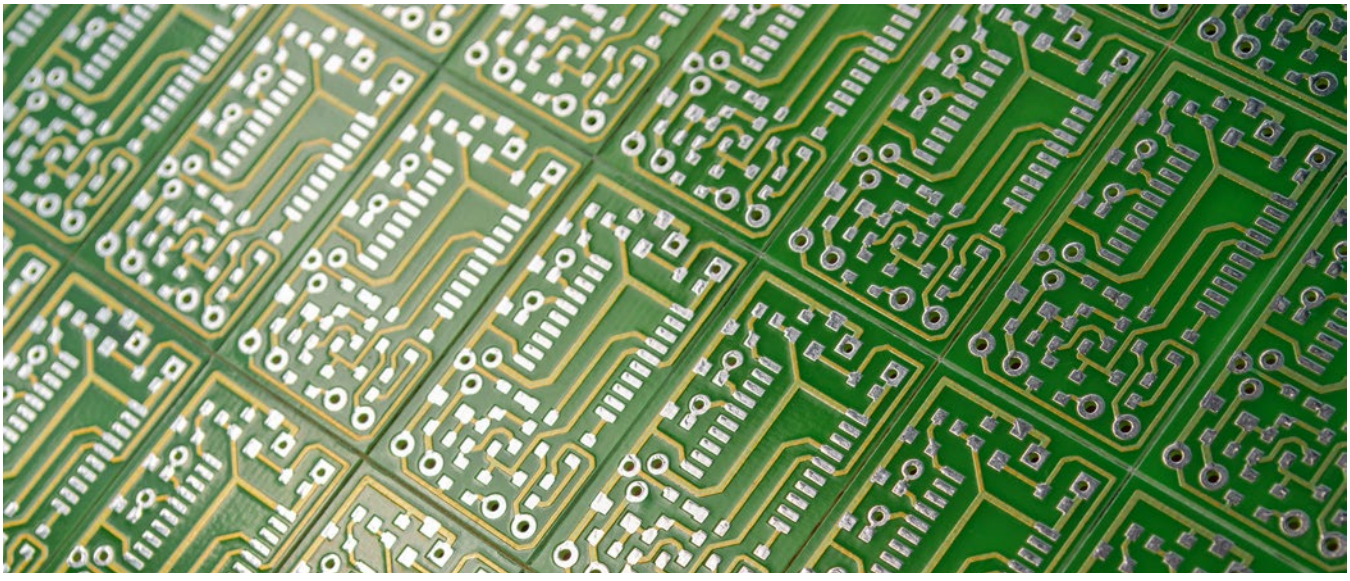

Monsoon Solutions: Achieve Greatest Reliability With Optimized Panelization, Part 2

Interview by the I-Connect007 Editorial Team

In the first part of this conversation, "Monsoon Solutions: Achieve Greatest Reliability With Optimized Panelization, Part 1," Nolan Johnson and Andy Shaughnessy spoke with Jennifer Kolar and Dan Warren of Monsoon Solutions about common issues that designers should think about when they're panelizing their designs for reliability. In Part 2, the conversation turns to best practices for putting multiple board designs on the same panel.

Nolan Johnson: Let's talk about one of the other bugaboos: Jamming in as many different boards as you can.

Jennifer Kolar: We hear this a lot when we have customers that are doing small test boards, such as a series of them or variants of them. They know it's not going to use up a whole panel, and they don't need that many, or they always need them together. They're the same stackup, so they think it will be a lot cheaper and more efficient, and just send them to the fab shop to deal with. The problem is the way most assemblers work—if they're working off pick-and-place data or the origin in ODB, that's based on your board data. If you send individual board data to the fab vendor, and they now panelize two together, then there's no correct XY data or origin location for the assembler to use to program how to assemble that array. They're going to have to scan it themselves and try to recreate that data, which is a time-intensive process.

When we do multiple designs per board, we will put them in the same database, and we will output them together so that we don't have conflicts on reference designators. Otherwise, if you are not careful, you end up with two different designs with two different R1s that are different parts. That's a really big problem in programming. You can also end up with so many different kinds of designs that the programming is really complicated, even if it is within one database. We'll try to reduce or minimize just how many different designs go into one database because it makes the programming so much more complicated. If we do have people who want to put multiple boards in one, rather than having the fab vendor panelize them together, we do that first. We'll put it in one database, panelize it, and then send

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it as a single design to the fab shop. When the assembler gets it, all the pick-and-place data will be correct, the origins will all be correct, and we'll make sure none of the reference designators overlap.

That's one thing we often have to regularly educate our customers on—especially if they've worked with the cheaper bucket shops—because they know they're all getting built, thrown onto a common panel, and cut out. If you're hand assembling, you're fine. If you're getting a board that's not an array and it's one up, it doesn't matter. If you need the rails and panel, then that's something that you really want to think about. You could have the fab shop combine the Gerbers. They can do that, but unless they're rerouting them back out as individual subpanels, so that when they go to assembly the origin and XY data match, you're better off merging it yourself because your assemblers are going to have something that they have no easy way to program.

Jennifer Kolar

Dan Warren: From a company standpoint, Jen just summed up everything really well. In my personal opinion, just don't do it. There are so many hassles in doing it. I'm very old school when it comes to this. There should be one board and one database. It's easier to manage the revisions and data. If you want to make a change to one, you don't have to make a change to both and fab them together. At Monsoon, I do whatever the customer wants. If they want 30 boards in a panel, I'll do it. I'll advise them not to, but I'll do it. In many places I've worked, it was just a hard no.

Kolar: People don't think about the fact that if we are combining them in one database, then we have to merge the schematics, too. We must have no conflicts between any reference designators or net names. Put these all together. Throw them all on the same board. You don't think about the fact they have to make the schematic properly associated with that. What I tend to encourage people to do, when they're really set on trying to save money building a few of each one, is to work with your fab vendor. Have them be independent databases. If it's the same stackup, the fab vendor can put multiple different sub-arrays on their overall working panel. You could have one array of board A, an array of board B, an array of board C, and your fab vendor knows how to optimize for that. Let them do what they're good at and make decisions on how to make it the most cost-effective.

Warren: That would be a much better way to do it.

Kolar: Assembly is such a painful time for a mistake to be found. We do so many manufacturing jobs, and in a lot of cases, we didn't necessarily do the design for them. We're finding out last minute if a part wasn't fully specified in the BOM, or it's not specified in the schematic, so you end up with the wrong one. One issue in assembly that commonly happens will be an engineer edited the schematic, but they may have changed the value of a part in the schematic and didn't change the entire symbol, so the BOM is still incorrect. A mismatch between a manufacturer part number and value happens all the time. We try to catch those while kitting, but if missed, you find those out in assembly.

From the project management perspective, assembly is where we lose time even more so than with fab questions. The machines are loaded, the assembler can't touch another board while their assembly line is loaded with this design, and you can count on the fact that it's going to be at least a day to mail them something else or order it. It's not, "Let me think about this and get you new data." You need physical things. Depending on how much time you have, they might not be able to just

keep it on the line for you. They may have to take it off, reprogram it, and pay a new setup fee. Now, you have these parts that have been loaded and unloaded, and you've lost whatever parts were on the lead tape that was loaded, so maybe you don't have enough spare parts anymore.

We also have customers who want to do their own kitting. That's when we either end up with mounds of individual little chunks of cut tape or an exact number. We beg them and beg them to let us do kitting because that will screw them in assembly.

Dan Warren

Johnson: For those who see themselves in what you just described—when they do finally let you do the kitting—you then do what?

Kolar: A good rule of thumb we use is if something is going through a pick-and-place machine—unless it's a really expensive part—we want to make sure there's a six-inch lead on the tape; how many components that is will vary by part. If it's an 0201, that might be about a hundred parts; if it's an 0402, maybe 70 is enough. You need to plan for a mechanical six-inch lead to go through and know that you're going to lose those parts. If they're really expensive parts, you can get away with fewer. We like to ideally do at least 3% over. If parts get really expensive or are hard to acquire, they may only get one over, or they may get none over. We make sure the assembler is aware in advance of those rare parts. People like to think that reusing kits saves a lot of money, but you spend more time digging back through those old kits. It's worth it for expensive parts. It's not worth it for passives.

The other thing I've seen people not think about when they send kits to assemblers is when you're building multiple boards at once and they share the same components, it's an issue if you send them on a single reel. That reel is trapped to one build at a time. If they have multiple assembly lines, unless they cut off from it as cut tape, you're trapping them. We do a lot of projects where we build subtle variants of boards where some things are populated, and some aren't, based on the availability of parts or based on experiments. It's tempting when you're ordering cut tape to say this board needs 20, and this needs 20, so I need 40, and let me maybe order 60 on one tape. Again, that's tempting to do if you expect the assembler to deal with it, and you send them one kit for two boards. Unless they're going to run them one after the other, you have an issue. If you want to run them at the same time, they have to go through and split all those up, and you need to realize they're not going to have enough excess for all of the parts.

That's typically where we're paying attention strategically to how they will run. Even if there's a lot of shared parts, we're kitting them separately. We're ordering them independently and kitting them as completely separate kits. It makes our assembler's lives a lot easier, and it gets things through a lot more quickly. We have to balance the cost benefit vs. the potential time delay of sharing parts.

Johnson: We just keep bumping up against the theme that designers have much more decision-making power than they realize.

Kolar: Yes, and they need to be willing to push back on the customer. It is also important to take the time to learn what you don't know. When we start new designers, if they haven't been in the industry or they have an EE, they don't know anything about manufacturing. We don't expect them to. They have to learn that somewhere.

Warren: Case in point: We had a designer who had never done board layout before, and he placed 0402 resistors within 0.4 mm of an RJ45

The team at Monsoon Solutions. (Source: msoon.com)

connector, which is rather hard to assemble. There was no DRC error due to how the placement courtyard was defined, but just because you can do it in the tool, doesn't mean you should. Situational awareness is important. I didn't get upset with him; I just took the time to explain to him why we shouldn't do it, why the boundaries are the way they are, and that you should look at IPC documents, etc. It's a good learning opportunity. Unfortunately, a lot of designers are working in a vacuum. I have worked in a couple of places where I was the only designer there. It is really hard to learn from other designers when you're the only one. I've seen a lot of designers get stuck in a past decade because they didn't keep up and keep learning. That's a one-way ticket to losing your job, unfortunately. It falls back on the designer to be assertive enough to ask questions, look for training, and make connections with other designers.

Kolar: To that point, this is something that we're trying to do more and more for designers. If you're working with similar customers, ask for feedback. Say, "How did the build go?" We'll rarely or occasionally get feedback if we didn't do the manufacturing, and we just sent a design package. We might occasionally hear that it went great, or this went great, but they had to rework a couple of things. Typically, you don't get a lot of feedback unless something goes colossally wrong. That would be a really good thing for people who are designers at service bureaus to do: Go back to their customers and ask how it went. Ask, "Were there any issues in fab? Were there any issues in assembly? Give me that feedback so that I can take that into account for the next one."

Johnson: The takeaway is if you're looking to become better at designing reliably, get the feedback from your manufacturers on how the build went.

Kolar: That's a huge part of it. A lot of assemblers and fab shops think by not telling you, they're making your life easier. It's done, so they've moved on to the next thing. They're on the next item. We don't work that way. We need to learn from our vendors to help our customers.

Warren: Take it as constructive feedback. Don't take it personally. Don't get upset because someone told you there was a mistake. Think, "I'll remember not to do that next time." Move on. Everyone will be much better for it. We're all adults, and it's just the way you're supposed to learn.

Johnson: Any parting words or last thoughts before we wrap up?

Warren: I can't stress communication enough. For the fab and assembly shops, just because

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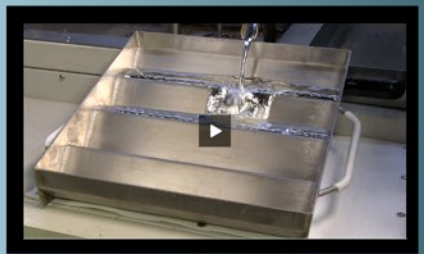

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it's not necessarily your job doesn't mean you shouldn't know it. I don't know all the details of assembly. I've been doing this for a long time, but I have people like Jen and project managers who I lean on. There's still that gap between the two, and I still have to have a general idea of what's going on. If you don't, then you're really setting yourself up for a fail. It may be a year down the road, but you're going to make a huge mistake because you weren't paying attention at some point.

Kolar: A lot of times, our customers provide their own libraries and footprints rather than having us build them. Dan has said that if it's a part that's going to be hard to rework in assembly, he will double check that footprint. He checks a lot of the connectors, as those are common points for mistakes. Even though that's not been asked, we've found a number of issues that way. The board will be useless if this part doesn't work. Take the extra time to check those parts, even if that wasn't asked. That's one of the things Dan has talked about doing on all of his projects that I really appreciate.

Warren: I'm pretty picky about library parts.

Kolar: That's where the most mistakes are when you get to assembly.

Johnson: Not the layout or the placement, but also all the subtleties about footprints and sizing.

Kolar: Don't forget keep-outs. That's where you're really dead in the water if you have the wrong footprint, and on the right one, the part is bigger than what you have on the board, or it's a sensitive part, signal wise, and you can't rework it back in.

Johnson: Thank you for your time.

Warren: Absolutely.

Kolar: You bet. SMT007

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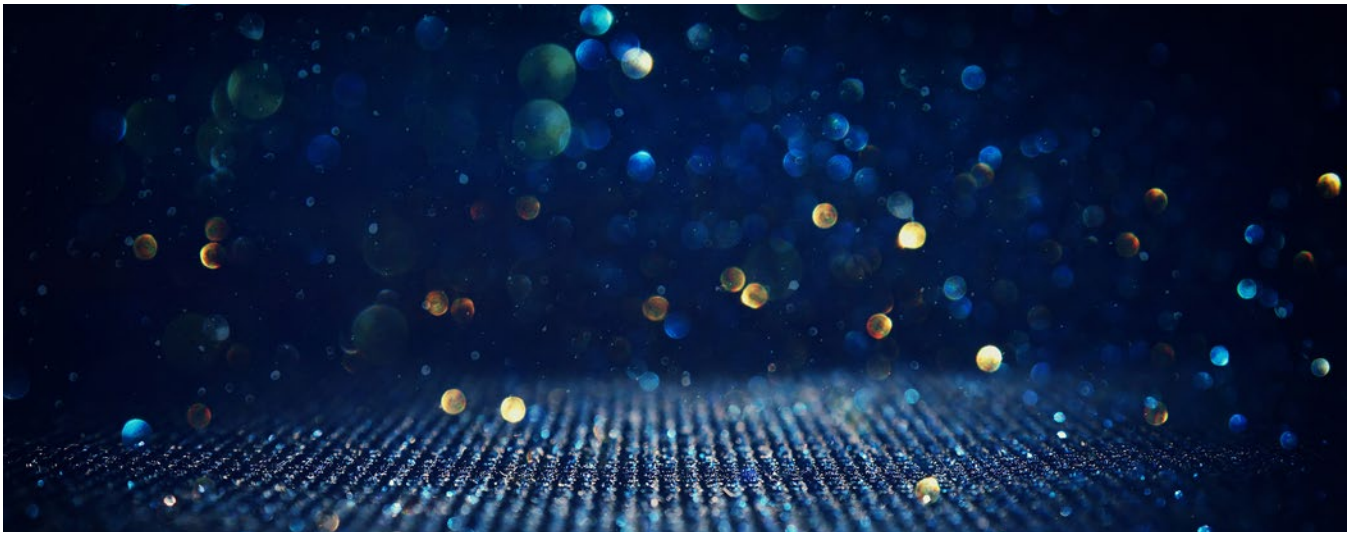

Reducing Flux Splatter in Sensors and Camera Modules

Article by Jasbir Bath, Shantanu Joshi, and Noriyoshi Uchida
KOKI SOLDER AMERICA AND KOKI COMPANY LIMITED

Abstract

With the increased use of electronics in new technology areas, flux formulations are being developed to address the new and existing requirements. For sensors and camera modules used for Advanced Driver Assistance System (ADAS) and internet of things (IoT) applications, there is a demand for no-clean flux formulations in lead-free solder paste, which can reduce flux splattering during reflow.

Development was done on a specially adopted flux chemistry, which helped to reduce solder/flux spattering without the use of a specially developed reflow profile adjustment in an air reflow atmosphere. The flux chemistry in the Sn3Ag0.5Cu solder paste was developed so that the flux residue layer can cover the molten solder surface during reflow preventing splattering.

Tests were done on a copper plate printed with solder paste and a copper plate placed slightly above the reflowing solder paste on the test vehicle to measure flux splattering with a variety of reflow profiles evaluated. While the conventional solder pastes required an increase of the preheat temperature to drive off volatile flux components to reduce splattering, this developed paste successfully prevented the occurrence of the splatter regardless of the type of preheat and reflow profile used. The results of the work will be reported in this article.

Introduction

During surface mount assembly with solder paste, flux splattering may occur during reflow. Flux splattering occurs as flux components disperse when gas is generated, which happens when flux components contained in solder paste dissolve and volatilize and are expelled from the solder (Figure 1).

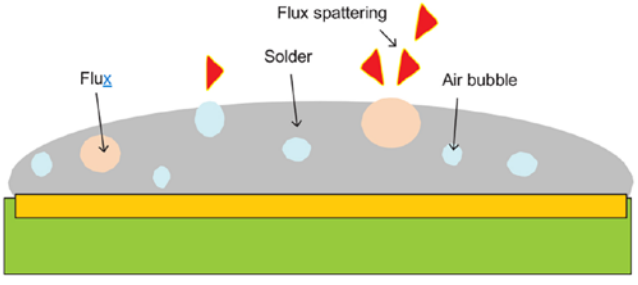

Figure 1: Flux spattering generation behavior.

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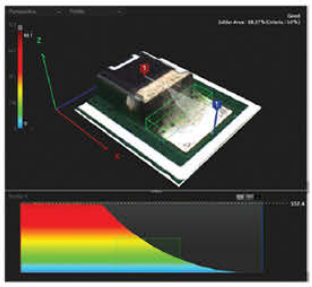

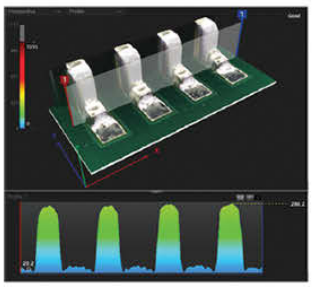

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Flux spattering causes problems, such as the generation of a contact failure, which occurs when flux adheres to the contact point of connectors, as well as illuminance and recognition errors that happen when flux adheres to light-emitting diodes (LEDs), lenses, and sensor components. As a means to prevent splattered flux from adhering to components, some customers use protective tapes to reduce such flux attachment. To lessen these defects and reduce the requirement for protective tapes in these growing applications, solder pastes that do not cause the occurrence of flux splattering are increasingly needed.

This article reports on tests to determine flux splattering generation timing, conditions of the occurrence of splattering which are dependent on reflow profile, and measures to reduce flux splattering through the development of the flux in the solder paste.

Experimental

Flux Splattering With Conventional Lead-Free SnAgCu Solder Paste Using Reflow Simulator

To investigate the splattering of flux, conventional Sn3Ag0.5Cu Type 4 no-clean solder Paste A was evaluated during reflow. The test vehicle was a copper plate of dimension 30-mm x 30-mm x 0.3-mm thickness. The stencil used had a 6.5-mm diameter aperture with a thickness of 0.2-mm thickness. The timing of the occurrence of splattering and the amount of splattered flux were checked using a reflow simulator (Figure 2). As shown in Figure 3, spacers were placed on the copper plate, on which solder paste had been printed, and then

Figure 2: Reflow simulator used for flux splattering timing evaluations.

a glass plate was placed on the spacers 2 mm above the solder paste so that the timing of flux splattering and the amount of splattered flux could be counted.

The splattered flux adhered to the glass plate during reflow in the reflow simulator with the number of flux splatters adhering to the glass counted.

The Occurrence of Spattering by Adjustment of Reflow Profile Using a Reflow Oven

The relationship between the reflow profile and the amount of flux splattering was studied using SnAgCu no-clean Type 4 conventional Paste A. Three different preheat temperatures and times were used corresponding to Profiles A, B, and C (Figure 4). For Profile A, the preheat temperature was 100–200°C for 95 seconds. For Profile B, the preheat tempera-

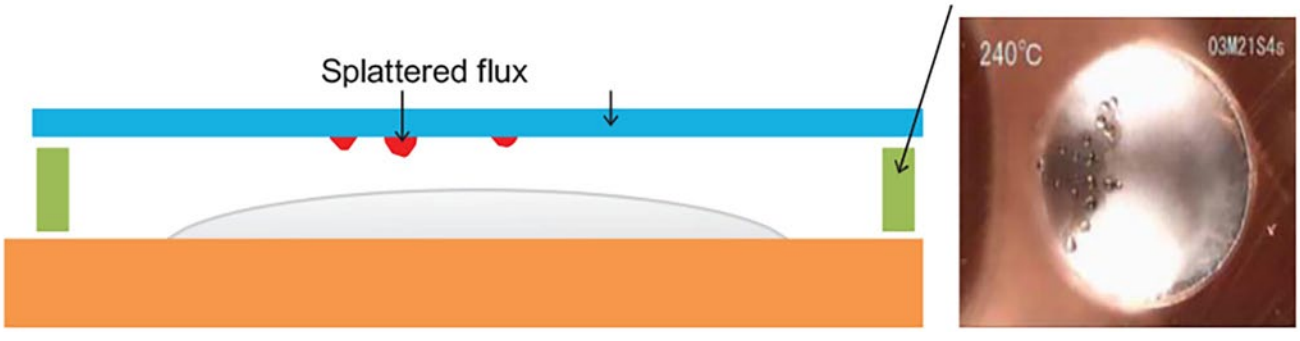


Figure 3: Evaluation method for flux splattering onto a glass plate.

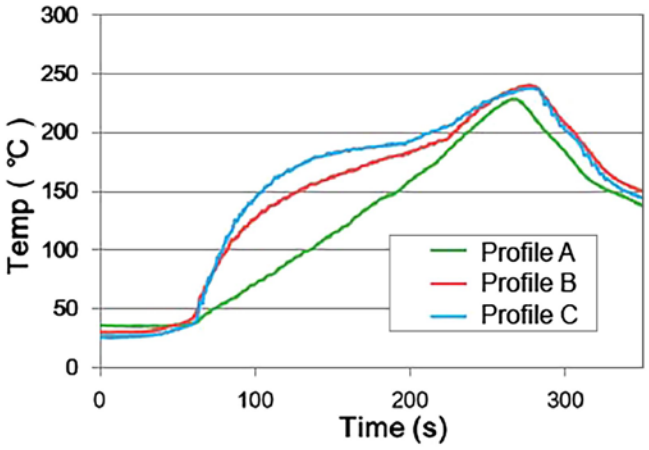


Figure 4: Reflow profiles used.

ture was 150–200°C for 105 seconds. For Profile C, the preheat temperature was 150–205°C for 120 seconds, with time between 180°C and 205°C at 80 seconds. All profiles were run in air atmosphere. In addition, for Profile B, a nitrogen atmosphere (1000ppm O_2) was also used to evaluate the difference in spattering occurrence by variation of the reflow atmosphere.

The Occurrence of Flux Splattering Based on the Variation of Stencil Thickness in the Reflow Oven

The occurrence of flux splattering on the copper plate using conventional Sn3Ag0.5Cu no-clean Type 4 Paste A based on different stencil thicknesses of 0.1 mm, 0.15 mm, and 0.2 mm were investigated using Profile B in air reflow atmosphere. The stencil aperture opening was 6.5-mm diameter.

Developed Paste Product C Flux Splattering Evaluation Using the Reflow Oven and Simulator

A new Paste Product C was developed to reduce flux splattering [1]. Type 4 lead-free Sn3Ag0.5Cu Paste Product C was compared to the conventional no-clean Type 4 Paste Products A and B, using Profiles A, B, and C in the air reflow atmosphere in the eight-heat-zone production reflow oven. Also, the reflow simulator was used to compare the flux splattering behavior of the Paste Product C versus conventional Paste Product A.

Additional Testing of Paste Product C

In addition to the flux splattering tests, tests were done with Paste Product C to understand its general printing and reflow performance in production. Testing included continuous paste printing tests on a company test vehicle on 0.4-mm pitch QFP board pads.

For the printing evaluations for the 0.4-mm pitch QFP, the board pads were 0.2 mm in width and 1.5 mm in length with the distance between pads at 0.2 mm. The thickness of the laser-cut stencil was 0.12 mm. The production printer speed was 40 mm/sec. The paste was inspected at time zero and after 200 print strokes.

For meltability testing, evaluations were conducted on the company test vehicle (Figure 5) on 0.25-mm diameter CSP board pads and 0603 pure tin-coated chip resistor components

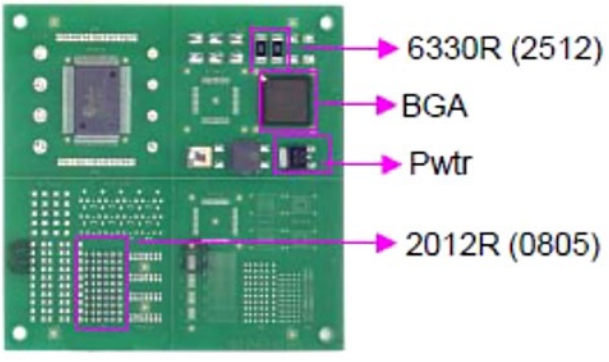


Figure 5: Company test vehicle used for additional testing on Paste Product C.

reflowed using Profile A in air atmosphere on boards with ENIG board surface finish. For reflow/voiding assessment, the evaluations were conducted on the same test board on pure tin-coated power transistor (BTC/QFN), pure tin-coated 6330 resistor, and 1-mm pitch Sn3Ag0.5Cu BGA components in air atmosphere using Profile A.

Results and Discussion

Timing of the Occurrence of Flux Splattering Using the Reflow Simulator Equipment

It was confirmed that splattering rarely occurs during preheating and occurs mainly

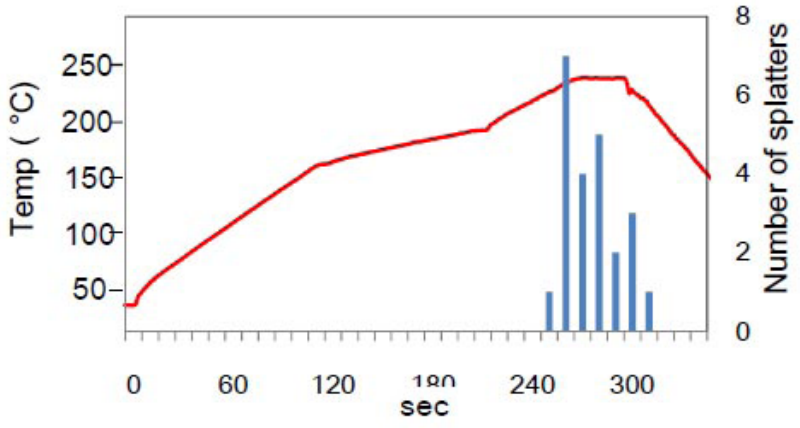


Figure 6: Timing of occurrence of splattering mainly occurring after the solder is molten.

after the solder is molten using the reflow simulator (Figure 6).

Although components of flux—such as solvents—volatilize during preheating, solder is not yet melted, and space exists between the solder powder. This allows generated gas to be discharged easily; therefore, splattering rarely occurs. In contrast, the number of splatters was the greatest immediately after the melting of the solder. When solder paste melts, solder powder merges together, at which time more flux is incorporated. This flux becomes volatile and is pushed out of the solder. This behavior causes the occurrence of a number of flux splatters (Figure 6).

The Occurrence of Splattering Based on Different Reflow Profiles in the Reflow Oven

The occurrence of splattering on the copper plate was determined using reflow profiles with different preheat conditions in the reflow oven (Figure 7). It was confirmed that by using a higher preheat temperature and time and nitrogen atmosphere, flux splattering could be reduced.

To suppress the occurrence of splattering, it is necessary to increase the volatilization of the volatile substances in solvents during preheating to reduce the remaining volatile substances during proper heating. However, increasing preheating temperature causes the degradation of active flux components during preheating and the increased reoxidation of solder powders and the component terminations and board surface finishes, which can result in the generation of defects during soldering. Hence, it is necessary to have a balance between increasing preheating temperature and the result of increasing soldering defects.

The splattering of solder paste can be suppressed to some extent by changing the reflow profile. However, changing the reflow profile is an issue for customers who may have many assembly lines. In addition to what was previously mentioned, increasing the preheating temperature leads to degradation of the component termination, board surface finish, and solder paste as well as potential warpage of substrates and packages.

The Occurrence of Flux Splattering Based on the Variation of Stencil Thickness in the Reflow Oven

The amount of flux splattering by different stencil thickness was tested using Profile B in the air atmosphere using conventional Sn3Ag0.5Cu no-clean Type 4 Paste A. It was

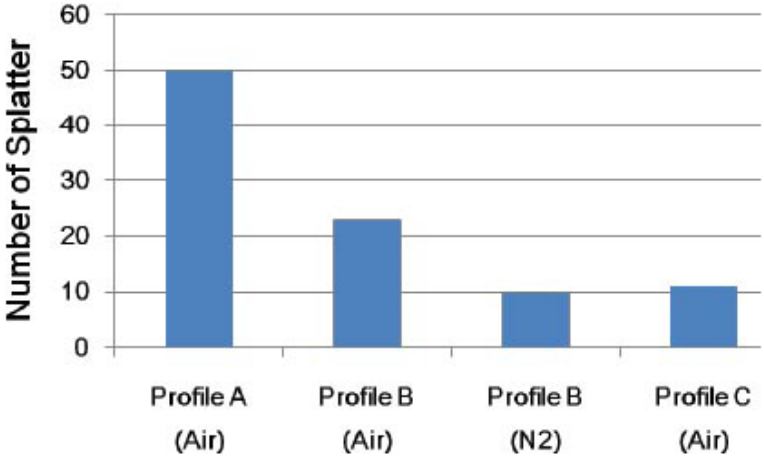


Figure 7: The number of flux splatters based on reflow profile and atmosphere.

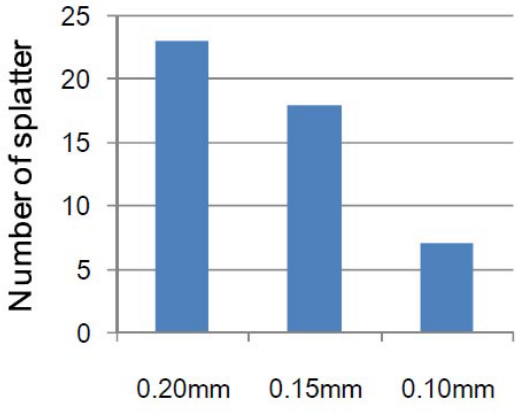


Figure 8: The amount of flux splattering based on the variation of stencil thickness.

observed that flux spattering could be reduced by using a thinner stencil as shown in Figure 8. Reducing the solder paste amount will help to reduce flux splattering, but reduced solder volume may lead to solder joint reliability issues.

Development of Solder Paste to Reduce Flux Splattering (Paste Product C)

Based on the results, a project was initiated to develop solder paste that could suppress flux splattering even when lower preheating temperatures and times were used. From these evaluations, to suppress flux splattering, flux designs that do not leave volatile substances during the melting of solder are needed. It is possible to design resin components, like rosin, and additives that volatilize less during reflow temperatures. However, in solvents with the largest volatilization amount, increasing the volatility by too much causes the progression of volatilization even at room temperature, resulting in many problems, such as the drying of the paste and increased viscosity, which has caused printing and assembly challenges.

We focused on the behavior of the flux residue and worked on how the flux residue can help to suppress flux spattering by developing a new paste material (Paste C) that used a flux system to suppress flux spattering. The solder paste product leaves flux residue on the surface of the molten solder during reflow so that

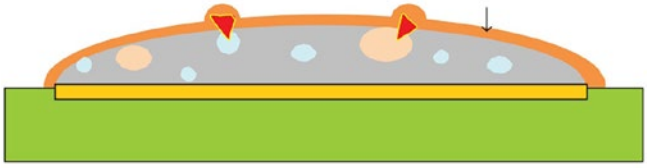


Figure 9: Capping effect by Paste Product C flux residue to reduce flux splattering.

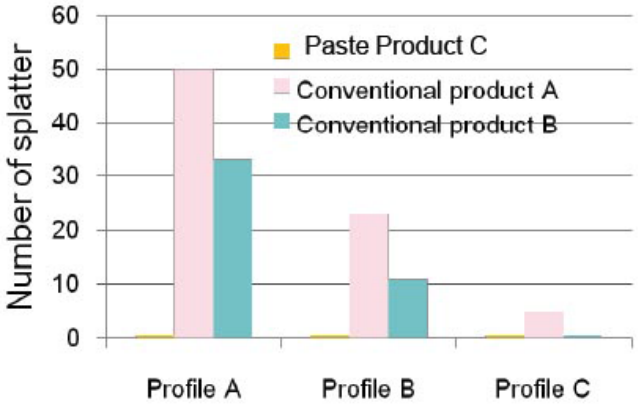


Figure 10: The comparison of flux residue spattering of Paste Product C with conventional Pastes A and B using different reflow profiles.

flux splattering can be prevented even when gas is discharged (by a capping effect) after the melting of solder, instead of suppressing the generation of gas (Figure 9).

As shown in Figure 10, compared with conventional paste products, flux splattering of Paste C was suppressed even when using low preheat temperatures and times, allowing soldering with low flux splattering under a wide variety of reflow conditions.

Figure 11 shows screenshot film images from the reflow simulator using Paste Product C with no flux splattering. Figure 12 shows screenshot film images from the reflow simulator using the conventional no-clean Type 4 Paste Product A as a comparison, showing flux splattering.

Additional Testing of Paste Product C

In addition to the flux splattering tests, Paste Product C was evaluated using various tests to assess its general applicability to electronics manufacturing assembly.

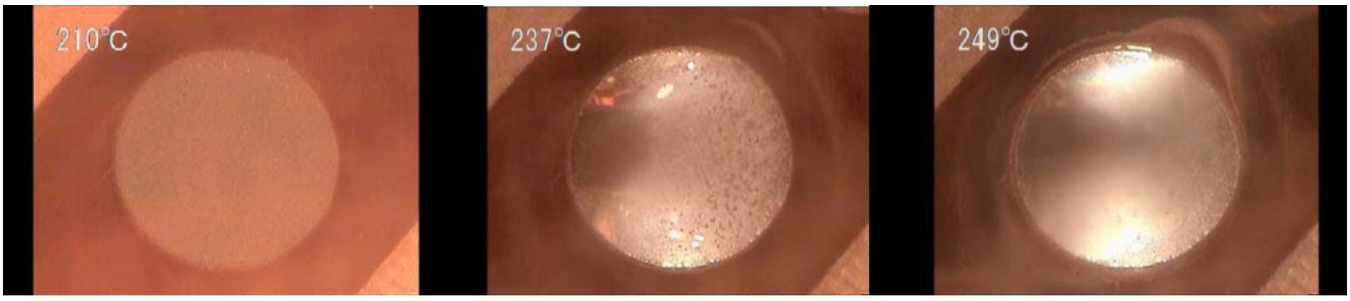


Figure 11: No flux splattering with Type 4 Sn3Ag0.5Cu no-clean Paste Product C using a reflow simulator.

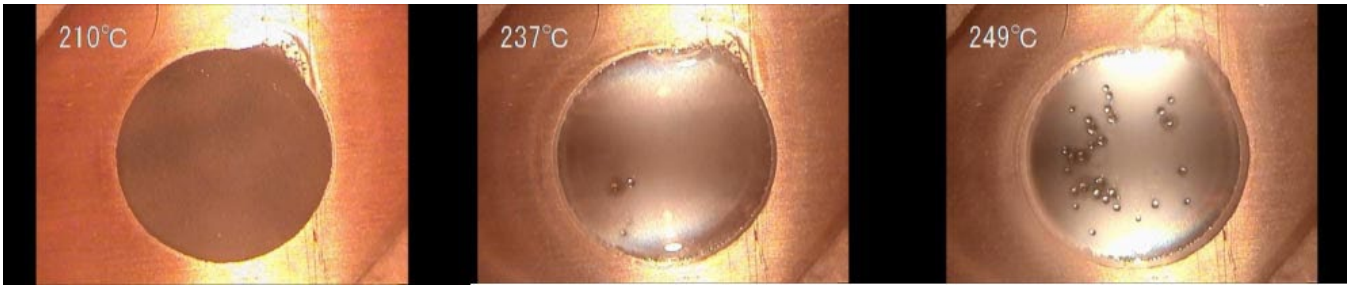


Figure 12: Flux splattering with no-clean Type 4 Sn3Ag0.5Cu conventional Paste Product A using a reflow simulator.

It exhibited stable soldering characteristics, such as printability with the 0.4-mm pitch QFP board pads after 200 print strokes (Figure 13) and good melting properties on the 0.25-mm diameter CSP board pads and the 0603 chip resistor components (Figure 14). In addition, there was found to be low voiding behavior with this solder paste with soldered power transistor/BTC, 6330 chip, and BGA components (Figure 15), allowing its use as a general-purpose solder paste product. It was also found to be an effective solder paste for the assembly of sensor components and camera modules; these application areas are expected to expand in the future.

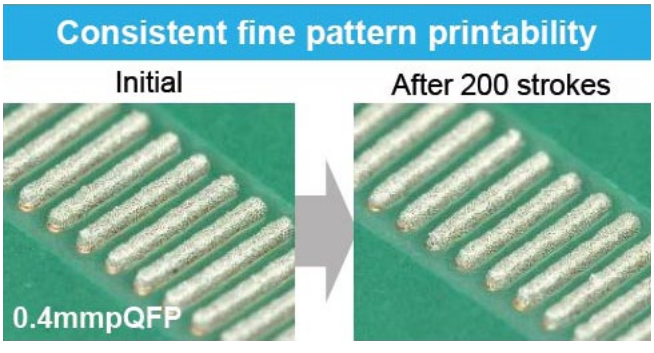


Figure 13: Fine-pitch printing on 0.4-mm pitch QFP board pad (left: initial; right: after 200 print strokes).

Conclusions

This article discussed the mechanism of flux splattering during soldering, preventive measures

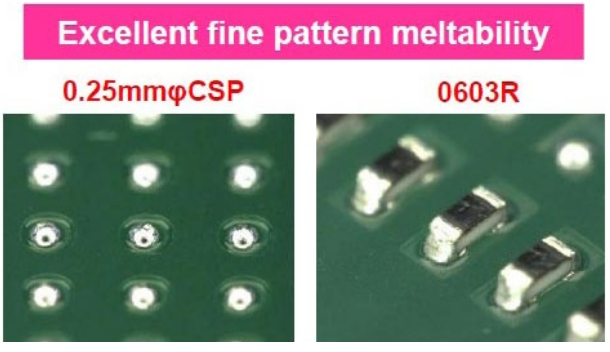


Figure 14: Reflow behavior on 0.25-mm diameter CSP board pads (L) and 0603 chip components (R).

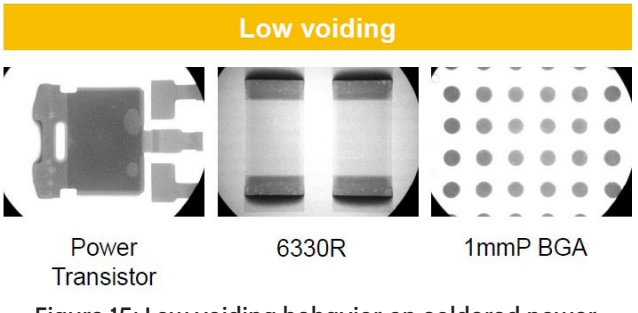


Figure 15: Low voiding behavior on soldered power transistor (L), 6330 chip (center), and 1-mm pitch BGA components (R).

to reduce splattering using reflow profiles, and the development of a solder paste with low splattering occurrence.

Most of the flux splattering in conventional solder paste occurs immediately after the melting of the solder. To suppress flux spattering, increasing preheating temperature and time was effective in reducing volatile components during reflow soldering. But the deterioration of melting property and reduced process window during soldering would be of concern. The work showed that the developed Paste C enables the suppression of flux splattering through a capping effect of flux residue without the need for selecting a different reflow profile, which could cause other issues.

Paste Product C also had good general printing and soldering properties and can be used for sensor and camera modules in ADAS and IoT applications, as well as others. SMT007

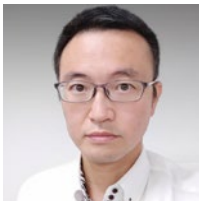
References

1. "Low-Splattering Solder Suppresses Occurrence of Flux Splatter," productronica, AEI, 2017.

Editor's Note: Originally titled "Development of Low Flux Splattering Solder Paste for Sensor and Camera Module Applications" and distributed at the International Conference for Electronics Enabling Technologies in Markham, Ontario, June 5-7, 2018.

Jasbir Bath is a support advisory engineer with Koki Solder America in the San Francisco Bay Area.

Shantanu Joshi is an engineering sales manager with Koki Solder America in Cincinnati, Ohio.



Noriyoshi Uchida is assistant general manager of the Research and Development Division with Koki Company Limited in Tokyo, Japan.

Real Time with... SMTAI: KYZEN

KYZEN Executive Vice President Tom Forsythe shares company updates on stencil cleaning with Nolan Johnson. KYZEN recently announced its newest stencil cleaning product—KYZEN E5631. Forsythe details how the product is best used, as well as the benefits it brings to maximizing stencil life and improving manufacturing yields. (View more at Real Time with... SMTAI 2020 virtual.)

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Electronics Industry News and Market Highlights

NSF Announces MIT-Led Institute for Artificial Intelligence and Fundamental Interactions ▶

The U.S. National Science Foundation announced an investment of more than $100 million to establish five artificial intelligence institutes, each receiving roughly $20 million over five years. One of these, the NSF AI Institute for Artificial Intelligence and Fundamental Interactions, will be led by MIT's Laboratory for Nuclear Science and become the intellectual home of more than 25 physics and AI senior researchers at MIT and Harvard, Northeastern, and Tufts universities.

DuPont Names Lavoisier, Pedersen Award Medalists ▶

DuPont announced it named 12 outstanding scientists as recipients of the Lavoisier Medal of Technical Achievement and the Pedersen Award Medal.

NVIDIA's Three Next-Generation GPUs Excite Consumers ▶

NVIDIA recently announced its next-generation RTX 3000 Series Graphics GPUs, and the stated capabilities are amazing. Dan Feinberg explains how the three new graphics cards are the first consumer-level devices powered by NVIDIA's Ampere architecture.

Qualcomm Small Business Accelerator: From Music Teaching to Cleantech Engineering ▶

Qualcomm Technologies Inc. announced selections for the Qualcomm® Small Business Accelerator Program, which is designed to help small businesses transition to a mobile-first digital work environment to thrive in today's business climate and set-up for success in the long term.

Ethertronics Releases First UWB Antenna Solutions for Samsung Electronics ▶

AVX Corporation—a manufacturer and supplier of advanced electronic components and interconnect, sensor, control, and antenna solutions—announced that its AVX/Ethertronics Korea team completed the development and mass production of the first ultra-wideband antenna solutions to be integrated into Samsung Electronics products.

Panasonic Completes Transfer of Its Semiconductor Business ▶

Panasonic Corporation announced that it completed the previously announced transfer of its semiconductor business to Nuvoton Technology Corporation, a Taiwan-based semiconductor company under the umbrella of Winbond Electronics Corporation group, following the receipt of regulatory approvals.

Keysight's 5G Test Solutions Enable Jabil to Address Demand for 5G Product Validation ▶

Keysight Technologies Inc.—a technology company that helps enterprises, service providers, and governments accelerate innovation to connect and secure the world—announced that Jabil selected Keysight's 5G device test solutions to address the demand for 5G product validation in design and manufacturing.

Sony Delivers Second-Level Cycle Mobile Base Station Control Using Dynamic Spectrum Access Technology ▶

Sony Corporation announced that it had developed Dynamic Spectrum Access technology for the optimized use of radio-frequency resources, achieving fast spectrum assignment and control in a cycle of seconds for the first time.

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Programs for Veterans: A Blackfox Update

Interview by Nolan Johnson
I-CONNECT007

At IPC APEX EXPO 2020, I spoke with Al Dill, president and CEO of Blackfox, about the Evolution Foundation, a nonprofit program to assist veterans with training and assistance into civilian tech jobs. Here, we get an update from Dill, Jahr Turchan, director of veteran services and advanced manufacturing programs, and Sharon Montana-Beard, VP and director of sales and operations, on Blackfox's programs for veterans.

Nolan Johnson: Al, we did an interview at IPC a while back on your program for veterans. Can you give us a quick update on how that's going currently through all of this?

Al Dill: Because of this pandemic, a lot of the program has slowed down quite a bit because of lack of access to the military bases and everyone being cautious about travel and too much movement. We worked with some other veteran-related organizations that are manufacturer organizations, and we're preparing to launch as soon as this loosens up.

We haven't just sat idle here; we are ready. We have good connections at the military bases, particularly in Colorado, and other veteran-affiliated associations that we're ready to turn on. And as I mentioned in the interview, we launched a nonprofit called the Evolution Foundation in that timeframe. It's formed and ready to roll. We have a director overseeing the nonprofit, and its primary goal is to provide monetary resources to help support mostly our veterans in their pursuit of the career.

Jahr, can you talk about our relationship with them and what we've done?

Jahr Turchan: Absolutely. Although we did slow things down a little bit, the executive director of the Evolution Foundation, Jerry Ward, has been very active in seeking strategic partnerships to keep that moving forward. Unfortunately, nonprofit donations have dipped extremely during the COVID-19 pandemic, and what little donations are still coming out of people's pockets are obviously focused as much as

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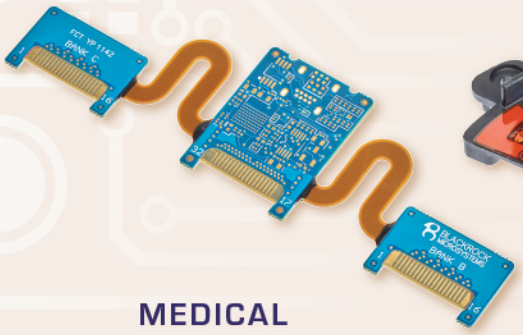

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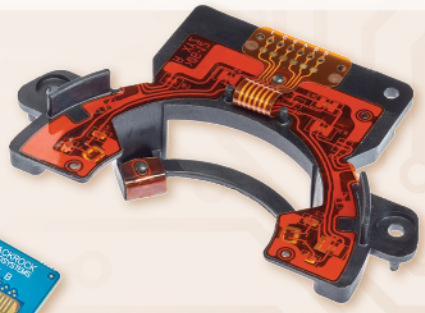

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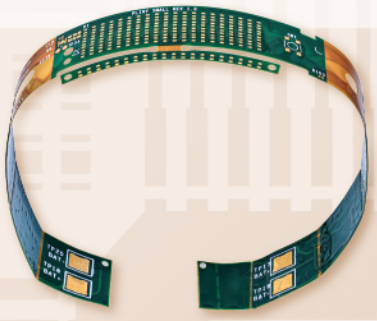

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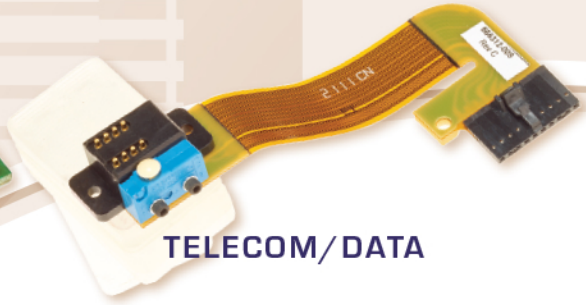

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possible on COVID-19 relief-type activities. We've been doing whatever we can to strengthen our infrastructure and be ready for a post-COVID-19 environment to utilize that vehicle and really help veterans successfully transfer to civilian careers.

Jahr Turchan

Regarding veterans, from a Blackfox standpoint, we had best-laid plans, and then COVID-19 happened. We had a number of manufacturing partners lined up to support the effort, and the goal was to have a physical training center near the bases here in Colorado Springs to upskill them with manufacturing skills to help them transition. We have taken that desire and purpose but pivoted to an online e-learning platform, which we'll launch later this year. It is still very veteran-focused.

The goal will be for veterans to be able to utilize these trainings at little to no cost to them, whether that's through WIOA funding, workforce centers, nonprofit donations (such as Evolution Foundation), or other methods that we'll discover. The other organizations that we're working with are the National Association of Manufacturers (NAM) and Heroes MAKE America, their sub-organization; Blackfox was going to be their first affiliate partner.

They are currently on three other bases across the USA and need help to expand into further bases. And we were going to be that first affiliate partner to expand into Colorado Springs for them and manage the training for these transitioning veterans. That is still slated to happen, and discussions on that will resume in early 2021. They have just had to dial everything back because they had to pivot all of their programs, obviously being online, plus all of the other 2020 debacles have slowed things down. But the progress is still there. The NAM organization, as well as our contacts at the various military bases here in Colorado Springs, are all very excited for this program because we will be the first manufacturing-focused Career Skills Program (CSP) on the base.

There are currently 17 CSPs offered to transitioning military personnel to give them skill sets to move into the civilian workforce, but none of them have a manufacturing focus. It will be the first one. And that's exciting for us and exciting for them.

Dill: One of our challenges has been getting feedback from manufacturers in general, as to what specific skills are important in their new hiring process because we want to make sure we integrate all of these needs when we launch this program. Everyone is so busy right now, trying to reset and move forward with our new environment, that we're having some difficulty getting feedback.

Al Dill

But if there are manufacturers out there that are interested in potentially considering hiring our veterans and giving us some input on some of their important skills, we would certainly appreciate that. If they'd reach out to us and make that contact, it's critical for us to move forward quickly once we have a little relief. We must clearly understand what is critical for manufacturers when it comes to either upgrading their workforce or the new workforce, but—more specifically—the new workforce, and mostly veteran-focused.

Johnson: Blackfox touches on a three-circle Venn diagram. You have industry needs around staffing, employer needs around staffing, and veteran transition needs. You're working in the dead center of that Venn diagram.

Dill: Exactly. You've got it, Nolan. I very much appreciate that.

Johnson: It's a good program.

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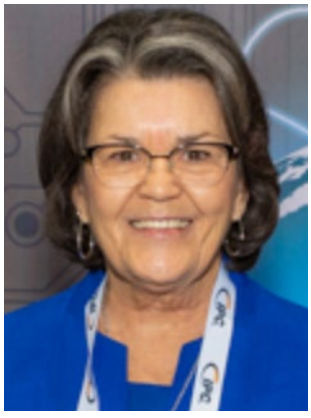
Sharon Montana-Beard: To support that, I just want to say that what we knew last year about what their needs were, we don't know this year, and that's all in the change of the environment. As the water is lower and the rocks start sticking up, perhaps some of their pains and desires or needs have changed. We need to know that.



Sharon Montana-Beard

Johnson: There are definitely more conversations to be had and more interactions required with the people involved. I get that. This has been incredibly productive. Thank you for your time.

Dill: Thank you, Nolan. **SMT007**

If you're interested in hiring veterans or learning more about our e-learning programs, contact Jahr Turchan.

New Electronic Skin Can React to Pain Like Human Skin

Researchers have developed electronic artificial skin that reacts to pain just like real skin, opening the way to better prosthetics, smarter robotics, and non-invasive alternatives to skin grafts. The prototype device developed by a team at RMIT University in Australia can electronically replicate the way human skin senses pain.

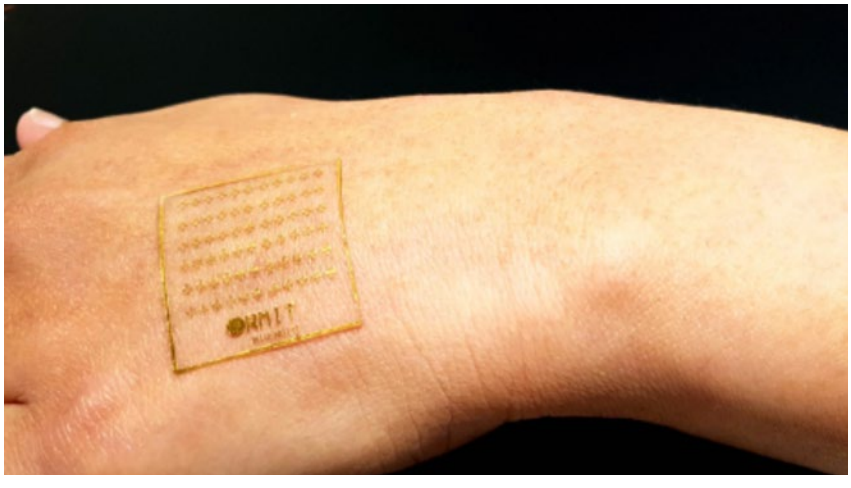
The device mimics the body's near-instant feedback response and can react to painful sensations with the same lightning speed that nerve signals travel to the brain. Lead researcher Professor Madhu Bhaskaran said the pain-sensing prototype was a significant advance toward next-generation biomedical technologies and intelligent robotics.

"Skin is our body's largest sensory organ, with complex features designed to send rapid-fire warning signals when anything hurts," Bhaskaran said. "We're sensing things all the time through the skin, but our pain response only kicks in at a certain point, like when we touch something too hot or too sharp. No electronic technologies have been able to realistically mimic that very human feeling of pain until now. Our artificial skin reacts instantly when pressure, heat or cold reach a painful threshold. It's a critical step forward in the future development of the sophisticated feedback systems that we need to deliver truly smart prosthetics and intelligent robotics."

The new research, published in *Advanced Intelligent Systems* and filed as a provisional patent, combines three technologies previously pioneered and patented by the team:

- **Stretchable electronics:** Combining oxide materials with biocompatible silicone to deliver transparent, unbreakable, and wearable electronics as thin as a sticker.
- **Temperature-reactive coatings:** Self-modifying coatings 1,000 times thinner than a human hair based on a material that transforms in response to heat.
- **Brain-mimicking memory:** Electronic memory cells that imitate the way the brain uses long-term memory to recall and retain previous information.

(Source: RMIT University)



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Critter & Guitari Installs In-House PCB Assembly Line from Manncorp ▶

Music company Critter & Guitari decided to take on their own PCB production with a little help from Manncorp, and it is changing their process of creating and selling products for the better.

Organizational and Team Management in Times of Change ▶

Ross Berntson, president and COO of Indium Corporation, shares his perspective, thoughts, and lessons learned on managing his global organization as Indium Corporation responds to health issues, market demand shifts, and organizational change.

Dymax Corporation Celebrates 40th Anniversary ▶

Over the past 40 years, Dymax Corporation has built a tradition of excellence providing manufacturers with adhesive chemistry and equipment solutions for a variety of applications within the medical device, automotive, electronics, and aerospace and defense industries worldwide.

Insituware Hires Director of Customer Experience ▶

Insituware LLC, the provider of the first smart in situ measurement solution with integrated machine learning technology, recently announced the appointment of Jeanne R. Nevelos to Director of Customer Experience. Nevelos was hired under Insituware's parent company.

Indium Corporation Introduces New Ball-Attach Flux ▶

Indium Corporation has released a new ball-attach flux, WS-829, designed for printing and pin transfer applications for the smallest sphere and high-density applications, including LED die-attach.

MacDermid Alpha Scheduled to Exhibit, Present Five Technology Papers at SMTAi ▶

MacDermid Alpha Scheduled to Exhibit, Present Five Technology Papers at SMTAi MacDermid Alpha Electronics Solutions presented five technical papers at SMTA International Virtual Conference and Exhibition, held Sept. 28-30, 2020, and was also an exhibitor at the event.

KYZEN Announces Participation at SMTAi Virtual Conference & Expo ▶

KYZEN Announces Participation at SMTAi Virtual Conference & Expo Environmentally friendly cleaning chemistry provider KYZEN is pleased to announce its participation in the SMTA International Virtual Conference & Expo, scheduled to take place Sept. 28-30, 2020.

Electrolube Facilitates Product Selection with New Websites, Online Tools, Samples ▶

The specialist electro-chemicals manufacturer, Electrolube, announced the launch of its brand-new product selection tool to help customers source the most pertinent products more easily for their application requirements.

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What's Lurking in the Shadows?

Quest for Reliability

by Eric Camden, FORESITE INC.

There are two terms in the electronics industry that I feel should be more widely used. The first is an acronym for "violates minimum electrical clearance," which is obviously, and simply, VMEC. It has always confused me why this isn't already heavily used. We use TLAs for everything (TLA is an acronym for three-letter acronyms, by the way).

The second term I use on a regular basis, and the focus of this month's column, is "contamination relocation." I use this term mostly when I test a PCBA that has gone through some sort of localized cleaning process after a manual or selective soldering operation. In most of the cases I have seen, when a no-clean flux is used, localized cleaning is a totally useless practice intended only to improve a cosmetic issue. Cosmetic issues are usually just that and don't have any impact at all on functionality or reliability. I'd rather have an ugly, reliable board than a sparkling clean field failure.

In some cases, there are legitimate reasons to perform localized cleaning. The number one reason is when you are using a water-soluble flux for the soldering process. As with any water-soluble flux, the activators are never rendered near benign through a thermal excursion and will always be hygroscopic, as well as corrosive. That means you don't have to worry only about electrical leakage failures. The residues can cause corrosion without any bias differential or available atmospheric moisture. That's one reason I really like working on PCBA failures if they were built with a water-soluble flux. If you see flux residues, that is more than likely your root cause of failure. It's a short day, and I can go fishing in no time.

Another valid reason to perform localized cleaning is when you are planning to use conformal coating on the PCBA. Flux residues can cause adhesion issues in some cases, and if you use parylene, a full cleaning is required. You

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may also need to clean the residues to access test points if you're not using a probable flux. Sensitive RF circuits also can be affected by flux residues and need to be removed to ensure proper operation. I think that pretty much exhausts the good reasons to perform localized cleaning. It's not a long list. Please note that cosmetic appearance did not make the list.

What is lurking in the shadow? It is most likely active flux residues spread around by the localized cleaning process. And much like a teenager standing on your porch, trying to score some candy from you by stuffing a few pens in their shirt pocket and saying they're a nerd, you just don't want that. And ouch, by the way, that's just rude. This month, I want to highlight localized cleaning that is performed correctly and incorrectly, as well as the impact on cleanliness and reliability.

I often go into a production facility for a process review and see operators using an acid brush of questionable cleanliness that's been dipped in IPA, scrubbing away after a manual soldering process and then inspecting the area of concern for residues. If none are found, they simply pass the boards down the line for subsequent processing. What I never see is that the same operator looking in the adjacent areas for residues. Those areas are the shadows I mentioned. In almost every case, you can't inspect monolayers for residue under components with low standoff height for some time.

That same low standoff height makes them very difficult to clean under the best of circumstances. When you add IPA or other solvents to the flux residue, all that does is make it soluble. What it does not do is magically make detrimental flux residues disappear like many seem to think it does. Don't believe me? Let's look at some ion chromatography (IC) data from a field failure.

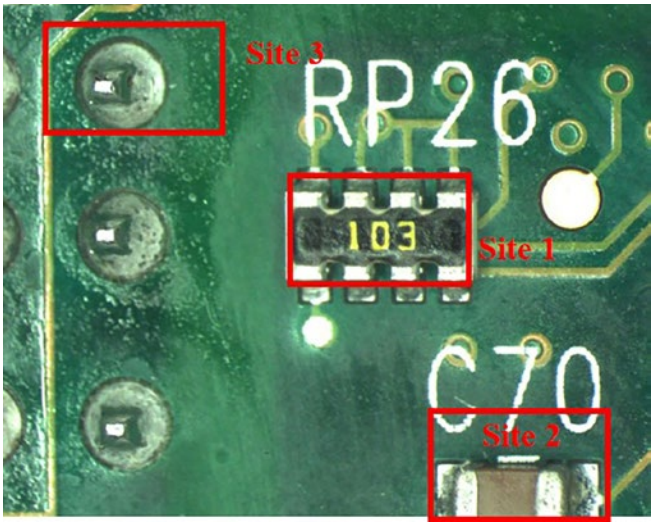

Figure 1: Area after localized cleaning.

Touch-up soldering was done to an SMT component, and according to the work instruction, this process includes a quick cleaning with IPA. The boards are already built with no-clean flux, but any touch-up requires cleaning. Figure 1 shows the SMT part that was cleaned, as well as the capacitor and PTH pins that were tested.

The IC data in Table 1 shows low levels of ionics at the SMT location, but much higher

all values in ug/in^2							
Sample Description	Chloride	Bromide	Nitrate	Sulfate	WOA	Sodium	Ammonium
Foresite recommended limits for PCBA (clean)	6.0	6.0	3	3.0	25	3	3
After Localized Cleaning							
Area #1	1.24	2.35	0.59	0.00	23.15	2.35	1.24
Area #2	2.07	2.04	1.36	0.00	174.69	4.51	2.11
Area #3	1.63	0.57	2.15	0.00	143.17	4.06	2.15
After Recovery Cleaning							
Area #1	0.30	1.21	0.21	0.00	6.52	0.25	0.41
Area #2	0.41	1.05	0.05	0.00	4.27	0.36	0.50
Area #3	0.65	0.56	0.03	0.00	6.08	0.14	0.26

Table 1: IC data results.

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levels are now present in the other two areas. Performing localized cleanliness testing was key to shining light on those "shadows." The chemical signature shows that the flux uses a weak organic acid, and at these levels in the PTH/capacitor, areas are at an increased risk of electrical leakage or even dendrite growth. This same board was put through an inline wash process, and the second set of IC data shows acceptable levels of ionics across the board.

A large batch of boards processed like this had to be recovery cleaned before shipping to the customer because of that increased reliability risk. It's what we had to do to get that darn teenager off the porch. This method of localized cleaning is like running your vacuum without a bag, or you could also say contamination relocation. Please say it as a matter of fact. It's my "Git-r-done," if you will. The similarities stop there.

The good news is there is a simple way to enhance this same basic cleaning method while reducing the spread of IPA and solubilized residues onto neighboring components. Instead of dipping the end of the acid brush into a bottle, soak a lab wipe with IPA and then place that wipe over the area that needs to be cleaned. Then, you use the brush on top of that wipe to clean as normal (Figure 2). The wipe will absorb the flux/solvent mixture (Figure 3), not allowing the solution to transfer to neighboring components and become a potential risk for electrical leakage in the field.

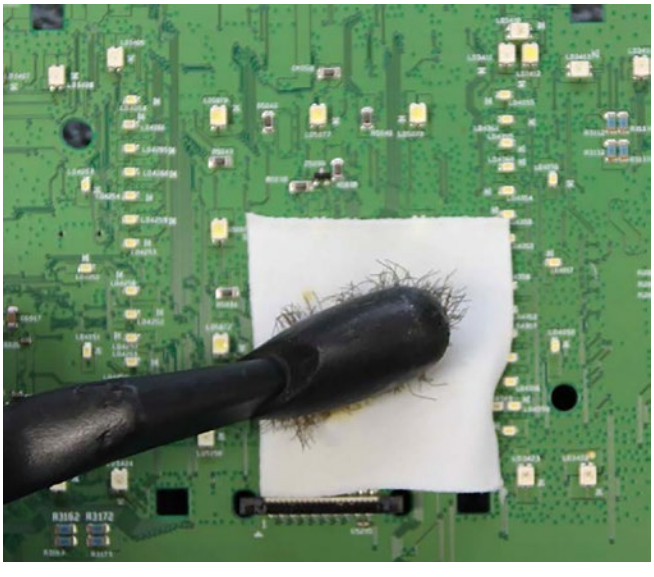

Figure 2: Lab wipe and brush.

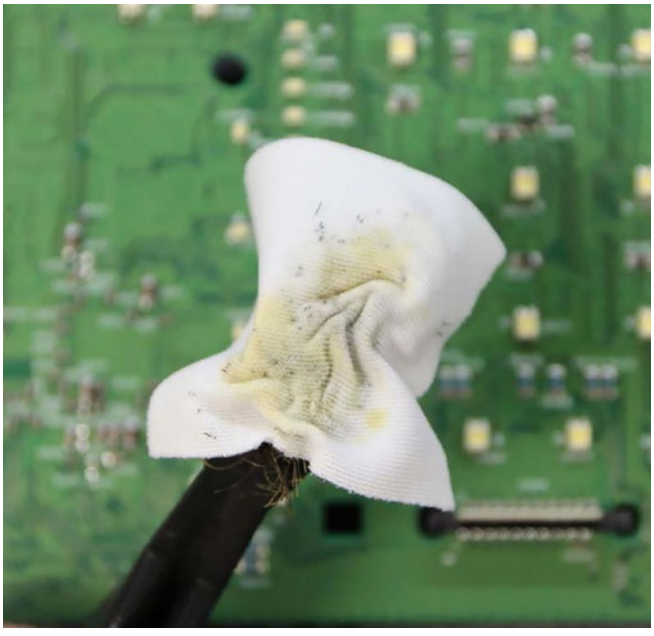

Figure 3: Lab wipe after localized cleaning.

The wipe is then simply discarded. It's important that a new wipe is used for each individual cleaning process. A wipe or brush will collect residue over time, so using a new wipe eliminates cross-contamination. As with any assembly process, you need to create objective evidence that the process is effective using some sort of cleanliness or environmental exposure testing.

Conclusion

It might be close to Halloween, but there isn't any reason to be afraid of what your cleaning process is doing to reliability if you shine enough light on the process. And should teenagers try and haunt your porch this year, give them full-size candy bars instead of a hassle. Everyone likes candy. **SMT007**

Eric Camden is a lead investigator at Foresite Inc. To read past columns or contact Camden, click here.

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2/3 of electronic industry companies have difficulty finding production workers.[1]

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[1] IPC. (2017). Findings on the Skills Gap in U.S. Electronics Manufacturing.

Process Effectiveness Qualification

Operational Excellence
by Alfred Macha, AMT PARTNERS

A New Approach to Supplier Qualification After COVID-19

Traditional supplier qualification processes have been forced to rapidly change to new approaches as suppliers have been affected by shelter-in-place directives across the globe. On-site supplier audits are no longer a viable method to review a supplier's facility and controls. Customers have been forced to rely on the supplier self-audit checklist, resulting in higher scrutiny of supplier quality procedures and increased incoming quality inspection of first article or pilot production lots.

These mitigation steps add a higher level of administrative burden to customers by creating non-value-add activities that may not result in proper risk assessment. The need to reconfigure supplier qualification processes is a top priority for many manufacturing organizations. Before we discuss process effectiveness qualification reviews, let's go over the fundamentals of assessment definitions of conformance, effectiveness, risk, and intellectual property (IP).

Conformance vs. Effectiveness

The traditional ISO-based self-audit checklists, where quality system documentation is provided by a supplier, confirms that the supplier has a quality system in place. Conformance to a quality system standard is important, as it informs the supplier qualification team that procedures are in place and objectives have been defined. However, it does not indicate that procedures have been effectively implemented nor if the process is monitored to achieve process or quality objectives. The definition of "effectiveness" is the ability to meet objectives and be successful in producing the desired result. Thus, supplier qualification requires an effectiveness review to properly assess the risk of working with a supplier [1].

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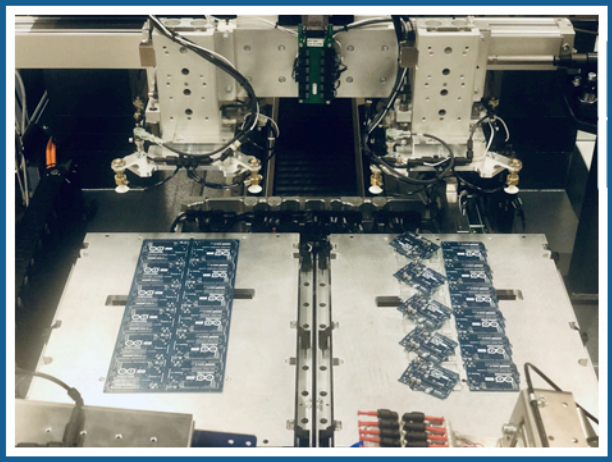

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Practical Approach to Risk Evaluation

The foundation of supplier qualification is based on risk evaluation. Risk management has taken a higher level of importance in recent quality system standards of ISO 9001, ISO 13485, and AS9100, among other quality system standards. But first, we need to understand risk. The new ISO 31000:2018 risk management guidelines offer the following definition of risk in section 3.1 [2]:

Risk: Effect of uncertainty on objectives

1. Note 1 to entry: An effect is a deviation from the expected. It can be positive, negative, or both and can address, create, or result in opportunities and threats.
2. Note 2 to entry: Objectives can have different aspects and categories and can be applied at different levels.
3. Note 3 to entry: Risk is usually expressed in terms of risk sources (3.4), potential events (3.5), their consequences (3.6), and their likelihood (3.7).

In essence, supplier qualification requires risk assessment before approving a new supplier to the supply chain. Companies need to establish risk evaluation procedures for qualifying new suppliers. Risk assessment allows companies to objectively determine the qualification level required for a new supplier depending on the supplier's performance impact and supply chain to the company. Table 1 provides considerations needed when determining the qualification level for a new supplier.

Higher risk suppliers require a process effectiveness qualification and a quality system conformance qualification. Medium-risk suppliers are only required to do a quality system conformance qualification. Low-risk suppliers may be sufficient to complete a questionnaire or demonstrate an ISO certification.

IP Considerations

Suppliers typically have no concerns providing quality systems documentation to customers as a method to demonstrate conformance to established quality systems standards. This practice has been commonly accepted in all industries for many decades. However, when it comes to process effectiveness qualification, suppliers are required to provide process conformance information to demonstrate the ability to perform to expectations.

Suppliers may initially be hesitant to do this if process knowhow is requested as part of the process effectiveness qualification. It is important to protect a supplier's IP during any review of process effectiveness exercise. The focus should be to monitor performance vs. plan on key process characteristics.

Process Effectiveness Qualification Plan

The foundation of process effectiveness is to have an unbiased way to measure performance results in comparison to the plan. Suppliers are required to demonstrate performance with empirical data. Performance effectiveness qualification activities can be done

Supplier	Performance Impact Risk Level	Supply Chain Risk Level	Qualification Level
Evaluation should be completed for each supplier.	Determine the performance impact of the service or material sourced to the overall functionality of your product.	Determine the ability to source this material or service with desired lead times or delivery complexity.	This should be applied based on the risk levels for the material or service.
	Levels should be high, medium, or low.	Levels should be high, medium, or low.	Process effectiveness qualification and/or quality system conformance qualification.

Table 1: Considerations when determining the qualification level for a new supplier.

Performance Section	What Is Measured?	Purpose of Measurement
Delivery	On-Time	Measure the consistency of product deliveries. Request on-time trend data to determine the level of consistency.
	Average Lead Time	Measure the lead time for materials or services sourced over a period of time.
Quality	RMA %	Measure returns based on product conformance. Request for RMA % trend data to determine the level of consistency.
	Complaint Response Time	Measure the responsiveness to field issues reported. Request complaint response time trend data to determine the level of consistency.
	CAR Implementation Duration	Measure the ability to successfully implement corrective actions within an adequate timeline.
Process Controls	Key Process Control Parameter	Define the process parameter(s) that are key performance indicators of process consistency. Request control charts for these key process parameters to evaluate consistency and variation over time.
Training	On-Time	The percentage of training on-time shows the commitment that the supplier has to develop skills.

Table 2: How to set up a process effectiveness qualification plan.

remotely.

Table 2 provides guidance on how to set up a process effectiveness qualification plan. The requirement is for the supplier to complete this table and provide periodic reports to demonstrate effectiveness for the agreed-upon measurements. This plan allows customers to assess risk and monitor the performance of key suppliers.

Every item provided below should have a defined measurement target and frequency of when this measure is taken and reported. Include an evaluation section for each line item to assess the ability of the supplier to provide this data periodically and the results to the plan.

The expectation is for the supplier to provide historical performance data of product lines similar to what they will be providing you as a new customer. This data will serve as a baseline to compare to how the supplier performs to your product requirements in the future against baseline measurements established in Table 2.

Once the process effectiveness plan has been completed, then the supplier can provide periodic updates—usually monthly or quarterly—of new performance data. The data can be trended to monitor improvements over time.

The qualification team should review the data provided by the supplier to determine the adequacy and assess qualification risk. This document should then be retained in the file as a quality record for supplier qualification before the supplier is added to the AVL. **SMT007**

References

1. D. Banister-Hazama, J. Moreci, & K. England, "Increase project team effectiveness: step-by-step," PMI® Global Congress 2012–North America, Vancouver, British Columbia, Canada. Newtown Square, PA: Project Management Institute, 2012.
2. ISO, "ISO 31000:2018(en): Risk management–Guidelines."

Alfred Macha is the president of AMT Partners. He can be reached at Alfred@amt-partners.com. To read past columns or contact Macha, click here.

1 Lean Digital Thread: Data-Driven Decisions and Micro-Solutions in Manufacturing ▶


Sagi Reuven

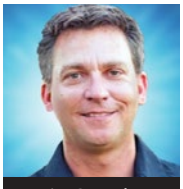
In past columns, Sagi Reuven has written about two pillars: (1) data collection and the basic questions you can answer, and (2) material management and its impact. In this column, he discusses the next level—changing the mindset from reporting to analytics and focusing on making small improvements.

2 What Is Digital Twin Technology, and Why Is It So Important? ▶


Happy Holden

Happy Holden describes how Siemens' 12-part webinar series, "Implementing Digital Twin Best Practices From Design Through Manufacturing," is an excellent series designed to educate the electronic manufacturing engineer on the progress of using a digital thread to improve products and performance.

3 Quest for Reliability: Reliability Starts at the Bottom ▶


Eric Camden

It is much cheaper to perform product-specific reliability testing before the product goes into the field. Eric Camden shares some testing recommendations based on failure analysis, as well as lessons learned from a few of our customers over the years using case studies and data on failed units.

4 Zulki's PCB Nuggets: FCBGA Packaging Enters PCB Microelectronics Assembly ▶


Zulki Khan

The demand for smaller circuitry and packaging, as well as ever-shrinking PCB real estate, have continually pushed PCB assembly and manufacturing protocols. Part of these technological advances involves a combination of flip-chip and BGA (FCBGA) packaging. Zulki Khan explains the importance of FCBGAs.

5 TT Electronics Awarded Team Tempest Contract from BAE Systems ▶

TT Electronics, a global provider of engineered electronics for performance-critical applications, announced it had been awarded a contract from BAE Systems for the design, development, and qualification of a DC-DC Converter to support project Tempest. Harnessing TT's extensive engineering capabilities, this unit will be used within the Flight Control System to deliver power conversion functionality to a number of elements within the FCS.

6 Knocking Down the Bone Pile: PCB Rework of 0201 Packages ▶

As electronic passive components continue to shrink in size, methods for their rework need to be developed by electronic manufacturers to maintain and support PCB assembly processes. Columnist Bob Wettermann compares and outlines a few of these rework methods.

7 Free Webinar Series on How to Implement Digital Twin Best Practices ▶

I-007e Micro Webinars recently released a free, on-demand series titled "Implementing Digital Twin Best Practices From Design Through Manufacturing." Each of the 12 segments can be viewed in about five minutes.

8 I-Connect007 Releases Exclusive Coverage of 2020 IPC High-Reliability Virtual Forum ▶

I-Connect007 proudly announces the release of special event coverage of the 2020 IPC High-Reliability Forum.

9 Improving Tech Support During a Pandemic ▶

Koh Young's Quintin Armstrong, senior manager of technical services and applications for the Americas, discusses the work that has been going on at the company around field support, including pre- and post-sales support training, and how those areas have been affected by COVID-19.

10 Just Ask Joe: The Occam Process ▶

First, we asked you to send in your questions for Happy Holden. Now, it's Joe Fjelstad's turn! Inventor, columnist, instructor, and founder of Verdant Electronics, Joe has been involved with rigid PCBs and flexible circuits for decades, and he's ready to share some of his knowledge with our readers. We hope you enjoy "Just Ask Joe."

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THE PROFILE:

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Scope:

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- Write plan for process implementation
- Implement process and perform failure mode analysis to establish correct operating conditions
- Write all necessary procedures and instructions for process operation, maintenance and safety
- Monitor process operation on a daily basis to ensure consistency
- Perform failure and root cause analysis when product/process problems occur
- Perform chemical analyses on processes when required

Knowledge and Skills:

- Ability to read, write and communicate in English necessary to perform the job
- Knowledge and application of statistical techniques for process control
- Knowledge and application of failure mode effect analysis techniques as applied to process improvement and process development
- Ability to lift 25 pounds
- Will be exposed to hazardous waste while performing daily job duties
- Will undergo chemical handling training prior to start and will actively participate in ongoing hazardous waste and chemical handling training

Education and Experience:

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As a key member of the Flexible, Formable, and Printed Electronics (FFPE) Team, the applications engineer will be responsible for developing applications know-how for product evaluation, material testing and characterization, and prototyping. In addition, this applications engineer will provide applications and technical support to global customers for the FFPE Segment.

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Manncorp™

SMT Operator
Hatboro, PA

Manncorp, a leader in the electronics assembly industry, is looking for a **surface-mount technology (SMT) operator** to join their growing team in Hatboro, PA!

The **SMT operator** will be part of a collaborative team and operate the latest Manncorp equipment in our brand-new demonstration center.

Duties and Responsibilities:
- Set up and operate automated SMT assembly equipment
- Prepare component kits for manufacturing
- Perform visual inspection of SMT assembly
- Participate in directing the expansion and further development of our SMT capabilities
- Some mechanical assembly of lighting fixtures
- Assist Manncorp sales with customer demos

Requirements and Qualifications:
- Prior experience with SMT equipment or equivalent technical degree preferred; will consider recent graduates or those new to the industry
- Windows computer knowledge required
- Strong mechanical and electrical trouble-shooting skills
- Experience programming machinery or demonstrated willingness to learn
- Positive self-starter attitude with a good work ethic
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Skills and abilities required for the role:
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Qualifications

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- Excellent technical skills

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- Work with customers in developing cost-effective production processes.
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- Generate process control plan for manufacturing processes, and identify opportunities for capability or process improvement.
- Participate in FMEA activities as required.
- Create detailed plans for IQ, OQ, PQ and maintain validated status as required.
- Participate in existing change control mechanisms such as ECOs and PCRs.
- Perform defect reduction analysis and activities.

Qualifications

- BS degree in engineering
- 5-10 years of proven work experience
- Excellent technical skills

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Thank you, and we look forward to hearing from you soon.

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Manncorp™

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Hatboro, PA

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- Assist with demonstrations of equipment to potential customers
- Build and maintain positive relationships with customers
- Participate in the ongoing development and improvement of both our machines and the customer experience we offer

Requirements and Qualifications:
- Prior experience with SMT equipment, or equivalent technical degree
- Proven strong mechanical and electrical troubleshooting skills
- Proficiency in reading and verifying electrical, pneumatic, and mechanical schematics/drawings
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This professional has years of experience running PCBA companies. Led his companies with creative and innovative leaderships skills. Is a collaborative, hands-on leader. He is looking for a full-time position.

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Seasoned professional has spent the past 20 years building and growing American sales teams for both global and domestic companies. Specializes in building and managing rep networks. He is looking for a full-time position.

Global Engineering Manager/Quality Manager
Has experience working with large, global PCB companies managing both engineering and quality staff. Very experienced in chemical controls. She is interested in working on a project-by-project basis.

CAM Operators and Front-end Engineers
These candidates want to work remotely from their home offices and are willing to do full-time or part-time projects.

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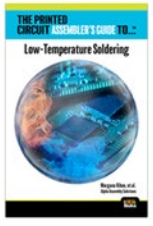

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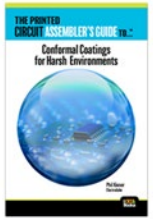

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