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DESIGN007 MAGAZINE

Streamlining Standards

It's no secret that the standards situation in PCB design, manufacturing, and assembly is anything but standard. This alphabet soup of documents and guidelines can be a confusing maze even for veteran professionals. This month, we untangle the often-confusing world of standards.

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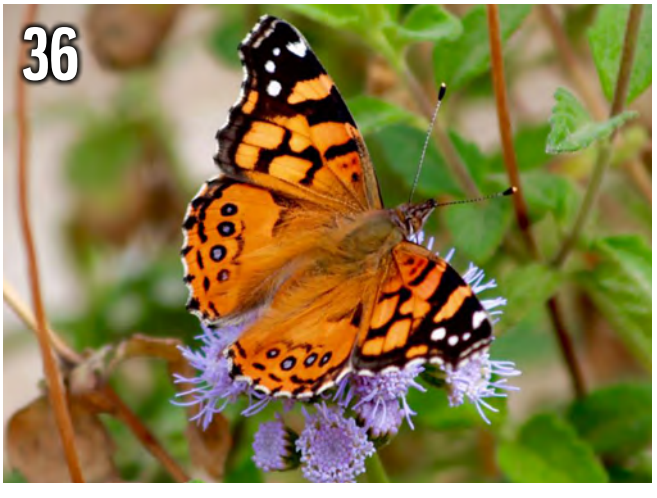

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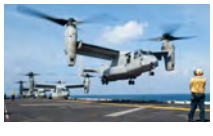

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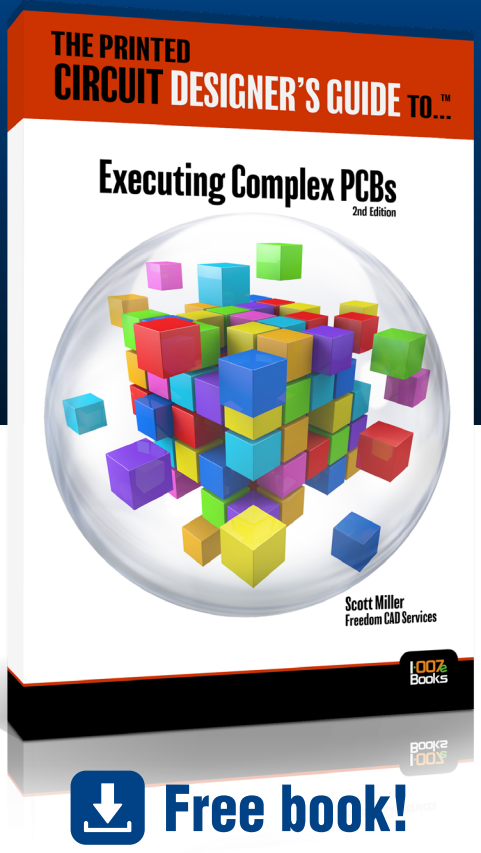

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FLEX007

Focusing on Flex

We're heading into fall, but the electronics industry is still smoking hot. Flexible circuits are continuing to find their way into almost every type of device. With the advent of 5G and IoT, flex standards are more critical than ever, especially for rigid board designers who have been forced into designing flexible circuits. This month we explore the world of standards for flexible circuits.

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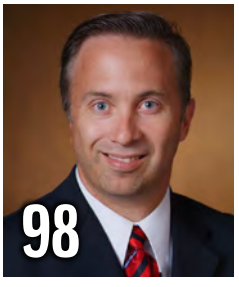

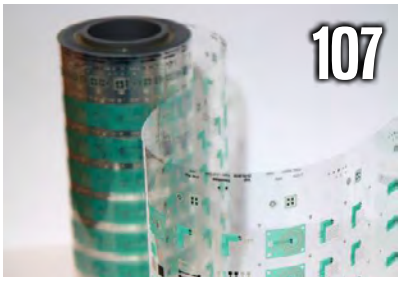

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Time to Streamline Standards

The Shaughnessy Report

by Andy Shaughnessy, I-CONNECT007

Right now, there's a lot going on with standards for the electronics industry. It's a busy time for all of the volunteers serving on standards committees, and I say only half-jokingly that you have my sympathy!

It's no secret that the standards situation in PCB design, manufacturing, and assembly is anything but standard. PCB designers have three options for data transfer standards: Gerber, ODB++, and IPC-2581. The overwhelming majority of PCB designs are handed off in Gerber files, but ODB++ and IPC-2581 are gaining popularity all the time. It's hard not to think, "Pick a standard and be done with it!" If only it were that simple.

After attending the IPC Summer Meetings in Raleigh, North Carolina, I have a better understanding of just how difficult standards development can be. Of course, I couldn't get into the actual meetings where the industry volunteers debated various changes to the standards and training documents. But I attended all of the "Panelpalooza" forums and had some really eye-opening conversations with committee members.

During lunch, one of the brand-new committee members said that he couldn't believe that his group spent almost an entire day discussing one word in a document. The grizzled veterans at the table laughed; that's just par for the course. I think I'd go crazy sitting in a room all day debating whether to change one word.

But as I learned, this tedious, nuts-and-bolts work has to be done. For instance, does the word "lead" in your document refer to the chemical element Pb or to the legs that attach a component to a PCB? If you translate that document into Spanish or Mandarin, these small details can cause big problems down the road. Some committees were working to change the standards process itself and make updates to the documents in a more timely manner. Other were focusing on the "harmonization" of this alphabet soup of global standards. There is

a lot of overlap in international standards; some of IPC's documents are duplicated by organizations, such as ANSI, IEC, and JEDEC. Streamlining these documents worldwide would eliminate a lot of unnecessary work.

Of particular interest for me at the IPC Summer Meetings was one group charged with the melding of the IPC-2581 design data format with IPC's Connected Factory Exchange (CFX) manufacturing standard into DPMX. As you'll see in this month's issue, the heavy lifting is over; DPMX will create a front-to-back flow of data from the schematic through final assembly, in a free, open-source process. I expect you'll be hearing a lot about this effort in the fall.

This month, we untangle the often-confusing world of standards. We start with a conversation with Karen McConnell of Northrop Grumman, who offers an update on the committees she chairs. Then, Gary Carter of XPLM and Michael Ford of Aegis Software discuss their work merging IPC-2581 with IPC's CFX into DPMX, a design-through-assembly standard. Next, Leo Lambert of EPTAC addresses the move by IPC to change the way standards and training documents are developed, including some methods for eliminating errors and duplicated comments during revision. We also have a conversation with Emma Hudson of Gen3 Systems who explains her work on a committee that seeks to streamline and "harmonize" IPC standards with other global organizations' standards.

Karel Tavernier of Ucamco provides an article explaining why so many PCB designers still use Gerber, and how Ucamco has continued to update the tried-and-true format. Max Clark of Mentor, a Siemens Business, traces the development of ODB++ and breaks down the advantages of using this format that's already installed at many manufacturing facilities. Linda Mazzitelli of PTC offers details about the IPC-2581 and how DPMX will help optimize Industry 4.0. And columnist Tim Haag explains why you should listen to your boss if they say, "Check the standard."

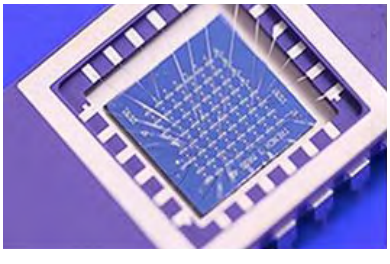
We also have a great article by our columnist John Coonrod, "Insertion Loss Performance Differences Due to Various Plated Finish and Circuit Structures." Further, we bring you columns by our regular contributors, including Stephen Chavez, Bob Tise, and Phil Kinner.

And let's all congratulate Barry Olney on his 100th "Beyond Design" column. It's hard to believe Barry has been writing this popular column for over eight years. Time flies when you're having fun! See you next month. **DESIGN007**

Andy Shaughnessy is managing editor of *Design007 Magazine.* He has been covering PCB design for 19 years. He can be reached by clicking here.

World's Smallest Accelerometer Points To New Era In Wearables, Gaming

Researchers at KTH have developed the smallest accelerometer yet reported, using the highly conductive nanomaterial graphene. The latest step forward is a tiny accelerometer made with graphene by an international research team involving KTH Royal Institute of Technology, RWTH Aachen University and Research Institute AMO GmbH, Aachen.



Among the conceivable applications are monitoring systems for cardiovascular diseases and ultra-sensitive wearable and portable motion-capture technologies. Max Lemme, professor at RWTH, is excited about the results.

"Our collaboration with KTH over the years has already shown the potential of graphene membranes for pressure and Hall sensors and microphones," says Lemme.

(Source: KTH Royal Institute of Technology)

Design For Excellence: Karen McConnell on Standards

Feature Interview by Andy Shaughnessy
I-Connect007

During the IPC Summer Meetings, I spoke with Karen McConnell, senior staff CAD CAM engineer with Northrop Grumman Mission Systems. Karen is a veteran PCB designer as well as an IPC committee chair and mentor. She offered an update on some of the IPC committees she chairs, the need for more mentor programs in this industry, and why you can call something a ham sandwich if you define it correctly in the standard.

Andy Shaughnessy: Karen, it's nice to see you again. Now, you seem to be staying fairly busy—you're a committee chair as well as an IPC mentor. Can you tell us about what's been happening in some of the committees that you chair?

Karen McConnell: I'll start with the Design for Excellence Committee (1-14). We recently released the IPC-2231 document on design for excellence (DFX). One of the things we're doing immediately in the next revision is adding the phrase "Design for Excellence" in the title so that everybody knows what DFX is. The document is a guideline for a company or a group to grow or start a DFX program. It includes the science of fabrication, assembly, test, and environment. The 1-14 Subcommittee went immediately into revision because we knew that the document would never be complete. We expected it to be one of those documents that are continuously revised because of comments coming in from the industry as they start to use this document. One of the things we want to do this time with revision A is to develop a feedback loop for the industry to supply their comments or better ways of doing what we suggested.

I am also a co-chair for the Land Pattern Committee (1-13). We were trying to redo a whole revision based on things that JEDEC had proposed, but a recent decision by the 2-30 Committee is making the 1-13 Committee revisit our decision. We're trying to come up with a plan to table some of the updates we have done, revise the 73-51 B version, correct any errors, release it, and then look at the JEDEC proposal.

Further, I'm an IPC mentor. My mentee, Kevin Kusiak of Lockheed Martin, graduated at IPC APEX EXPO last year. It is a great program if you have young engineers that you want to grow in the printed board industry. They are mentored by an experienced IPC member within your company or another company on how to navigate the IPC environment, the standards, what the standards are about, and how to take advantage of the training. They are given free admittance into IPC APEX EXPO for three years. The mentor's and mentee's managers have to sign off that they are committed

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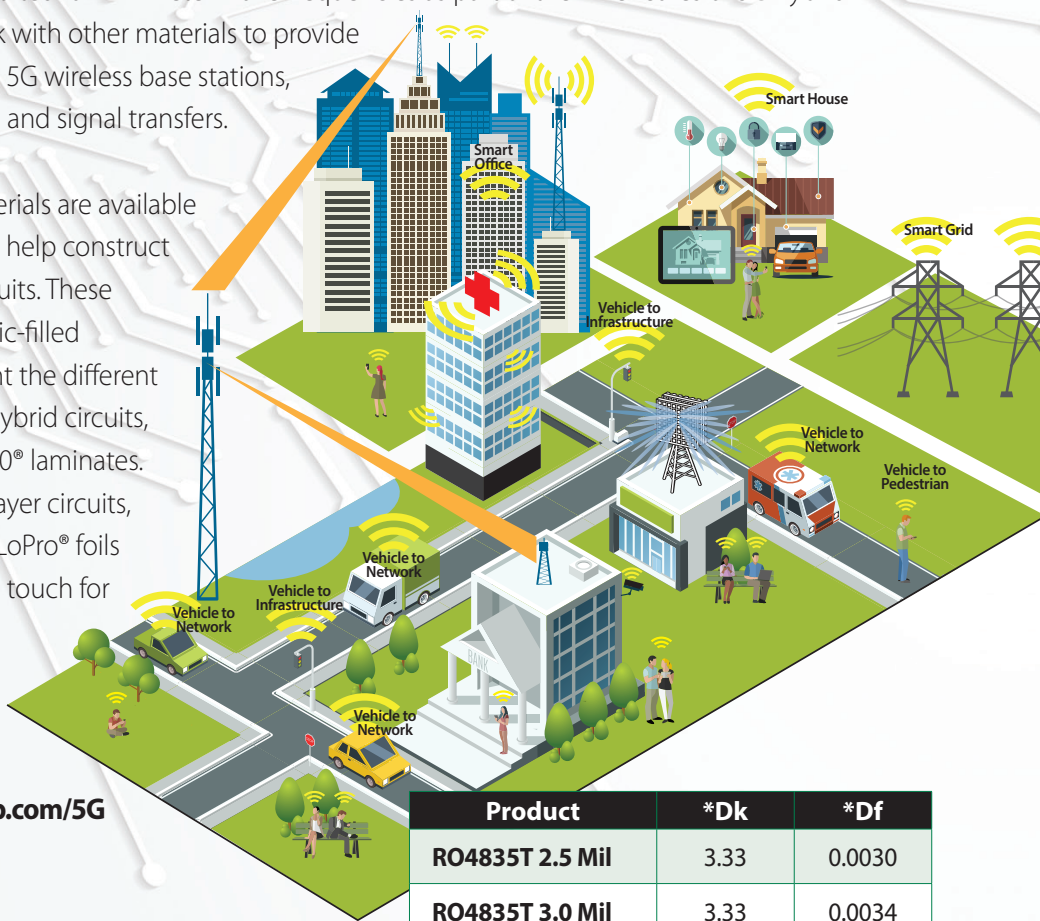

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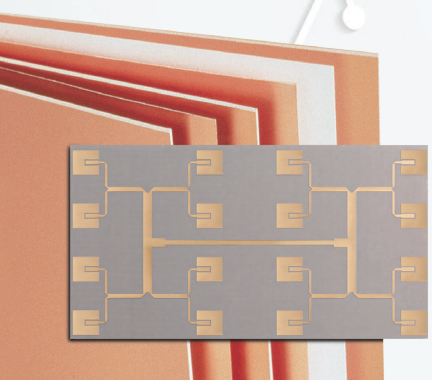

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to supporting the travel and the person's time throughout the three-year program.

When I was a mentor, IPC gathered mentees together to train them and to give them opportunities, even in social settings. The mentees move through in their different areas of expertise and grow; they deal with people in other areas. Some of the mentees have even started being co-leaders, so I think it's a really good program to keep the industry going with the younger folks. Companies should consider contacting IPC about this program.

Shaughnessy: I know a lot of companies don't have mentors anymore. New designers used to shadow a senior designer for six months.

McConnell: Right, companies are not paying for mentors anymore. This program benefits your company, and all you have to do is nominate someone. The program started with five mentors and mentees, and I was in the first group. My mentee started six months into the program, so he graduated with the second group. He couldn't attend the first meeting, so we ended up in this no man's land between the first two mentee groups. Sometimes, we were with the first group, but other times, we were with the newer group. This year, they're going to try to have 20 mentees.

Shaughnessy: Wow.

McConnell: Yes, that's how it's grown. The other committees I'm on document the design standards, which I review. In my job of supporting tools, I have to understand the rules to do the tools. How do I need the tools to grow to do the best practices? I'm also on the Terms and Definitions Committee (2-30).

Shaughnessy: I heard that it was an interesting meeting.

McConnell: That is the best committee to be on because it is so interesting, and many diverse topics are discussed.

Shaughnessy: Because you not only have to worry about being accurate in English but also

choosing the right words so that it's translated correctly into other languages.

McConnell: Definitions are important because I can call something a ham sandwich if I define it right; that used to be a Dieter Bergman thing. Everything was a ham sandwich, and "ham sandwich" had a definition. If you don't have the definitions correct with no ambiguity, you don't have a common language. This year, the 2-30 Committee is in an ambitious revision. We looked at every definition in the document and decided if it was still used and needed to be defined for the printed board industry. For example, statistical terms were common enough that you don't need to define for the circuit boards.

Back in the day, when we were starting to make statistical process improvement, we had to explain what everything meant. That's not needed now, so we're removing a lot of terms. And we've revised a lot of terms to make them more meaningful. If you're defining a term, such as like lead, you can't use the term you're defining in the definition, so it's a challenge.

Shaughnessy: Or how "terminal" means "termination" to some people.

McConnell: Exactly. For me, that's one of the most important committees IPC has. It's about getting a common definition for us all to talk and share that's also translatable. Sometimes, we'll say things like, "I barely understand that in English, so how does that read if I translate it?" Then, we simplify the language so that it's not super technical. The definition should not give you the necessary criteria; it should give you the definition.

It was an ambitious goal. We are into our second time through the document discussion definitions marked that needed work. We have some more meetings, and then it will be ready for industry review. One of the neat things we did when we were deleting terms was discussed if there was be a reason to keep a term. We said, "Well, the experts could argue it back in if they want." That's why we redlined everything rather than removing the definition.

Shaughnessy: I spoke with Gary Carter and Michael Ford about the merging of IPC-2581 with CFX. That's going to be something. Are you involved with CFX?

McConnell: I'm the historian for IPC-2581. For many years, I was the lone committee meeting attendee. When I worked for Lockheed Martin, Dieter Bergman and I believed in IPC-2581, and so did Lockheed Martin. And when the industry had that downturn, a lot of people couldn't go to meetings, but we kept moving the standard forward. I was involved in the GenCAM wars and the peace negotiation, so I go way back with this. I'm a data person by heart.

A few years ago, IPC said, "We're looking for some area where there can be new leadership." Gary Carter had been in my committee, and one of the best things I did was ask him, "Would you like to be my co-chair, then move into my chair position?" Northrop wanted me to reduce the number of committees I had because there were too many. The best thing I did was step down and give it over to the people who knew how to write XML. I knew what I wanted to say, but I wasn't an XML expert, and I'm not a programmer. I'm a PCB designer at heart. I know what needs to be done, and the committee took it and went gangbusters. It is a great standard; I am so proud to see what it can do now and where it is going.

Then, CFX was amazing. I go to the committees. Their dial-ins are at a bad time for me, but when I can, I join their meeting and love what's happening. I'm pushing it at my company. This is what we want to adopt. I don't know how far I'll get, but I keep saying that this is what we need. I really like it; I think it is a great thing. In fact, I agreed with what Gary's trying to do in rebranding IPC-2581 from a number. There's a chart on the factory of the future, how everything works, and it forms the digital twin for you. It is the data for the digital twin.

Shaughnessy: In a roundabout way, this combined IPC-2581 and CFX standard will force the designer and the fabricator to talk to each other.

McConnell: Oh, yes; it gives them the means to talk to each other.

Shaughnessy: Switching gears a little, what do you think about this harmonization that IPC is pushing with trying to get IPC, JEDEC, and everybody else on the same page?

McConnell: It would be nice if it were harmonized. It's easier to work and talk together, but it takes time. It will happen over time because of the digital twin. How we harmonize becomes a difference. Do I have to use the same terms? Because that becomes expensive for IPC to change something with the number of documents that have to be written, such as "lead" to "terminal." Could I do something else, such as interchange the terms and definitions of "lead' and "terminal?" Then, when you do a major revision, you make the change. Right now, it's too soon, but it is something that we shouldn't drop; we have to keep an eye on that.

When I first started in the industry, IPC and JEDEC were very much in sync. I'm going to say that we were in sync when everybody had the money and time to be there. That's where the industry was; we were new and had to be in sync. Then, we had that bad period in the industry where nobody had the money, and we drifted apart. We did our own things. It happens in companies too.

Shaughnessy: A lot of people are retiring or have left the industry during the downturns, and there are fewer subject-matter experts at companies.

McConnell: I agree. A lot of retiring went on, and those that made it stayed but are approaching retirement age. Mil-aero experienced a few years ago what we called a gap in the industry. There was a time in this industry where nobody new was coming in. Now, we have new people coming in, but we don't have that middle engineer anymore. The people who retired or were laid off were the older end. The middle group that stayed are retiring. I'm even looking forward to my retirement in a few years. And some of us are not staying with IPC. It could be that IPC has to think, "We have a bunch of former SMEs who are now retirees. Is there some way

IPC can keep them involved even if they don't come to the face-to-face meetings without them having to pay to join IPC?" Because you have to be an IPC member to be a committee chair.

Again, I'm looking towards retirement now. But I either have to pay the IPC membership or drop my committee chairs. I haven't really talked about that with the management at IPC or TAEC, but I think that's something that I have to look at bringing up in TAEC because we do have a large number of people looking toward retirement.

Shaughnessy: A couple of people have said to me this week, "I don't know what I'm going to do. I want to be the conference chair, but I don't want to pay a lot of money each year."

McConnell: I could pay it now, but after I retire, I can't. So, that's going to be a problem in a few years.

Shaughnessy: But it sounds like you're having fun.

McConnell: I love getting together with my other IPC members, including sitting and talking at conferences and lunchtime breaks. I always try to find a table with an empty seat where I don't know anyone. Then, I meet the people beside me and hear interesting technical discussions that I probably would never have thought about. It has been a fascinating way to grow my knowledge of the industry, even after 30 years.

Shaughnessy: I appreciate your time, Karen. It's always great to talk to you.

McConnell: Thank you for covering this, Andy.

DESIGN007

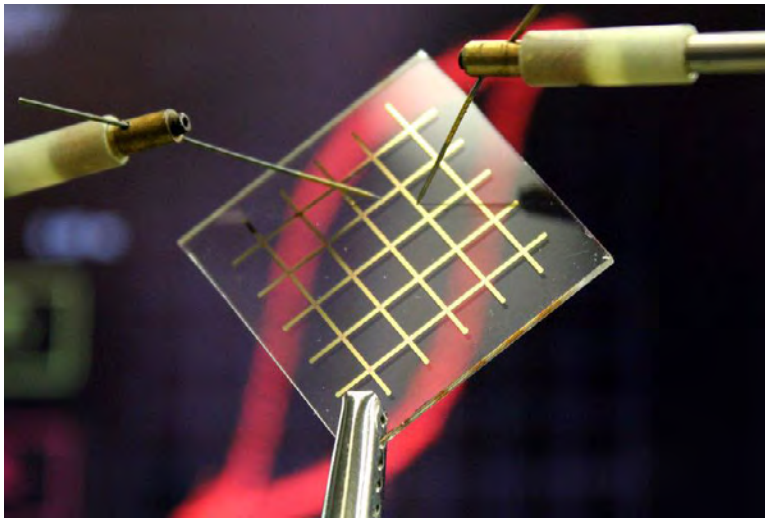
Nylon as a Building Block for Transparent Electronic Devices?

Scientists at the Max Planck Institute for Polymer Research (MPIP), led by Dr. Kamal Asadi, have solved a four-decade challenge of producing very thin nylon films that can be used in electronic memory components.

As the microelectronic industry is now shifting toward wearable electronic gadgets and e-textiles, the comprising electronic materials, such as ferroelectrics, should be integrated with our clothes. Nylon was discovered also to exhibit ferroelectric properties; positive and negative electric charges can be separated, and this state can be maintained. The ferroelectric materials are used in sensors, actuators, memories, and energy-harvesting devices. The advantage in using polymers is that they can be liquified using adequate solvents; therefore, they can be processed from solution at low cost to form flexible thin-films, which are suitable for electronic devices, such as capacitors, transistors, and diodes.

Scientists at the MPIP, in collaboration with researchers from the Johannes Gutenberg University of Mainz and Lodz University of Technology, have developed a method to fabricate ferroelectric nylon thin-film capacitors by dissolving nylon in a mixture of trifluoroacetic acid and acetone and solidifying it again in a vacuum. They were able to realize thin nylon films that are typically only a few hundred nanometers thick, which is several hundred times thinner than human hair.

These new findings pave the way towards multifunctional fabrics that serve as a cloth for our body, and at the same time, can generate electricity from our body movement. (Source: MPIP)



The Convergence: IPC Merging CFX With IPC-2581

Feature Interview by Andy Shaughnessy
I-CONNECT007

Gary Carter of XPLM and Michael Ford of Aegis Software are heading a group tasked with combining the IPC-2581 standard, now referred to as Digital Product Model Exchange (DPMX), with IPC's Connected Factory Exchange (CFX). During the IPC Summer Meetings, they sat down with me to discuss the benefits that can be expected when these standards are fully merged for both PCB designers and process engineers on the manufacturing floor, especially when it comes to satisfying compliance and traceability requirements.

Andy Shaughnessy: Nice to see you both again. And I understand the two of you are co-chairs on the committee that's working on combining DPMX and CFX. Tell me about that.

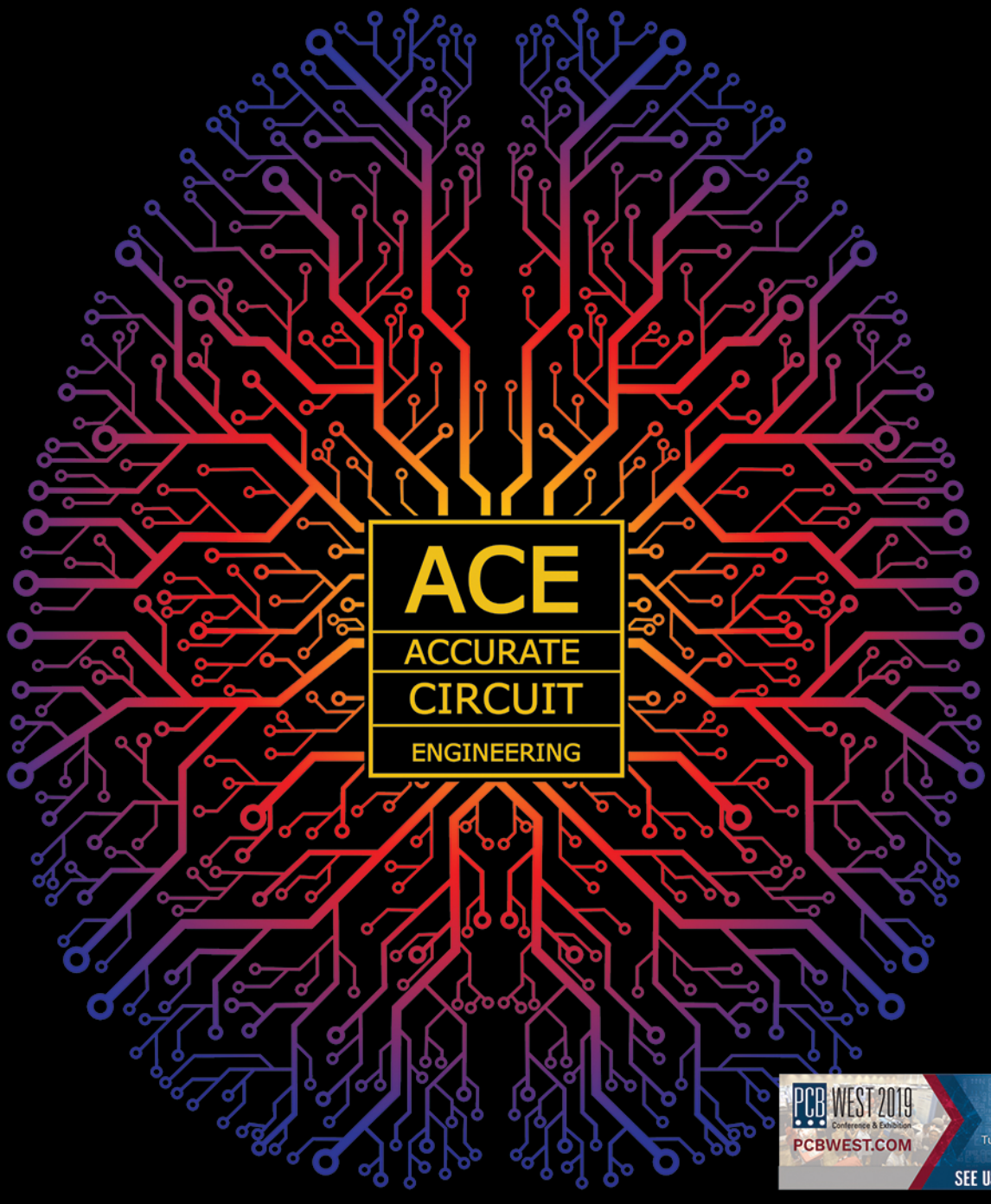
Gary Carter: Sure. The 2-10 Committee is looking to leverage the synergy between a number of IPC standards to describe now digital best practices that IPC owns, from beginning to end of design and manufacturing of PCB-based products.

Michael Ford: The strength of IPC standards is that each of them satisfies a particular need in the industry. DPMX is a great example where we needed to get an extremely complicated set of information from design to manufacturing in a single file. Why do we need to understand so many different files and try to put them together and cross-reference everything? It's the kind of role people would have had 20 years ago. Now, it's sent through in one digital format that has always been your digital product model for exchanging the data from design through manufacturing.

Another digital standard—the Connected Factory Exchange (CFX)—allows data to be exchanged between machines and factory systems. Put the two together, and you start to think, "Well, I have my digital product model exchange coming in, together with that from CFX, so I know what to do and how to do it. I can measure what I'm doing. Let's put those two things together. What benefit is that going to make? Couldn't I feed that information back through to design to make a complete digital loop for manufacturing?"

But this is not something that you have to buy. This is something that is a digitally created

Don't Overthink Your Prototype Builds



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Gary Carter

technology IPC standard so that everybody can use it. There's no real cost to ownership. You can choose your favorite engineering, design, or manufacturing tools. The nice thing is that digital best practices are now defined by IPC through DPMX, CFX, and even our traceability standard, IPC-1782, which defines the type of information that needs to be retained by manufacturing to satisfy compliance and traceability requirements.

Shaughnessy: How long have you all been working on this?

Carter: The last year and a half. We've been talking and co-presenting in some venues and brainstorming on other IPC standards that add to this value proposition and need to be a part of this story.

Shaughnessy: It seems like there would be some natural hurdles; design data is one type of data, but CFX is a different animal. How do you blend the two?

Ford: It is, though DPMX consists of many different kinds of data, and that data is exactly what is needed in manufacturing, by machines, for example. Even before we started this project, there were cases where DPMX data was used by particular machine vendors because they needed access to the design information to understand where the components were supposed to go, what measurements they were supposed to take, and what they should expect to see in visual inspection.

As far as translating the standard design format into a standard manufacturing format, it's the same data source, but sections of the data are being used for the different manufacturing processes. So, CFX already carries the ability to take the data derived from the design and out to the machines. We're improving on that as time goes on. We're collaborating in terms of the definitions of the standard so that we can be more specific and make it easier for machine vendors, for instance, to understand the layout of this board in terms of X, Y, and Z, and know how to get that data through CFX, which is derived from DPMX.

This flow, which would have taken an engineer hours if not days to achieve, can be done with the hit of a button because the information is now standard. It doesn't matter where it came from or where it's going in terms of engineering tools because it's the same format.

Shaughnessy: Gary, you mentioned how traceability was a big part of this. How is that working?

Carter: Traceability has become a big concern, especially with counterfeit components and knowing the provenance of the materials that you are using. CFX is able to close the loop with what occurred on a line during manufacturing assembly and test. Now, you're able to have a complete record of what your product was made of, where it was operated on, how that material moved or didn't move properly through the process, and identify where your problem areas are. Further, you can do a full Six Sigma analysis that tells you what happened, why it happened, and what you need to do to eliminate it from happening again if it's not the desired outcome.

Ford: Think of the sheer power this brings back to people. Let's take your phone, for instance. There's going to be a design for that. And do

you think you make it according to the design? No. People will come along and say, "Making one phone is not going to be very practical. We're going to put it on a board and make 16 of them at the same time. And we can't buy the material that you specified in the design in China, so we're going to buy something else." Does that mean it's the same size, footprint, or quality? Not necessarily. Then, you end up with phones in the market that have issues. Nobody knows if it was due to the design, materials, the change in manufacturing, etc. Now, you could find out.

With traceability data, in the past, you didn't want to capture anything beyond what was immediately specified for a specific need, because it cost you money; now, it's free because you're getting the data through CFX. The IPC-1782 traceability standard lays out where all of the data will come from, which can then even go back into your design tool to statistically analyze opportunities to improve the decisions you make for manufacturing.

Shaughnessy: Are you in beta with this?

Ford: Many companies are starting to work with this idea, but we're in the early stages of putting this together. We want to be sure that the standard itself is clearly defined because IPC is consensus-based. Many companies in the industry are already interested in this and want to make sure that we satisfy everybody's needs, so that's step one.

Shaughnessy: Are there any other hurdles you see ahead? Just organizing it seems like the biggest thing.

Carter: There are a few standards we would like to create a schema structure around so that we can eliminate that last group of notes that requires some sort of human interpretation and re-entry downstream. But beyond that, I don't think we have any big challenges from a technical perspective.

Ford: All of the standards have been developed using IPC guidelines, so they are quite compatible with each other. The terms and definitions are pretty close. And the people who we've presented this to understand it. They think it's amazing and should be pursued. In one year's time, we're going to be doing this.

Michael Ford

Shaughnessy: Do you think it will take off?

Ford: The benefits are there. We see the kind of turmoil going on in the world now where people need to do local, flexible manufacturing. They're losing sight and control of what they need to make day by day. They need digital solutions to be able to do that, but you can't afford to buy those solutions from 20 different vendors, and they're all incompatible. People are realizing that it's standards first, but don't take five years on it. Do it within the next few months. Let's get a handle on what we need to do because we need to get this value into manufacturing that's going to seize the maximum opportunity and get the most profit from all of the necessary relocations or reconfigurations of what they are going to go through.

Shaughnessy: This won't change the way a designer does their job, right?

Carter: It will give them a lot more visibility about what is going on with their product when it hits the factory floor.

Shaughnessy: It will create more communication between the designer and fabricator, which is almost nonexistent sometimes because designers often don't know where it's going to be fabricated. But this way, it will be bidirectional.

Ford: Yes. You can imagine the kind of frustration from a designer's point of view. They make the design that they think is absolutely perfect, and they review it with their peers. Six months later, they hear that there are problems in manufacturing and in the market. "You didn't do a very good job on that design." They might say, "It's not my fault. You're using materials that are completely different from what we specified. You're using machines that are incapable of producing that kind of board."

For the first time, the clarity is there. And it's presented to the designer in a way that they understand. Statistics tell the designer that this is something that needs to be changed to accommodate the use of different materials or processes; they don't need to understand materials or processes themselves, but they will understand the need, and that's what we bring back in terms of statistics so that their world is the same. But it's so much more valuable to have all of the information that designers need to make design decisions.

Shaughnessy: So, if the designer needs to look downstream and see what kind of material they switched to in Shenzhen, all of that will be brought back.

Carter: With the digital product model exchange, they should be able to model that upfront. The stackup exchange is one of the features we added to DPMX some time back. You'll be able to have that upfront negotiation and say, "These are my impedance requirements and edge rates, and this is the kind of product it is. What materials do you have in Shenzhen?" In the case of the actual materials that your contract manufacturer might be doing substitutes on, now, you have a way to collect the as-built conditions. For example, you could say, "Wait a minute; that one's not equivalent. It may have saved you a dime, but there's the root of the problem."

Shaughnessy: What are you going to call the combination? Is it going to have a name?

Ford: It's going to have an X in it. That's all we know at the moment (laughs)! We have CFX and DPMX, and we're putting together this as a whole digital manufacturing engine exchange. "X" means excellent and exchange.

Shaughnessy: And they'll be communicating whether they want to or not.

Ford: They're going to have to because manufacturing is changing. Instead of being six months of planning, it's six days. Getting information digitally and being able to snap your fingers and make things happen on different production lines and configurations and materials is the future; as a matter of fact, that's what's happening now. People can't click their fingers; they have to do it manually, which is a real cost for them. But this is essential for modern manufacturing. If people want to continue making progress with their customers and expanding their business, this is a necessity. You can't do it with human beings alone.

Shaughnessy: And it will bring designers into smart manufacturing. If you ask most designers what they think about smart manufacturing, they'll say that they don't have any thoughts on it. But if they start using this combination, that should change.

Ford: Yes. They're going to get a lot more enjoyment out of not having problems with any design, especially ones that are not their fault. And it will let them see any opportunities to improve.

Shaughnessy: It has been great talking to you. Thank you.

Carter: It's our pleasure.

Ford: Thank you for your time. DESIGN007

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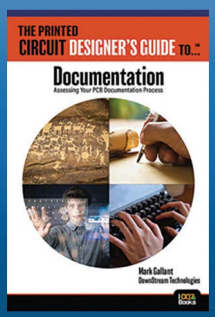

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Why Does the PCB Industry Still Use Gerber?

Feature by Karel Tavernier
UCAMCO

Every so often, I hear technologists ask why so many PCB designers still use Gerber. That is a fair question. Ucamco has over 35 years of experience in developing and supporting cutting-edge software and hardware solutions for the global PCB industry. Our customers—small, medium, and large PCB fabricators—include the electronics industry's leading companies, and many of them have been with us for over 30 years. We are dedicated to our industry and excellence in everything we do, which includes our custodianship of the Gerber format.

Data Intelligence

With us, the Gerber format has undergone a significant evolution in the past 10 years, and a near revolution in the past five years alone. Like the previous Extended Gerber (X1) format, today's Gerber X2 is simple, easy to use, and freely available to our industry, but simple and free doesn't mean dumb—far from it. Thanks to the use of cleverly designed attributes, Gerber X2 is an intelligent format that can do all of the things that some critics say it can't. Gerber X2 can differentiate between pins, vias, and traces, and anyone who cares to read section 5.6 of the Gerber X2 specification will see that it does so in more detail and with greater precision than the ODB++ and IPC-2581 formats.

The industry's professionals know this because we talk with our customers daily and listen very carefully to what they tell us about being at the electronics production coalface. What they tell us is confirmed by a quick glance at the industry's use of the different formats. IPC-2581 is used for a negligible fraction of the world's fabrication data sets, ODB++ is used for 5%, Gerber X2 is used for 10%, and the rest—the vast majority—uses the traditional Gerber X1 format.

Supporters of ODB++ and IPC-2581 point to the "intelligence" of these PCB data formats, but Gerber X2 is the global PCB industry's most popular intelligent PCB data format. Sure, these formats are more intelligent than the old Gerber X1, which can't differentiate between SMD and BGA pins. But when ODB++ was launched, it did not contain any component information either.

Figure 1 shows an apples-to-apples comparison of ODB++, IPC-2581, and Gerber X2. These

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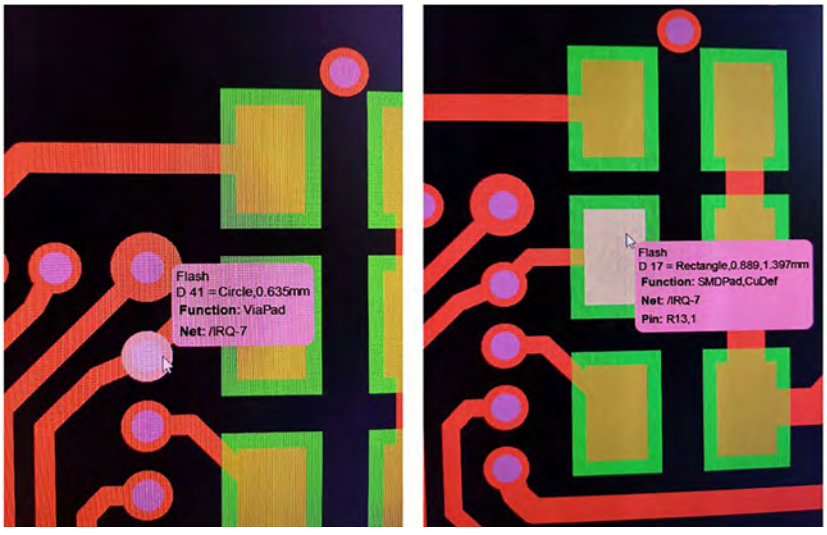

Figure 1: Output from a popular CAD system illustrates that Gerber X2 fully identifies pad types, sizes, nets, and pins.

screenshots from the Reference Gerber Viewer illustrate the level of information carried in a current Gerber X2 file. The pad selected on the left is identified as a via pad, and the pad selected on the right is identified as a copper-defined SMD pad, and as pin 1 of R13 with net / IRQ-7. With Gerber X2, a designer can easily distinguish between a pin, via, and trace.

As you can see, any claim that Gerber is "dumb" is wrong and misleading.

Directories and Files

Some detractors claim that Gerber's files and directories are awkward to use. But realistically, a zipped directory with ODB++ files is no different from a zipped directory of Gerber files. Furthermore, a typical ODB++ package is not even a single directory but a complex directory structure. To be fair, the IPC-2581 package is a single file, even before zipping it. This can be seen as an advantage, but it can be seen as a disadvantage too. Individual layers—such as AOI or imaging—must often be accessed during fabrication, so storing these layers in separate files (as in Gerber and ODB++) makes their extraction easier and cleaner.

DFM

Other naysayers claim that it is not possible to generate full and meaningful DFM reports from Gerber files. Figure 2 shows part of a QED report generated by Ucamco software from a Gerber job. The first block shows the rings categorized by vias, laser vias, component pads, and mechanical pads. The last block shows the clearances to outline split by pads, tracks, and copper pours. Clearly, meaningful DFM reports can be generated from Gerber files.

Evolution

For some users, the fact that Gerber has—apparently—remained unchanged is another no-no. Apart from the fact that Gerber has indeed evolved over its lifetime and continues to do so, let's go with this. Let's take the automotive industry's steering wheel. This has been, well, a wheel, since 1894 when Alfred Vacheron took part in the Paris-Rouen race with a four-horsepower Panhard model that he fitted with a steering wheel instead of the then-popular tiller. It was such a great idea that within a decade, the vast majority of new cars had steering wheels. The round shape was a winner, and its position at the front of the car was a pretty good idea too.

That was 125 years ago, and guess what? Steering wheels are still round, in the front, and used to direct cars. Nobody would say that they haven't evolved because they're not square or attached to the roof of the car. Steering wheels have kept what works and have evolved with automotive steering and safety technology, integrating in-car entertainment and comfort features on the way. This is a bit like Gerber. Like the steering wheel, Gerber has stayed at the front, keeping what works, while the rest of this free, open format evolves to keep abreast of and drive beneficial developments in PCB design and engineering.

Why Use Gerber?

One common question I hear is, "Why do designers still use Gerber?" I believe that designers have very solid grounds for their reluctance to drop what works in favor of a new format. It is not that these new formats are bad—

Copper Layer Minima - Copper vs Drill - Original

File	Pos.	Ring					Copper to Plated Clr.	Copper to NPTH Clr.	Copper to Outline Clr.			
		Overall	Via	Laser Via	Comp.	Mech.			Overall	Pad to Outline	Track to Outline	Region to Outline
		mm	mm	mm	mm	mm	mm	mm	mm	mm	mm	mm
TOP_art	1	0.062	0.125	0.062	0.300	0.000	0.150	0.301	0.625	0.625	0.645	1.044
INTERNE1_art	2	0.062	0.124	0.062	0.275	0.250	0.138	0.087	0.540	0.600	0.867	0.540
INTERNE2_art	3	0.062	0.150	0.062	0.275	0.000	0.138	0.301	0.600	0.600	0.763	>1.600
INTERNE3_art	4	0.062	0.150	0.062	0.275	0.000	0.138	0.255	0.555	0.600	0.555	>1.600
INTERNE4_art	5	0.150	0.150		0.275	0.250	0.237	0.087	0.540	0.600	1.550	0.540
INTERNE5_art	6	0.000	0.000		0.300	0.250	0.237	0.087	1.050	>1.600	1.417	1.050
INTERNE6_art	7	0.000	0.000		>0.800	>0.800	0.237	0.087	1.100	1.145	1.550	1.100
INTERNE7_art	8	0.150	0.150		0.275	0.250	0.237	0.087	0.540	0.600	1.550	0.540
INTERNE8_art	9	0.062	0.150	0.062	0.275	0.000	0.172	0.202	0.600	0.600	0.748	1.100
INTERNE9_art	10	0.062	0.150	0.062	0.275	0.000	0.150	0.087	0.396	0.396	0.571	>1.600
INTERNE10_art	11	0.062	0.124	0.062	0.275	0.250	0.150	0.087	0.540	0.600	1.550	0.540
BOTTOM_art	12	0.062	0.125	0.062	0.275	0.000	0.162	0.301	0.625	0.625	0.904	1.094

Figure 2: A QED report generated from a Gerber job shows detailed DFM data.

they are not. But to gain access to the meta-information they contain, you must adopt them wholesale, and that includes a new image format. The problem is that image formats are notoriously hard to implement.

Much has been written about just how complicated geometric software is and how much effort it takes to get it right, not to mention the years it takes to debug. And that is a big consideration for anyone thinking about adopting a new format. Errors in image transfer are catastrophic as they inevitably lead to scrap. Gerber's image functionality has been thoroughly tried, tested, and debugged over many years, which is why the global PCB industry knows that its PCB data is safe with Gerber. Can the same be said of IPC-2581? How many jobs does this format have under its belt?

It's also worth noting here that a huge portion of PCB software is developed by tiny companies, often one-person outfits. For larger companies, implementing ODB++ (let alone IPC-2581) is already difficult enough, but for these smaller companies, it's a massive—and often prohibitive—undertaking. Compare this with the ease and simplicity of adding attributes to an existing Gerber implementation. Gerber X2 offers developers a straightforward, affordable, effortless way to add "intelligence" to their input/output, allowing companies of all sizes to participate in the growth and advancement of the global PCB industry. Similarly, it's very easy for designers and fabricators to implement Gerber X2 as it's compatible with X1, so if the software being used cannot handle X2's new meta-information, it can just skip it and continue to work as before. Easy.

So, why does the PCB industry still use Gerber? Because it is the very best PCB data format out there. Gerber offers our industry a standard with a great image specification that is trustworthy and easy to implement and use, and it has evolved over the years as intelligence has been added to the image data. Ucamco is dedicated to excellence—its own, that of its customers, and that of the industry. **DESIGN007**

References

1. Visit the Reference Gerber Viewer and download a sample job here.

Karel Tavernier is managing director of Ucamco.

Emma Hudson on the Harmonization of Standards

Feature Interview by Andy Shaughnessy
I-CONNECT007

At the IPC Summer Meetings, I spoke with Emma Hudson, CTO at Gen3 Systems, about the current movement to streamline and harmonize IPC's standards with standards from other global organizations. We also discussed what could be done to accelerate standardization to better keep up with changes in technology.

Andy Shaughnessy: Nice to meet you, Emma. Can you give us a little background on Gen3 Systems?

Emma Hudson: Gen3 is based in the U.K. We manufacture and distribute test equipment for high-reliability electronic applications. We are looking at SIR and CAF testing. We have the wetting balance. And ionic contamination is a big thing, so we make the Contaminometer, along with several other pieces of equipment.

One of the things that we have been doing a lot of at IPC this week is talking about the test methods for ionic contamination and looking at the harmonization—something that Gen3 is heavily involved in regarding standards work. We are with IEC and IPC, and I am also involved in UL standards work. I am currently the chair of the British Committee and the convener of Working Group 2 for the IEC Electronics Assembly Technology Technical Committee.

Further, we have clarified the test methods for SIR and process ionic contamination testing, including the process characterization using SIR and ionic contamination that we've seen with the changes going on with J-Standard-001 right now. We have created those test methods with IEC and are bringing them into the IPC committee meetings as well so that we can try and get some harmonization. The industry needs harmonization of standards.

Shaughnessy: Yes, it was pretty astounding hearing about all of these different global standards organizations, and many of them creating standards that overlap each other. It makes you wonder why we can't get them all on the same page.

Hudson: I agree. Being involved in the standards, you are often repeating the work. As an industry, and as someone who makes equip-

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ment and gets asked by our customers about standards, you realize that ideally, you just need one set of standards that is going to do the job. As I mentioned earlier, we are members of IPC, and IPC is the representative of the American National Standards Institute, so are the U.S. National Committee representative for IEC. With IEC, it's one country, one vote; with IPC, it's the manufacturing sites that get the vote.

IEC and IPC have slightly different takes and ways of approaching standards, but each with their good points. IPC via ANSI will bring in some of their standards to IEC, and we'll try to adopt them, and vice versa as well. We also have standards that are developed through IEC that we will try to bring to IPC, if they are suitable, to get them adopted here. In our industry, we need one set of standards. In essence, there's no allegiance to any standards or organizations; we just want to have a single set of standards to buy.

In our industry, we need one set of standards. In essence, there's no allegiance to any standards or organizations; we just want to have a single set of standards to buy.

As a company, the cost of buying standards is something that has quite an impact when you're being asked, "Do you meet this IEC, IPC, or JEDEC standard?" I've also been asked about VDA standards recently. There are so many standards, and you have to buy each one, read it, and see if you comply. Often, there are many similarities, and it can be a burden on a company. Thus, standardization and harmonization of standards for the global market is a key thing that we, as an industry, need to focus on.

Shaughnessy: It's too bad that there's not a way for an umbrella organization to get everybody to play nice.

Hudson: Yes, IEC is quite good for that, because it is one country, one vote. Organizations like IPC, who have the ANSI accreditation, have become the U.S. National Committee representative and regularly bring their work to IEC. There are Japanese, German, Korean, and British committees, just to name a small number of the members of Electronics Assembly Technology Technical Committee. We can each bring things together, and we have that international forum to work through the material and try to come to a consensus. But it is difficult because many other organizations are outside of IEC but industry-specific. Trying to bring them all into one umbrella organization would be idyllic. But above IEC and ISO is essentially the World Trade Organization. IEC is one of those organizations that is trying to umbrella the various national committees and standards coming up, but it is difficult.

Shaughnessy: Are there any steps that you think would be fairly simple to put into action?

Hudson: We do need to speed standards up. One of the things we talked about recently in working group meetings in Frankfurt for the IEC-TC91 group was the use of things like technical reports and trying to get information out there quickly. But you have to be careful because it is easy to write a bad standard with some wrong numbers. As soon as you do that and it is established, you have much bigger problems trying to fix it.

One of the things we talked about today was getting younger engineers involved and bringing the right people together. It is difficult because there are expenses to flying people to various meetings, including the time you are away from the day job, but there are some things we can do. We need to use technology more often, such as conference calls, where we can still talk rather than meet in person. We can also use A-teams or specialized groups;

both IPC and IEC have done this. The smaller groups focus on a given standard and drive it forward whilst still allowing the wider audience to have a say.

Shaughnessy: Yesterday, a new committee member said, "I cannot believe we spent all that time talking about one page." But that's how it is.

Hudson: Right. But to some people in that room, that was an important part of that standard. Terms and definitions have been brought up this week a lot, such as "lead" vs. "lead." When you read it, you see it is the same four letters. If you are English native-speaking, you may be able to differentiate between them given the context of the sentence.

Shaughnessy: And if it is in Kanji, is it the same character?

Hudson: Exactly. People from the outside world may question why we're spending so much time looking at this, but when you get down to it, these items can be critical. But we need to find a way to accelerate standards and drive them forward to keep up with new technology. One of the classic things I hear with standardization work is that they never keep up with technology, which is a difficulty. We need to find ways by using modern technology. For both IPC and IEC, there is a form you fill out, which can take time. I understand that JEDEC has an online approach to doing this.

Shaughnessy: IPC has been talking about trying to make everything digital for a while.

Hudson: Yes. We have been talking at committee meetings this week about the use of digital rights management, even on draft standards now, because IPC has found a lot of its content out on the internet. We want to make it digital, but we have to make sure that we are protecting the intellectual property of that standard. Each standards organization will want to sell those standards. Ideally, we need to start making the whole process more user-friendly and IT-based. As younger engineers come through, that is a natural way of doing things for them.

Shaughnessy: I spoke with a few first-time committee attendees, and they said, "Wow." They had no idea how much went into standards.

Hudson: The first IPC standard I used was 610 because I was in automotive electronics assembly. We were building something new and looking through IPC-A-610, and when I attended a meeting on it, I said, "Wow," too! Then, you really appreciate the decisions being made in those meetings. Today, a man from Lockheed said that he didn't necessarily understand where "25% of components over the pad" had come from. Suddenly, he was in the meeting and said, "That's why we have standards."

Shaughnessy: And I have to say, there are a lot of women here at the IPC Summer Meetings.

Hudson: It's great to see the number of women attending grow each year, but there are still not enough. However, that has nothing to do with IPC or IEC; it has to do with the fact that we need to get more women into engineering and STEM positions in general. We need to make girls understand that these are great careers; it's not all "oil under the fingernails." Engineering has given me a great career. I travel around the world and love it. I've met some wonderful people.

Shaughnessy: It is a great industry.

Hudson: Really, this industry is a family. You look forward to going to these meetings to meet people and talk about what is going on and the new technology.

Shaughnessy: We also have 5G and all the smart manufacturing and Industry 4.0 coming online.

Hudson: 5G was a big topic at the EIPC conference last week when we were in Austria. Ericsson presented a paper on 5G and all of the challenges we have in the industry and making sure the right materials are there. 5G is something the industry needs to be switching to because it's coming quickly and has been building for a while.

Shaughnessy: We need to straighten out that Huawei issue. Is the U.K. wary of them? In the U.S., the attitude is that Huawei cannot be involved in our 5G.

As an electronics industry, we are a global industry. And to now have to let politics come in and stop things is another reason we need to harmonize standards.

Hudson: It has been interesting in the U.K. There have been some discussions about allowing Huawei to be involved in certain aspects of 5G. There have also been some political conversations and clarifications with Trump's visit to see Theresa May recently. It came up in the standards meeting. We have to be careful about sharing information with people on the U.S. Entity List as it may break your government export ITAR-type rules. It's all goal posts at the moment, and they seem to keep moving. As an electronics industry, we are a global industry. And to now have to let politics come in and stop things is another reason we need to harmonize standards.

In Europe, we are lucky in the sense that if you buy a product in Europe, essentially, you know it is going to meet those same standards. And harmonization says that if we can have those single international standards, at least we know when we buy a product that it is going to meet certain quality, reliability, and safety levels; that has to be fundamental.

Shaughnessy: I cannot believe we have not standardized on metric or imperial.

Hudson: The U.K. is awful on this because we sometimes use both. I was taught in metric, but we still use miles with things related to automotive; for example, all of the road signs are still in miles, but when you go to Europe, it is all in kilometers. The U.K. is still in that transition zone of whether it should use metric or imperial, it often depends on your age with which way you want it to be. I have to ask people what units they're using when I talk to them. But we still talk in ounces of copper for weight but microns for thickness. We'll get there in the end.

Shaughnessy: It sounds like you have a fun job.

Hudson: I do, I love it. I am very lucky. It's been great working for Gen3 in this new role. I love that they support standards work; it keeps my brain active and challenges me. Attending industry events is great for networking as well.

Shaughnessy: How many people are in the company?

Hudson: We're growing and have over 20 in the U.K. now, which sounds quite small, but we have an international customer base, including many large companies.

Shaughnessy: It has been great talking with you, Emma. Thank you.

Hudson: Thank you, Andy. DESIGN007

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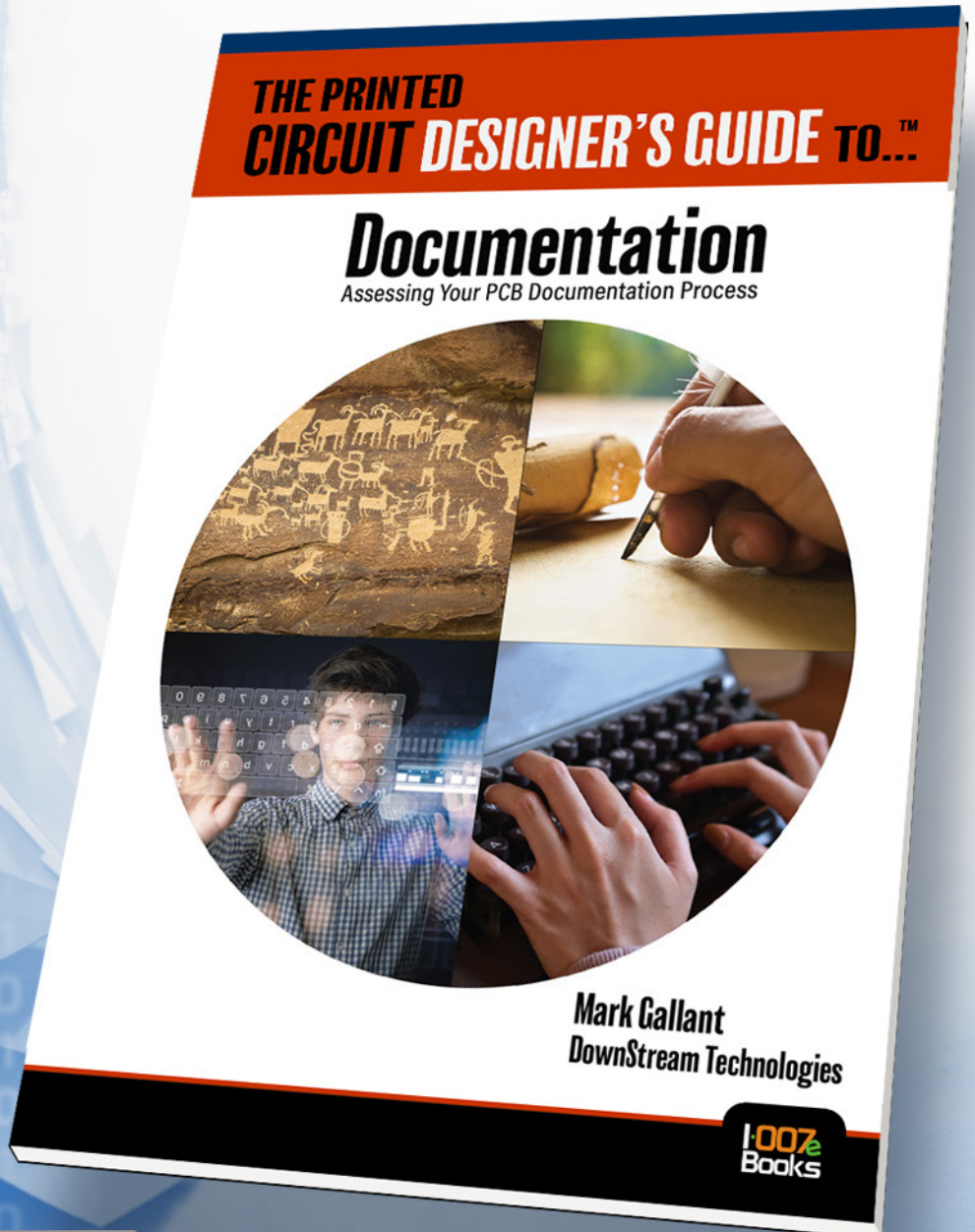

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So Many Standards Committees, So Little Time


Leo Lambert

Feature Interview by Andy Shaughnessy
I-CONNECT007

During the IPC Summer Meetings and Panelpalooza in Raleigh, North Carolina, I met with Leo Lambert, vice president and director of technology at EPTAC. We discussed IPC's recent efforts to revamp the way standards are developed and interpreted as well as changes to training and education committees and a variety of methods for eliminating errors and duplicated comments when revising standards.

Andy Shaughnessy: Another day, another show, Leo. You're the chair for a couple of committees, so can you tell us what your committees have been doing at the summer meetings?

Leo Lambert: Back in the day, I was the chair of the J-STD-001 task group of the Assembly and Joining Committee; now, I'm the chair of the IPC-A-600 Committee. IPC is reorganizing and taking a look at the way the standards are being developed, the way the standards are interpreted, and how the test programs are going to be conducted. There are also new sets of policies, rules, and procedures for the training programs—one for CIT/MIT, one for CIS, and one for CSE—which everyone is anticipating. They have released the initial version, but there are still corrections that need to be addressed and implemented.

In the meantime, this delay creates a lot of angst for the people who are using them, and we had a meeting this morning on some of those issues. Today, we had training meetings, which are very important to the development of the programs; however, everyone wants to attend all of the meetings. Therefore, with so many people involved, it is difficult to reach a consensus in a short period of time since everyone has some input and want to be heard. I understand wanting to attend all of the meetings, but then you realize that there are only so many hours in the day, so it is slow-moving.

Since we're involved in the training business, we need to go to the training meetings because that's the material that we're going to be using and presenting to the students. Additionally, there are many mistakes in those documents that must be corrected, and the new IPC organization is addressing all of these. However, it will take time and patience. These errors are repeated at each training program by all of the

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training centers, and multiple inputs are sent to the IPC, which become difficult to address in a timely manner.

That's the topic of discussion that we're organizing for the training meetings: how to update the programs in a timely fashion. Although it sounds simple enough, many of the trainers at these meetings also attend the specification meetings, which causes conflicts in everyone's schedules. Thus, scheduling for meeting participation is difficult for most of the attendees of the technical meetings.

Shaughnessy: Tell us about the new group at IPC.

Lambert: A new higher-level training and education committee was created to get a better understanding of those tasks, and those committees were creating sub-groups to service the various specification task groups. The training committee is looking at it in the perspective of the way the questions are written. Historically, IPC put questions together and submitted them for the training classes; now, IPC wants to know who's going to write the questions and verify that they're valid and defensible. IPC is also creating more controls over the use and application of the certification exams. Certain groups are being selected to create and review the questions, but these individuals cannot be instructors in those disciplines. IPC is creating additional questions to store and use, which will eliminate the memorization of the questions as was done previously.

To encourage new technology input into the specifications and other documents, IPC has now asked to accelerate the document development as they want the documents to be updated every three years from a five-year schedule. This is presenting problems for the developers of the training programs to get the new programs out to the training centers in a timely manner. Previously, there was a sense that when the document came out, the training program would also be released. Getting the training programs out in the shorter time frame forces the reviewer to rush, and thereby miss many of the errors in the document. There were often a lot of mistakes in the newly released training program because the information had not been approved at that time. Now, IPC is saying the training program has to come out after six months at the most. That gives us a little bit of time, but it's always a rush, so we will see what the results will be when the first couple of programs are released.

Shaughnessy: I know IPC didn't like the idea of having the Summer Meetings at SMTAI because that was only a couple months before IPC APEX EXPO, so it wasn't enough time for everyone to make the changes.

Lambert: Right. We still have our own jobs to do, so that doesn't help. It's a busy time.

Shaughnessy: I heard that the T-50 terms and definitions meeting was interesting this week, discussing "lead vs. lead" and how the term "terminal" also translates into "termination" in some other languages.

Lambert: I remember when we had that discussion when surface-mount first came out. We soldered everything to pads and then to lands, referring to land area. And you're right, "lead" and "lead" are spelled the same way, and when you look at it in the document, how do you translate it? We have to address that because the documents are used globally. The T-50 people try to put the new definitions in the existing specifications, so they're going crazy with all of the words. After the new words are in the specification documents for a couple of revisions, then those definitions will be relegated to the T-50 document.

Shaughnessy: And then you need to consider whether a similar term is going to be a different character in Mandarin, right?

Lambert: This past week, we were talking about Spanish. There's Castilian Spanish in Spain, but what about people in Mexico and Latin American countries? It's a different language, and IPC is trying to pick one that's good for

everybody. I'm not a linguist. I have enough trouble with the English language! But IPC has to take care of all of the rules of the English language, and some of the phraseology that we use is odd. In some documents, there would be a dime next to an object, trying to show the size relationship between the two objects. Who knows what size a dime is except for the people in the United States? You can't use a dime for global documents; you have to use something else.

Shaughnessy: Is this something that IPC President John Mitchell is pushing to try to streamline, or is it the chairpersons?

Lambert: New people are coming in with different educations, so that's part of it. John Mitchell is an educator to start with, and IPC is looking to get more involved with the vocational schools, two-year colleges, four-year colleges with PCB design, etc. There's a lot of effort going on in that direction. As the leader of the group, you can't get involved with the minutiae that we work with. John Mitchell is working those deals, and Collette Buscemi is focusing on education through the foundation. I want to try to work with her because I'm involved with UMass Lowell.

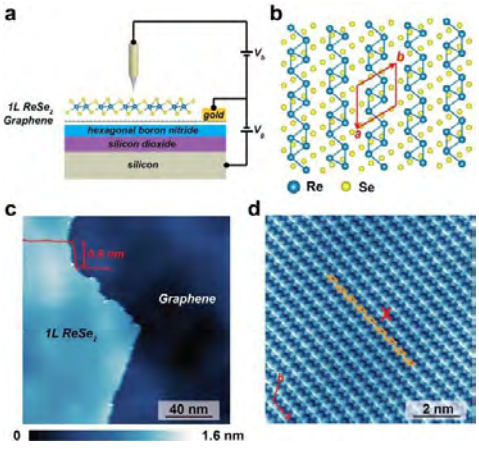
IPC wants you to talk to students. They have pockets within the United States that they're working on, but in Massachusetts, they didn't have anyone. I said I would help. When I used to talk to young people, they'd have no idea about this industry. Now, they're building robots, and we've trained a couple of professors so they're familiar with 001 and can teach it, which helps. IPC is also offering scholarships and working internships so that when students graduate, they'll have experience and can get hired.

It's a generational thing, and it won't happen overnight. I've been coming to IPC meetings for a long time, but you can't be involved in everything, so you have to pick and choose.

Shaughnessy: It has been good talking to you, Leo. Thanks for the update.

Lambert: My pleasure, Andy. **DESIGN007**

Control of Excitons in a 2D Semiconductor



National University of Singapore (NUS) scientists have developed a method to control the binding energies of excitons in a 2D semiconductor for advanced photonic and optoelectronic applications.

A research team led by Professor Lu Jiong, department of chemistry, has developed a method to control the excitons in a thin layer of rhenium diselenide (ReSe2) by adjusting the electron density in the underlying graphene film using the electrostatic gating effect, a method to modify the carrier concentration of atomically thin 2D materials by the application of an electric field. An increase (decrease) of electron carrier density in the graphene film will decrease (increase) the Coulomb interaction strength between the interacting excitons in the ReSe2 layer. By controlling the electron carrier concentration in the underlying graphene substrate, the researchers could control the electronic band gap and exciton binding energy of the monolayer ReSe2 by up to hundreds of milli-electronvolts (meV).

In their experiments, the researchers demonstrated that the exciton binding energy of the monolayer ReSe2 could be continuously tuned from 460 meV to 680 meV by electrostatic gating.

"The ability to precisely tune the band gap and excitonic effects of 2D semiconductors on graphene devices could provide new insights into the band alignment and exciton dissociation at the interface of 2D semiconductors and graphene. This could potentially reduce the interface contact resistance and improve the light-harvesting efficiency of such optoelectronic devices," said Professor Lu. (Source: NUS)

ODB++: Transforming Ideas Into Products

Feature by Max Clark
MENTOR, A SIEMENS BUSINESS

Figure 1: The painted lady butterfly. (Source: Renee Grayson)

This year, I witnessed an impressive natural event that I had never experienced before in all my life as a native Californian. The painted lady butterfly migration starts from the southeastern deserts of California heading northwest to Oregon, Washington, and further north into Alaska (Figure 1). While that distance covered by a butterfly with a wingspan of 2–3 inches is amazing, what was so impressive was the sheer number of them. This year's migration represented one billion butterflies, all striving to survive the long journey north. Throughout California, one could simply step outside to witness the most elegant stream of butterflies, one after the other, for days on end.

What does a butterfly migration have to do with transferring intelligent PCB data from design through the manufacturing process? The process of transforming from an earthbound caterpillar into a beautiful flying butterfly where each has a unique wing pattern is not much different than transforming an idea for a product into a schematic, and through hard work, into a unique PCB design. The difference is that nature has created a perfectly connected process, but we still are challenged doing our same process repeatedly with positive results. In the case of a PCB design, the transfer of the design intent and the manufacturing process needs are not yet connected in unison.

The ODB format originated with the objective of delivering on this need (Figure 2). The format was originally introduced for use by PCB fabricators, eliminating the need for a collection of CAM files in multiple formats—such as Gerber, Excellon, IPC-356, or even IPC-350, which was an early attempt to simplify this process. The key to the success of

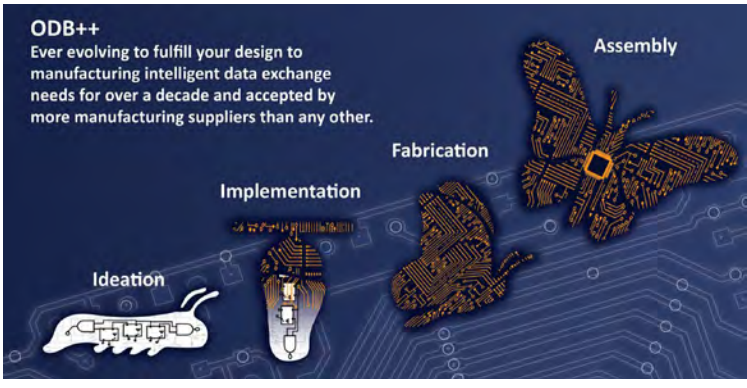


Figure 2: ODB++ helps users transform their designs into a final product.

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ODB was that it obtained industry acceptance. There was a friendly, informal group working together as early adopters put aside their previous thinking in the hopes of achieving a quick transformation from an effective product model into a deliverable PCB with the minimal amount of data manipulation possible, and in an effective, repeatable, and reliable manner (Figure 3).

Like the transformation of a butterfly, the creation of a PCB from design into manufacturing is complex. When assembly information was added to the ODB format, resulting in the ODB++ of today, this added additional demands to the format (Figure 4). This continued complexity was highlighted in a 2014 Aberdeen Group Study [1] in which 44% of respondents indicated that the top challenge in PCB design data management is the complexity of data followed by the integration of that data into management processes, data exchange, etc.

This article will discuss how ODB++ began addressing these challenges over two decades ago, and how ODB++ will continue to evolve based on the needs of the industry. ODB++ was always, and will always be, open to the community to support required additions and changes as industry processes and demands are ever-evolving.

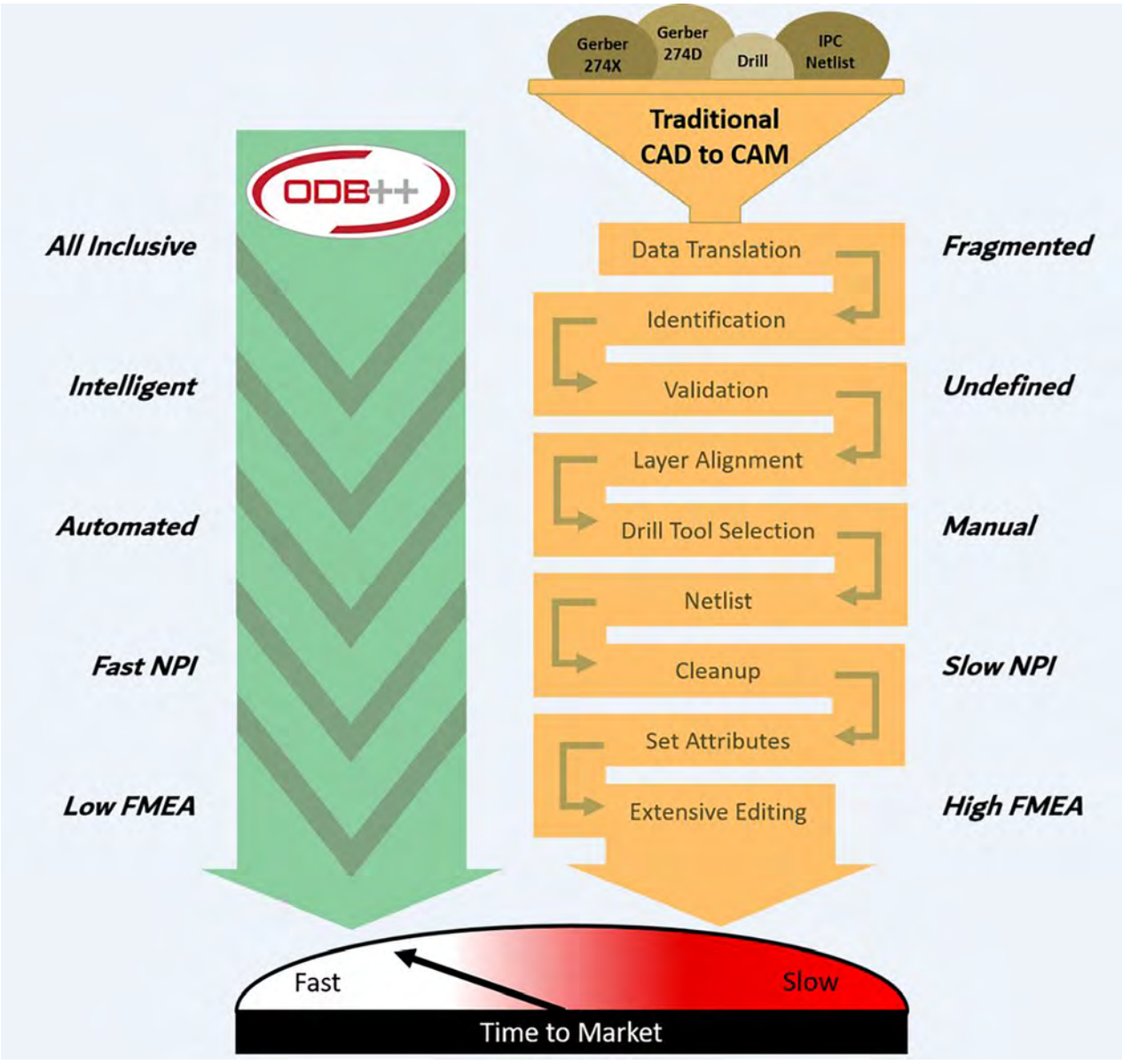

Figure 3: A comparison of ODB++ vs. the traditional design data transfer process.

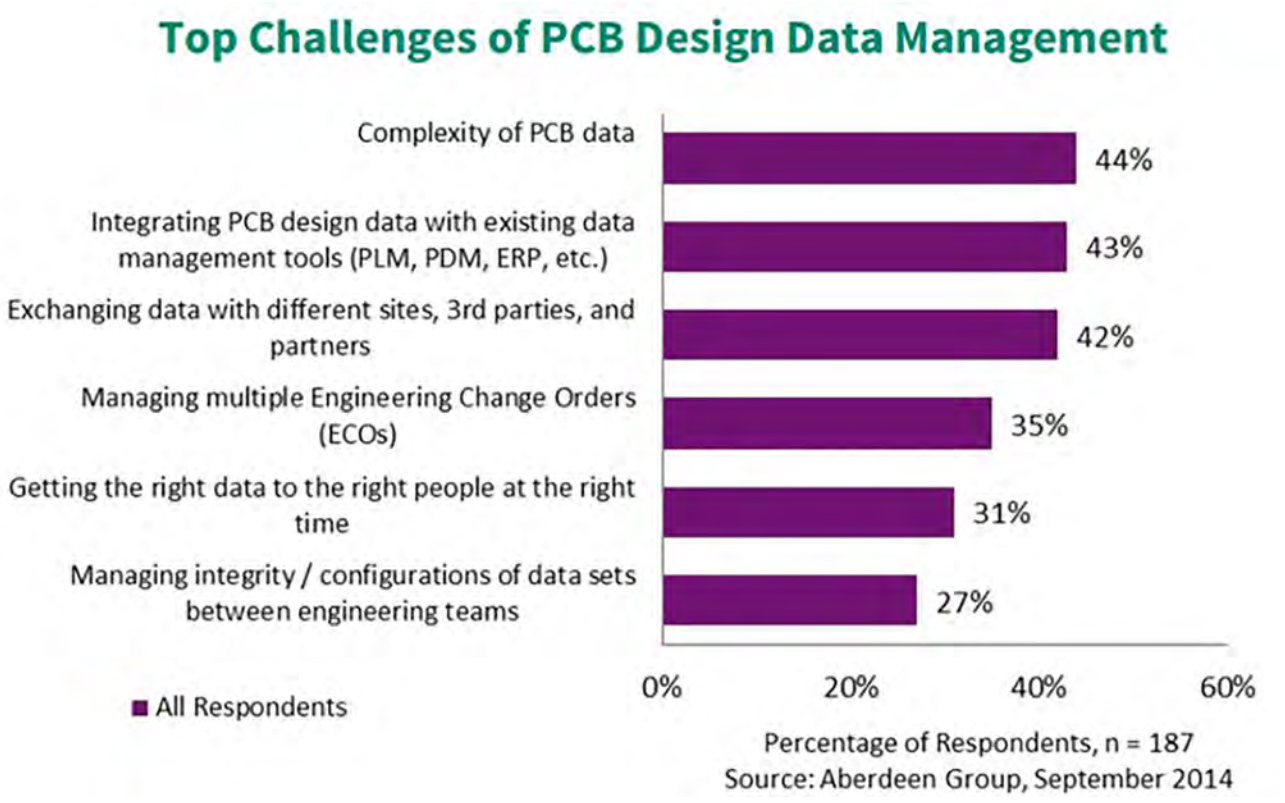

Figure 4: Proper design data management involves clearing a variety of hurdles.

The Basics Are Rooted in Complexity

When ODB was first introduced, the complexity of designs was primarily in the 4–6-layer range with lines/spaces just reaching eight mils, and only one drill pass was required to connect all the layers together. These were simpler times when compared to today's requirements. Yet in 2018, the production value for PCBs in the 4–6-layer range was about $15.5 billion. For layer counts of eight to 16, the PCB production value was about half ($7.6 billion). Over time, we have determined how to include more complexity in 4–6-layer designs. This required manufacturing processes to evolve; therefore, the product model for manufacturing those same designs also had to improve.

ODB is a defined foundation that represents a digital twin of the product to be manufactured. As the complexity of PCB designs increased, the data required to represent the digital twin multiplied at an alarming rate. Mainstream eight-layer designs became the norm, at least in part, but at the same time, lines/spaces moved to six mils and then to four mils at times while maintaining the same or less production area of the previous board designs. Another way to look at this is that the density of the copper routes on a design increased significantly, and the amount of data required increased at the same rate, if not more (Figure 5).

Drill processes also increased in complexity with the introduction of blind, buried, filled, and back-drilled through-holes, and the representation had to be added to the product model. PCB designs that were once all a rigid form became flexible. Then rigid-flexible was introduced with rigid and flexible areas existing in multiple stackup zones within a single board design. The number of manufacturing process combinations seems almost limitless.

As ODB++ began to obtain broader adoption, the supporters recognized the need for component-related content to be included within the product model. The initial purpose was to provide the ability to review components through the introduction of assembly analysis solutions. Later, assembly programming solutions

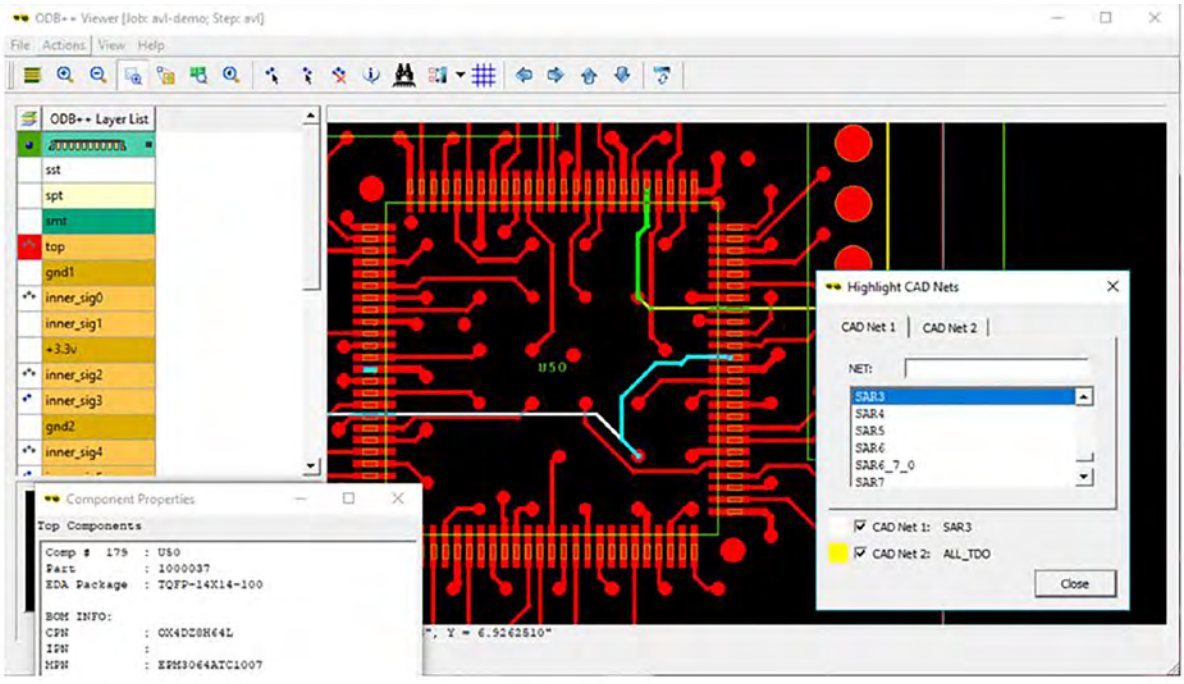

Figure 5: A look at a design in ODB++.

began using ODB++ as the foundation to drive assembly placement equipment, design solder stencils, and as a basis for the creation of assembly instruction. When the complexity of components was added, ODB became ODB++. With this change, the ODB++ product model could now house both fabrication and assembly content from a single self-contained source.

The ODB++ of today is rooted in fulfilling the complexity found in the data requirements for both the fabrication and assembly manufacturing processes. ODB++ is continuously being enhanced to keep up with further PCB data complexity that is a result of changing manufacturing process requirements.

Integrating and Using PCB Design Data

The ODB product model is the most successful commercially viable solution to address the needs of the PCB fabrication market since the advent of Gerber. There were attempts to provide other solutions leading up to the success of ODB++ that were available commercially and through industry sponsorship.

One example is a company that sponsored the use of the format GenCAM with the release of several IPC-25XX specifications [2]. The stated objective behind these IPC standards was, "The GenCAM format is intended to provide CAD-to-CAM, or CAM-to-CAM, data transfer rules and parameters related to manufacturing printed boards and printed board assemblies." An example of a commercially viable solution is Ucamco's introduction of an updated version of Gerber referred to as Gerber X2.

Today, the main design-to-manufacturing commercially available flows include the ODB++ export or import solution. All primary solution providers that serve the PCB design, DFM, fabrication, and assembly marketplace enable the use of the ODB++ product model directly in their application interfaces, and many of them have for over a decade (Figure 6).

The ODB++ model is a set of ASCII files stored within a series of directories each defined for a specific purpose. This approach has advantages and disadvantages when integrating with other solutions.

ODB++ spans multiple files within numerous directories that are later archived for release using a single file. Another approach could be to use a single file containing the product model, enabling the compression and transfer of a file when released to manufacturing. Because of the file size, in both cases, it would be necessary to decompress or unarchive the product

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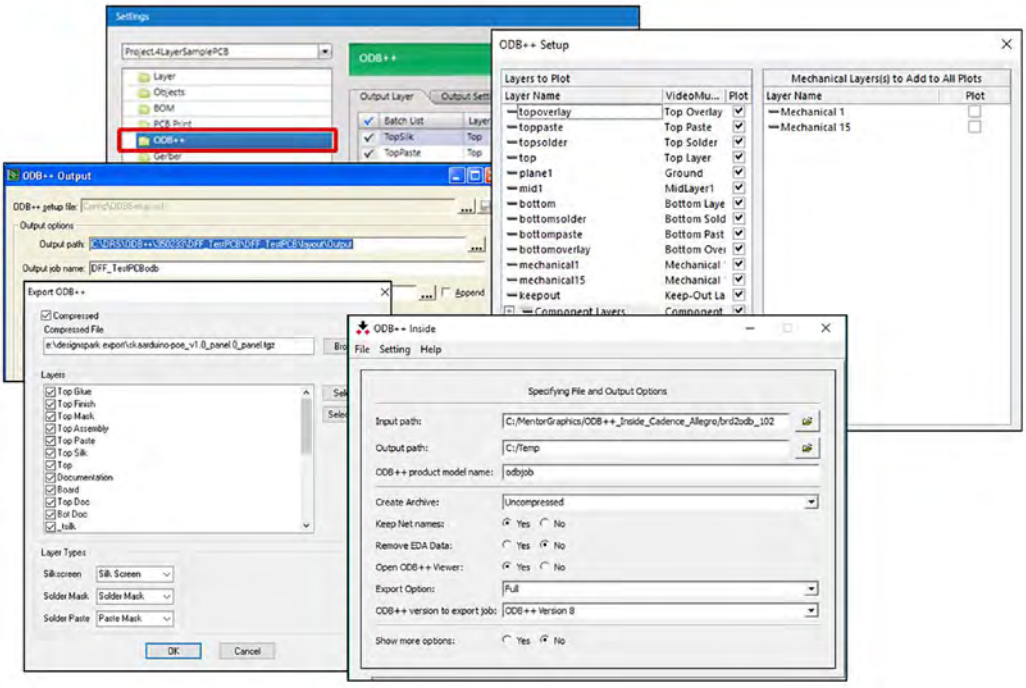

Figure 6: Examples of ODB++ outputs.

model for any of the content to be available for application use. The single-file approach is simpler and less prone to error. However, the consumption of the product model in either form is transparent to the user of manufacturing solutions, making either choice no more or less complex than the other.

As described earlier, the product models are getting larger in data size at an amazing rate. A single PCB product model reaching the size of over 200 megabytes can be a daily occurrence. When integrating a product model into other applications, the responsiveness of the results is typically a measure of success. When a product model is divided into files that contain content intended for specific purposes, the integration effort is only required to read a targeted portion of the complete product model. This improves application response time and encourages the further use of the product model. Other approaches may require an application to transverse a large portion until the data being requested has been located.

An example is knowing the location of a specific component reference designator on the top side of the product model and the location of the tooling holes from a specified drill layer within a product model. In the case of ODB++, the information would be located in two much smaller files specifically for this purpose: one file would contain the location of components and the other for the location of the drills. In other cases, the integration would need to read and possibly rationalize a larger portion of the product model than necessary to obtain this same information.

There are many cases where the ODB++ product model content has become part of a larger release-to-manufacturing process in cooperation with solution suppliers and along with existing adopters of ODB++. Bob Dylan once said, "There is nothing so stable as change." The evolution of design and the change in the manufacturing processes since the first release of ODB has been significant. Every change in ODB++ today is scrutinized under a set of criterion.

At the base is whether a change in the format will maintain backward compatibility. The ODB++ format can do that because the structure of the data is such that one change is isolated for a designated purpose. If the change does not result in the loss of backward compatibility, the change can go in an update or a minor release under the same version number. Changes that affect backward compatibil-

ity need to wait for a major release of ODB++.

Why is this important? Whether the integration is with commercial application suppliers or custom implementation completed by an ODB++ adopter, being able to rely on the use of the product model for a dependable timeframe is critical. When changes are required, the updated areas are easily identifiable and created in such a way to have minimal effect on the design-to-manufacturing flow. Development has ensured that releases of the ODB++ product model format do not negatively affect any partners within the supply chain.

ODB++ is a simple-to-understand set of files each with an intended purpose. It ensures quick access to the portion of the product model from an application provider or even with custom development. The format is stable with a history of rules that ensures stability around compatibility from release to release. The openness of the ODB++ product model lends itself to integration with other manufacturing management applications.

The Perils of Exchanging Data

The traditional exchange of multiple data files in multiple formats for the purpose of manufacturing was done to inform the suppliers by defining what needed to be manufactured, but it did not define how the manufacturing process would be accomplished. ODB++ contains the necessary manufacturing content to convey the fabrication, assembly, and test requirements to suppliers.

The effectiveness of communicating the product model is key in implementing process efficiencies, improving the level of product quality, and reducing the time to volume production, which defines the overall time-to-market. When the ODB++ product model is implemented to streamline the design-to-manufacturing process, many segments in both manufacturing operations can contribute to the successful launch of a new product.

The ODB++ model enables OEMs and suppliers to compete in global markets where continuously seeking ways to effectively communication manufacturing requirements is the key to success. For many years, virtually every industry software supplier starting from design throughout manufacturing includes ODB++ product model support currently available within the product flow. The ODB++ product model is already an industry evaluated, confirmed, and adopted solution that delivers today.

What's Next?

Adopting the ODB++ product model as the comprehensive data exchange method of choice allows both OEMs and suppliers to more effectively:

- Meet product requirements while reducing costs
- Minimize production delays
- Optimize manufacturing productivity through improved knowledge exchange

When considering the adoption of a product model, think back to the transformation of the earthbound caterpillar into a beautiful butterfly as the primary objective. The caterpillar has built right inside its model the information that is required to make such a transformation. The ODB++ product model is a solid representation of the PCB design while embracing the need for defining manufacturing process requirements designed to deliver a PCB interruption-free, on time, and with the overall lowest cost. For more information, visit the ODB++ Solutions website. Registration and access to the format are free to all, users, and solution partners alike. **DESIGN007**

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2. IPC, "IPC-2516A: Sectional Requirements for Implementation of Assembled Board Product Manufacturing Data Description (BDASM)," November 2000.

Max Clark is a business unit manager in Mentor's Valor division with responsibilities in DFM and intelligent manufacturing data exchange.

IPC-2581 Continues to Flourish

Feature by Linda Mazzitelli
PTC

New processes and standards seem to be popping out of the woodwork these days. With Industry 4.0 and other initiatives coming to the forefront, now—more than ever—there is a need to start earnestly looking at what is out there and if (or how) it can be implemented to meet your technical and business goals.

For example, take board manufacturing data. For years, Gerber data has dominated as the de-facto way to provide information to bare board shops along with drill files and manual READ-ME files that need to be included to ensure that everything is clearly understood. ODB++, while also around for a while, was considered the new way to communicate; however, adoption was slow and never really caught on as a preferred way of sharing data.

Issues With Current Methodologies

Today, it takes multiple disparate files to represent bare board and assembly information. Not only does it take time to create and verify them before they go out the door, but once the downstream vendor receives the files, the data must be reformatted to enable the various machines to read the data the way they were programmed to interpret it—as they all "speak" different languages. This can require hours of manual effort. Then, each time design changes occur, the same process needs to be repeated. Add to this having to communicate with overseas suppliers, and the issues multiply.

In addition, electronic computer-aided design (ECAD) is only one piece of a much larger, project-centric definition that needs to be captured and ultimately, optimized. It does not contain all of the part information, software, and mechanical data that ultimately defines a full, working product.

There Has to Be A Better Way

Because standards adoption in this industry tends to be akin to turning around a battleship, what is often seen as new has generally already been in production for 10 years or more. Often, there are outside influences and dependencies that cause this, so most of us tend to take a "wait-and-see" approach—let others shake out the issues. And even then,

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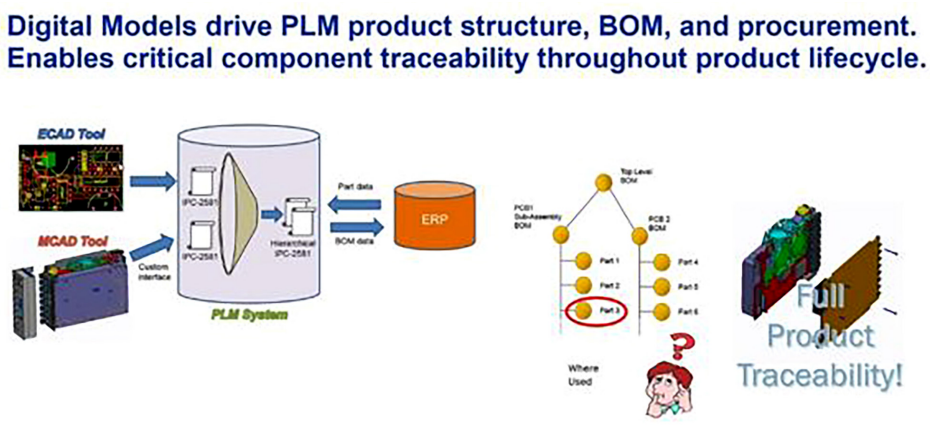


Figure 1: Digital data transfer offers benefits for every stakeholder in the manufacturing process.

we only look at adoption if the mandate comes from higher-ups in the organization. It works the way we do it now, so why change?

While this is understandable, it is not ideal. Better practices and methodologies continue to be introduced and are evolving along with the industry (Figure 1). One of these is IPC-2581, now known as Digital Product Model Exchange (DPMX). If you haven't heard of it before, you're not exactly alone. The standard itself was developed in the early 2000s but was not able to gain any ground at that time.

Fast forward to 2011, which is when several companies regrouped with the goal of reinvigorating the consortium. As a result of their efforts, it now is rapidly gaining attention and support from ECAD vendors and contract manufacturers (CMs) alike. Jim Pierce, a manufacturing engineer at Axiom Electronics, is seeing the wave, "Industry demands require innovation and automation to stay competitive. To meet those goals, we are striving towards paperless and more automated processes." Pierce adds, "Working with a single IPC-2581 file allows us to not only achieve our objectives but also ensures that the customers' needs are also met."

IPC-2581/DPMX and Industry 4.0

An IPC-2581/DPMX proof of concept was executed under DMDII 15-05-06 (System Design Using the Digital Thread). DMDII (now MxD) was an institute created under the National Network for Manufacturing Innovation (NNMI). This started as an effort through a fund that was set aside to encourage individual institutes to invigorate and promote new manufacturing initiatives in the United States. Each participating organization was tasked with raising money that would then be matched, dollar for dollar, up to $70 million in support of their efforts. Part of the criteria was that each institute must have an educational organization on board with the overall goal being to close the gap between research and implementation.

From a board design perspective, the idea was to develop a format that would contain all of the information required to manufacture and assemble a complete design without the need for any manual intervention (i.e., paperless and completely machine-driven). This resulted in a $2-million project call that was answered by both a large telecommunications company and an equally large aerospace and defense company, which led to a detailed report focusing on PCB design digital factories.

Jamie Wise, vice president of WISE Software Solutions, has been a strong proponent from the beginning, "As one of the founding members of the IPC-2581 Consortium, we are pleased to witness the rapid adoption of the IPC-2581 specification as the format of choice for design, fabrication, and assembly." Wise continues, "IPC-2581 is the EDA transfer solution the industry has been waiting for. All of the essential EDA data is supported, including stackups, bills of materials (BOMs), fabrication notes, drawings, etc. It's great for going digital/paperless."

The Benefits of IPC-2581

As mentioned earlier, the current formats require many individual files (i.e., artwork, solder mask, solder paste, drill, pick-and-place,

	Graphical Features	Feature Intelligence	Stackup	Mechanical Specification	Notes	Fabrication Acceptability Specification
RS-274X	√	Manually Added	ePaper Drawing	ePaper Drawing	ePaper Drawing	ePaper Documents
ODB++	√	√	ePaper Drawing	ePaper Drawing	ePaper Drawing	ePaper Documents
IPC-2581	√	√	√	√	√	ePaper Documents

Figure 2: A comparison of the three design data transfer standards.

BOM, netlist, and the list goes on). Each file requires a separate output that then also requires its own set of instructions. This takes time to set up and send from the design and engineering end. It also requires setup by the CMs to ensure all of their machines are aligned and can work in concert with each other through the entire board manufacturing and assembly process. Since much of this involves manual effort, it is more prone to errors on both sides. Further, a lot of time is required to pull together the different specifications based on which manufacturer the data is going to or modify the data if you need to change fabrication houses (Figure 2).

The main goal of IPC-2581 is to eliminate all of that risk and at the push of a button from your CAD tools, generate a single file that you can send to your downstream suppliers, enabling them to do their work more efficiently without the need for any manual intervention. All of the files and instructions are electronically embedded and machine-readable within the IPC-2581 file itself. "IPC-2581 moves multiple e-paper file intelligence (i.e., PDF, DXF, etc.) into a single, specific CAD feature with associated requirements," says Dana Korf, senior consultant with Korf Consultancy, formerly with Multek and Huawei. "For example, connector pads may show that they require thicker electrolytic gold and a specific finished hole tolerance. Both can now be embedded, eliminating the need for a fabrication drawing, additional CAD layers and drawing notes, which can be conflicting or misread." Korf concludes, "Reduced data transfer time and improved quality are the results."

Mapping the Way

In the pioneering days, it was an arduous task to try to explore and map new frontiers and territories. However, getting the process started for adopting IPC-2581 is easier than you may think. Most major ECAD vendors already have an "easy button" that will enable you to export your designs to IPC-2581, thereby providing that first step in your path to adoption. The resulting file contains all of the ECAD-related information for both your bare board and assembly supply chain partners. In addition, to help maintain IP security, the file can be controlled so that your bare board and assembly houses only see the data that they need to do their individual jobs, as the source data is fully protected, reducing the chances of reverse-engineering (Figure 3).

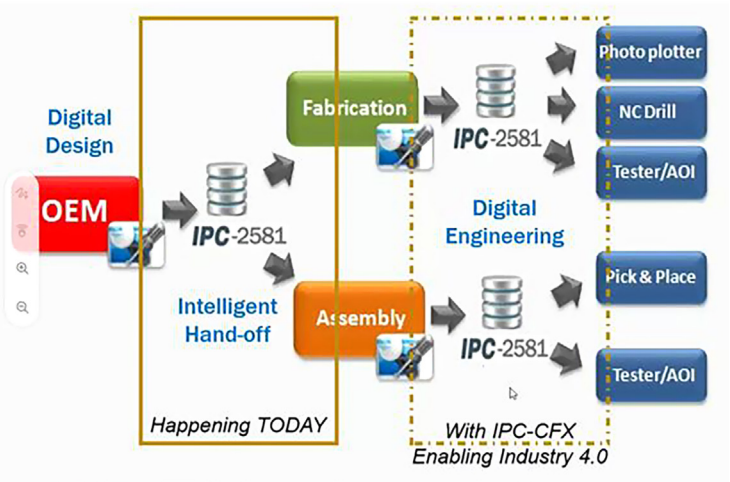


Figure 3: Flowchart showing IPC-2581 connected to IPC's Connected Factory Exchange (CFX) manufacturing format.

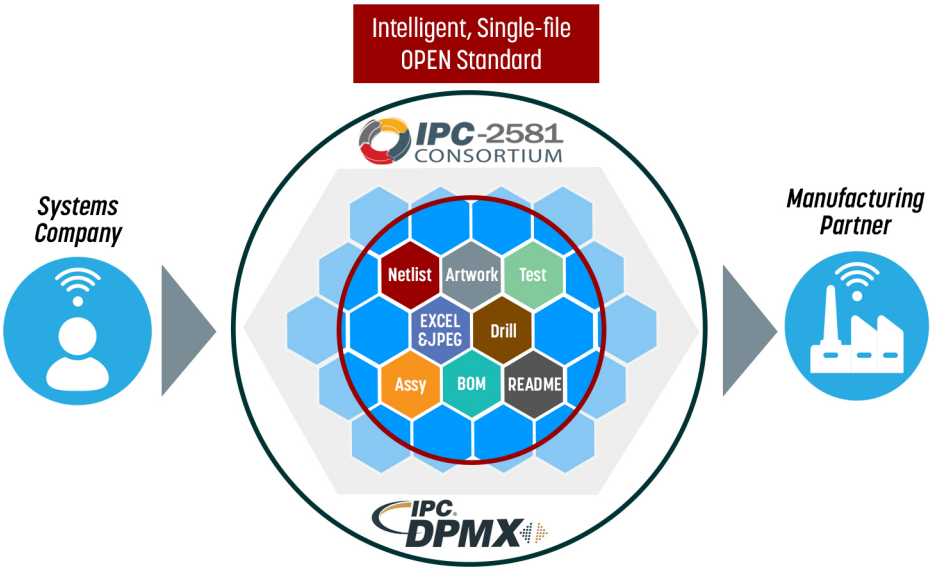


Figure 4: IPC DPMX will connect IPC-2581 with IPC's CFX standard.

Once you have tried and are comfortable with the first step, the next level would be to also include enterprise information, such as MCAD assemblies, CAM, ERP, MRP, PLM, and MCAD/software BOMs. By incorporating procurement (buy), fabrication (manufacture), and assembly (build) data together, you can now also tie in the extended project design team and enable them to collaborate and contribute to the final output package.

Lastly, including programmable data per individual part, mechanical data, drawing files, and enterprise part data—such as manufacturer specification sheets, classifications, approval manufacturer lists (AMLs) and approved vendor lists (AVLs) along with other product-specific requirements—enables you to have a single file that contains your full product definition from design to manufacturing (Figure 4).

Leading the Charge

If you want to give this a try, there is a lot of existing support you can take advantage of. Currently, many large companies are paving the way to help promote adoption and willing to share both their experiences and programs they have written to streamline the process. Because of the efficiencies gained on the manufacturing side using IPC-2581, some CMs have begun charging more when they receive only Gerber data (Figure 5).

Many free viewers are also available on the market today that enable you to look at the file content before shipping out. For an added fee, some packages include built-in DFM packages that enable you to compare your Gerber and IPC-2581 data. After sending the files, let your suppliers review each and provide feedback regarding what is different and why. Armed with that information, you can begin to move forward and help to pioneer this evolving standard.

Once you develop a comfort level with the first step, start involving others to discuss how to represent a full product specification, including what digital thread and Industry 4.0 mean to your company. From there, you can begin to plan how to characterize a more robust representation of your full product architecture in a secure and collaborative format.

Manufacturer Support Status				
Company Name	Software Used	IPC-2581 A	IPC-2581 B	Stack-up Exchang
Any manufacturing company	**Genesis, CAM250 AEGIS, WISE, Siemens**	✓	✓	
AT&S	Genesis 2000®, Insight®, InPlan®	✓	✓	
Accurate Circuit Engineering	Genesis 2000®, Insight®, InPlan®	✓		
Axiom Electronics	VisualCAM	✓	✓	✓
	CircuitCAM	✓	✓	
CC Electronics	VisualCAM	✓	✓	✓
Electrostein	CAM350	✓	✓	
Multek	Genesis 2000®, Insight®, InPlan®, InCAM®	✓	✓	
Sanmina	Genesis 2000®, Insight®, InCAM®	✓	✓	
Sierra Circuits	Genesis 2000®	✓	✓	
Tempo Automation	("internal")		✓	
TTM Technologies	Genesis 2000®, Insight®, InCAM®, In-Plan®	✓	✓	Q1, 2019

Figure 5: IPC-2581 is already in use by a variety of companies.

This Is Something You Can Do Today

If you want to give this a try, start simply. Try exporting an IPC-2581 file in parallel with your current artwork and assembly files. For example, download one of the free viewers and look at the files after they are generated, or send both to your fabrication and assembly supply chain vendors for feedback. You can also evaluate the information provided back to you and look at how to best optimize the fabrication and assembly process going forward.

Next, get involved and join a group, such as IPC. Becoming a member is free for you and/or your organization. You can also visit www.ipc2581.com for expert advice; you are not alone! And once you have had a chance to see the benefits, communicate the value to others. Pull together an internal team—including IT, manufacturing, procurement, component engineering, etc.—to develop a plan for Industry 4.0. Do a proof of concept. Then, document your process and share with others both internally and those getting started on their own journey to adoption. **DESIGN007**

A special thanks to Gary Carter, ECAD project manager at XPLM, for all of his help and insight regarding the value that IPC-2581 brings to both customers and manufacturers.

Linda Mazzitelli is the product management director at PTC responsible for ECAD design data management, visualization, and ECAD partner management.

Researchers Demonstrate 3D Quantum Hall Effect for the First Time

The quantum Hall effect (QHE), which was previously known for two-dimensional (2D) systems, was predicted to be possible for three-dimensional (3D) systems by Bertrand Halperin in 1987. However, the theory was not proven until recently by researchers from the Singapore University of Technology and Design (SUTD) and their research collaborators from around the globe.

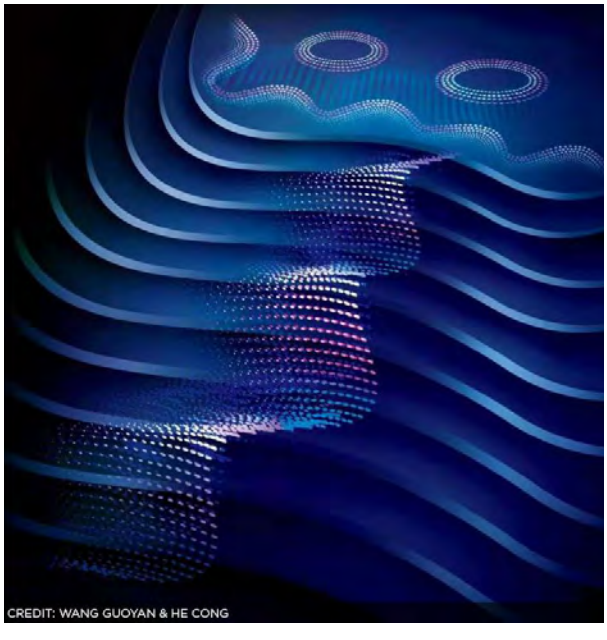
SUTD's experimental collaborator, the Southern University of Science and Technology (SUSTech) in China, has been working on a unique material known as ZrTe5 since 2014. This material can satisfy the required conditions and exhibit the signatures of 3D QHE.

In the research published in *Nature,* the researchers show that when the material is cooled to a very low temperature while under a moderate magnetic field, its longitudinal resistivity drops to zero, indicating that the material transforms from a metal to an insulator. This is due to the electronic interactions where the electrons redistribute themselves and form a periodic density wave along the magnetic field direction called the charge density wave.

"This change would usually freeze the electron motion, and the material becomes insulating, disallowing the electron to flow through the interior of the material. However, using this unique material, the electrons can move through the surfaces, giving a Hall resistivity quantized by the wavelength of the charge density wave," explained co-author Professor Zhang Liyuan from SUSTech.

"We can expect that the discovery of 3D QHE will lead to new breakthroughs in our knowledge of physics and provide a cornucopia of new physical effects. This new knowledge will also provide us new opportunities for practical technological development," said co-author Assistant Professor Yang Shengyuan from SUTD.

(Source: SUTD)



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Realizing a Higher Standard for PCB Design

Tim's Takeaways

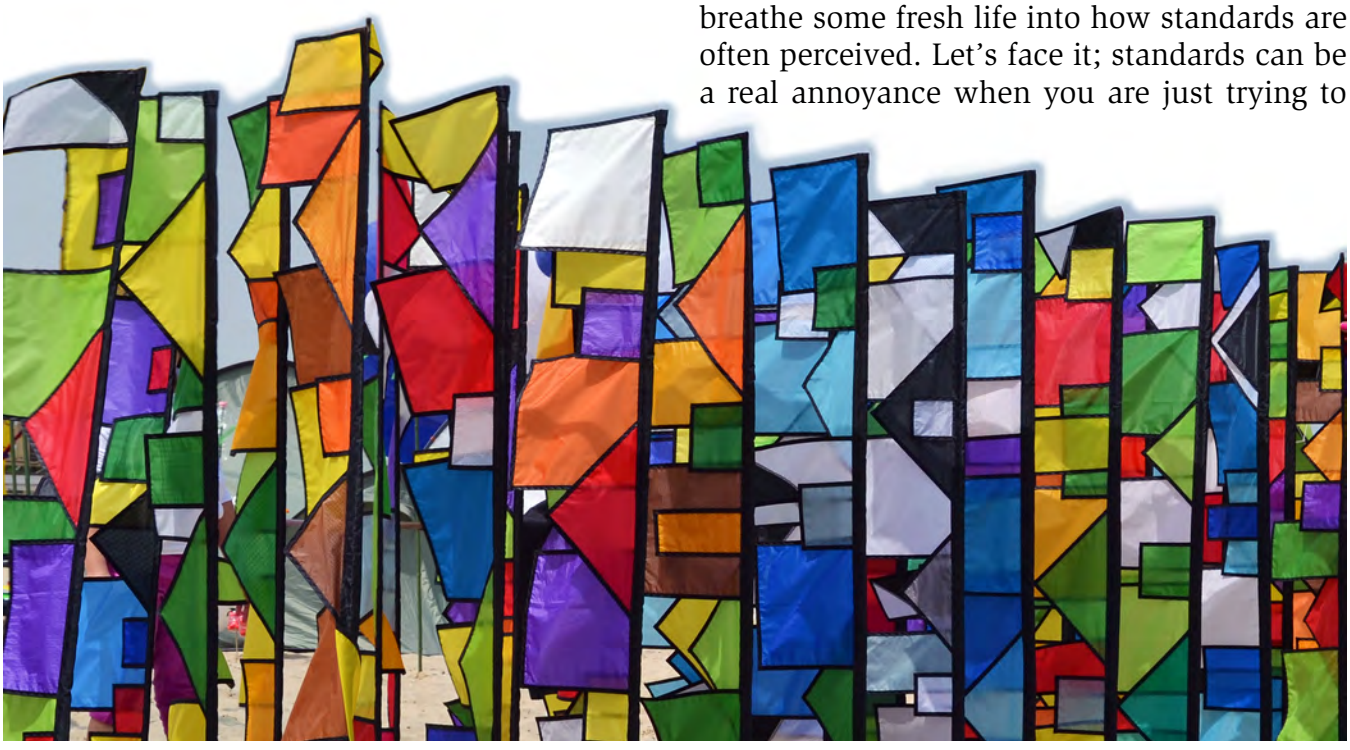
Feature Column by Tim Haag, CONSULTANT

There are a lot of standards in our lives. In the late fall, many of us switch from daylight savings time to *standard time*. Someone's favorite team or athlete often sets the *standard* for a higher level of performance, and I personally think that Sean Connery set the *standard* for James Bond. On Saturday mornings, my wife and I even have our standard breakfast that we cook. And of course, there are three-bazillion *standards* that are in place regulating what we eat, wear, drive, and live in as well as how we design PCBs.

But did you know that there was another definition of "standard?" In years past, colorful flags or banners of identification called "standards" were carried by military organizations into battle to serve as a rallying point for the troops and to mark the location of the group commander. It is believed that this practice originated back in ancient Egypt, and later on the Roman empire made battle standards part of their vast armies. Eventually, the battle standard was formalized during the Middle Ages by the armies of Europe with the standards displaying the commander's coat of arms.

Carrying a standard may seem silly in today's era of technological warfare where any such display that identified your commander's location would surely guarantee a quick missile strike in return. But back in the days of Napoleonic battle tactics involving swords, bayonets, muskets, and cannons, it was important to know where to look up at for your leadership in all the dust, smoke, and confusion of the battle.

With this thought in mind, perhaps we can breathe some fresh life into how standards are often perceived. Let's face it; standards can be a real annoyance when you are just trying to



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get the job done: What size should this via be? *Check the standard.* What do you mean I used the wrong trace width? *Check the standard.* How should I document this process? *Check the standard.* Like the colors that were carried into battle, today's standards can still offer us the ability to identify authority, lead us in the right direction, and even offer protection. If we can just get over our annoyance, perhaps this fresh perspective will illuminate standards in a new light.

If we can just get over our annoyance, perhaps this fresh perspective will illuminate standards in a new light.

Identification of Authority

To the untrained eye, one circuit board may look pretty much like any other, but as we know, there are major differences between them. Not only are they different in purpose and design but also in how they are manufactured for specific industries. If you are designing medical equipment, for instance, you will have to meet many different regulatory requirements from organizations, such as the Food and Drug Administration (FDA), World Health Organization (WHO), and International Electrotechnical Commission (IEC), among others. If called upon by any of these regulatory organizations to provide specific information on how your equipment was manufactured, you need to be ready to provide the required documentation. This documentation can include the quality control processes that were used during assembly as well as component and material traceability records.

The reasons for this are pretty obvious; you don't want low-level workmanship used in the pacemaker that is going to be implanted in someone's chest to regulate their heartbeat. And if there is ever a question on parts or materials used in a piece of equipment, you need to be able to trace it back to its source as quickly as possible. As a medical equipment manufacturer, you will want to have your circuit boards built by an assembler that is registered with standards such as ISO 13485. Standards like these are what identify a PCBA manufacturer as being authorized to build circuit boards to the high level of quality you need for the medical equipment you are creating.

Direction

All of us who have laid out PCBs for a living probably share many of the same career experiences, such as not having a clue what PCB layout was really all about when we first started. If you're like me, you probably started out throwing parts on the board and connecting them up until one of the older hands in the department would critique my work and point out my mistakes:

- "This small part is getting shadowed by this large part, and it won't wave solder correctly."
- "You have too much metal going into this pad compared to the other pad, and your resistor is going to tombstone during reflow."
- "Your part placement is too tight, and the rework technicians are going to end up hating you. We don't want to clean up the mess in here after they beat you to a pulp!" (okay, I might have embellished that last one a bit).

The point is that a lot goes into designing a PCB so that it can be successfully and efficiently manufactured. I learned much of it slowly through tribal knowledge, and fortunately, I had some really good teachers. But many designers don't have the advantage that I had of working with experienced designers for training, and they end up making a boat-load of costly mistakes. Some of these can be corrected while others require a redesign, and sadly, some will result in the design being scrapped. If only there was some clear direction on how

to design the board correctly in the first place. Well, there is.

Standards, such as IPC-A-610, lay out many of the PCB acceptability requirements that you need to know to design a board that can be manufactured correctly. One portion of this standard covers everything you've ever wanted to know in order to design your board for good solder joints. IPC-A-610 is a vast document, but like a detailed map, it will give you the direction you need.

Protection

Of all the benefits that a colorful standard offered on the battlefield, the one that seems the most attractive to me is in its protection. A soldier who was separated from their battalion could look up and find where they needed to go to come under the protection of the group. Interestingly enough, today's standards offer that same sort of protection. If you want electronics that you know are certified for use, you may look for a UL standard. And if you want to know if a board can be sold or distributed in the European Union, you would look to see if it was RoHS-compliant. Certification to different standards will tell you if the circuit board that you are using can be used in the manner that you want it to be used. For the PCB designer, however, there's more to the protective nature of standards than just that.

When you lay out a PCB, you are responsible for how that board will eventually be manufactured. As I pointed out earlier, a standard can give you excellent direction when you don't know how something should be designed. At the same time, though, a standard can also give you a threshold that shouldn't be crossed. If you are being asked to design something and you aren't sure if you should push the level of tolerances that far, don't be afraid to say that what you are being asked to do will violate the standard. And if you are pushed over that threshold, then document that you were required to violate the standard so that there will be no question in the future about why you did what you did.

Conclusion

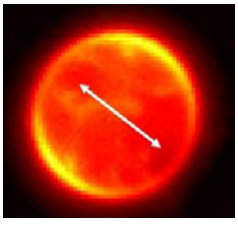
I hope that this insight will be helpful to you the next time you are tempted to grumble or groan about having to adhere to a particular standard. Today's design standards provide a necessary level of identification to our work, give us direction on how best to accomplish our work, and protect us and our work as long as we take the time to follow them. I would even say that working with standards should become part of our regular standard operating procedure (SOP).

And now I believe that there is a new standard that I need to explore—one that involves some dessert and a quiet evening. Until next time then, keep on designing. **DESIGN007**

Tim Haag is a PCB design consultant based in Portland, Oregon. To read past columns or contact Haag, click here.

Graphene Layer Enables Advance in Super-Resolution Microscopy

Researchers at the University of Göttingen have developed a new method that takes advantage of the unusual properties of graphene to electromagnetically interact with fluorescing (light-emitting) molecules.



Led by Professor Enderlein, researchers used a single sheet of graphene, just one atom thick (0.34 nm), to modulate the emission of light-emitting (fluorescent) molecules when they came close to the graphene sheet. The excellent optical transparency of graphene and its capability to modulate through space the molecules' emission made it an extremely sensitive tool for measuring the distance of single molecules from the graphene sheet. The accuracy of this method is so good that even the slightest distance changes of around 1 ångström.

(Source: University of Göttingen)

PCB007 Highlights

Trouble in Your Tank: Moving Into Microvias, Part 4 ▶

Copper deposit in the vias with electroless copper or alternatives, such as carbon-based direct plate processes to the vias, depends on process control, equipment design, and chemical parameters. When these are not in control, defects arise. In this installment of the column series, Mike Carano discusses metallization for HDI blind via processing.

Nano Dimention Details New DragonFly LDM ▶

Dan Feinberg talks with Nano Dimension CEO Amit Dror about the new DragonFly LDM 3D printer technology announced by the Israeli company on July 24, 2019, aimed at increasing machine uptime and moving forward from prototyping to higher production volumes.

Pollution Prevention Techniques: Rinse Water Reduction ▶

The first step in any pollution prevention strategy is to minimize chemical wastes and their rinse waters. There are five general categories of common techniques for pollution prevention in a PCB fabrication facility: (1) new processes to replace sources of pollution; (2) extend the bath's life; (3) rinse water reduction; (4) dragout reduction; and (5) ventilation reduction.

The PCB Norsemen: Avoid Failures in PCB Production With Compliance Control ▶

Failures and reliability in the printed circuit industry are usually considered in the context of quality claims and non-conformity. This is a logical approach; however, there is a new context where these aspects are under close scrutiny, namely compliance—especially in the defense industry.

Testing Todd: What Do You Mean 'Passed' Isn't Enough? ▶

From a reliability standpoint, we need to quickly assess what risk we may have uncovered when faults are detected during electrical test (ET). "Passed" is not always passed. We must be diligent to scrutinize the failures found during routine ET as a high yield may not indicate high reliability.

Better to Light a Candle: Chapter Four—Next Steps for Developing the Future Workforce ▶

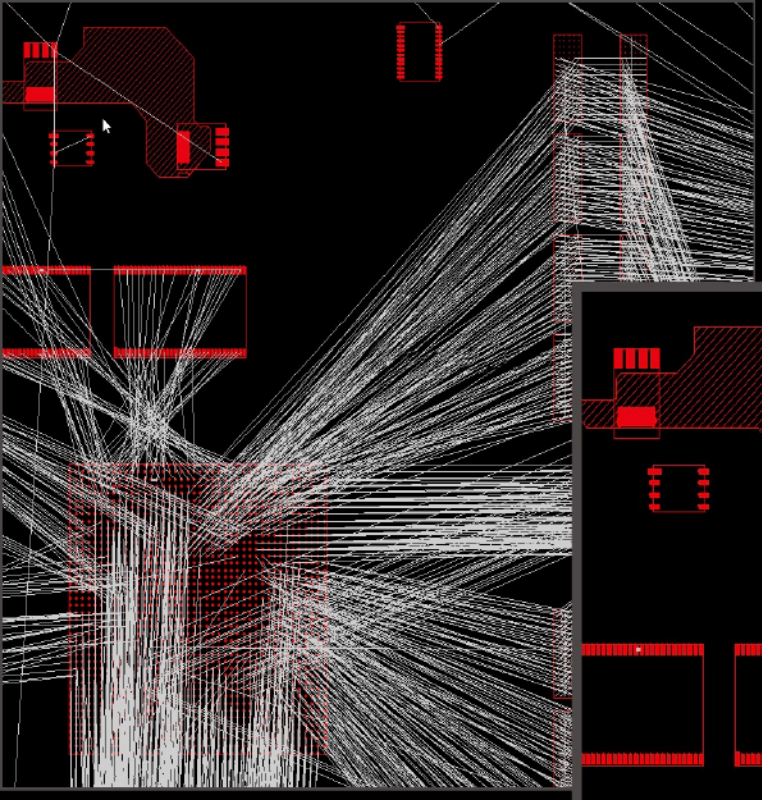
This fourth installment of Marc Carter's column series provides an update on repeat (and perhaps even expanded) classes at Michigan Tech and reports on developing contacts at other prospective university, industry, and government nodes for similar efforts to ensure basic printed circuit technology familiarity of college graduates over the next few years.

TTM Technologies Unveils Executive Transition ▶

TTM Technologies Inc. has announced that Catherine Gridley will be joining the TTM executive team on September 3 as incoming senior vice president and president of the aerospace and defense/specialty (A&D) business unit (BU) and will formally assume the A&D leadership role on January 1, 2020.

How to Feed Test Data Back to Engineering for Process Improvement ▶

Some people think of the PCB manufacturing process as a black box: design data goes to the manufacturer (fabrication house), and magically, the finished PCB is produced. While it may have been like that in the past, in actuality, fabricating PCBs today is quite a ballet of processes.



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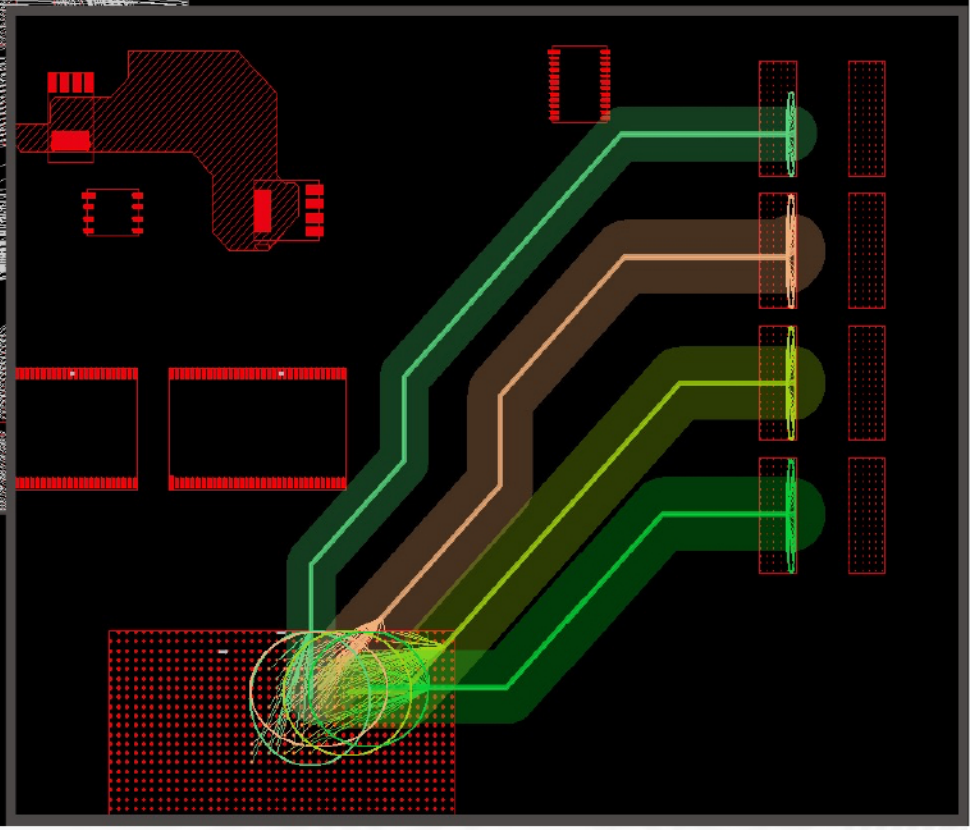

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My 100th Column

Beyond Design

by Barry Olney, IN-CIRCUIT DESIGN PTY LTD / AUSTRALIA

Believe it or not, this is my 100th "Beyond Design" column. The editors at I-Connect007 are a great group to work with. I eagerly await each month's magazine release to see how creative the team have been with editing, laying out, and producing my column.

I-Connect007 was founded in 1999 and is now the industry's longest-running electronics media portal. Personal development and continued education are so important—especially in a relatively new and ever-changing industry where designers are continually pushing the envelope. And with its line-up of three online magazines—Design007 (featuring Flex007), PCB007, and SMT007—I-Connect007 provides the latest information from industry experts.

My first "Beyond Design" column on ground pours was published online in 2011 [1]. Over the years, I think that I only missed publishing one month when I was on vacation. I'll have to work on that lazy streak! When I was first approached to write a regular column, I thought that I might be able to convert my course on advanced design for SMT, which I had been presenting throughout Australia and New Zealand since 1994, into a number of segments. However, I never envisaged reaching the 100 mark.

"Beyond Design" focuses on high-speed PCB design, signal and power integrity, and EMC design techniques. To wrap-up my 100th column, I look back over the past 99 columns and reflect on what I believe to be the Top 10 most enlightening for high-speed PCB designers, counting down in reverse order of preference.

10. The Dumping Ground

Ground planes in a multilayer PCB allow the designer to ground anything, anywhere, without having to run multiple tracks, the net

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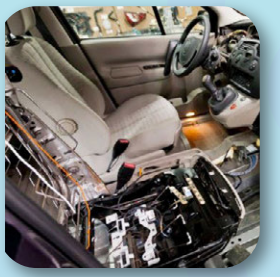
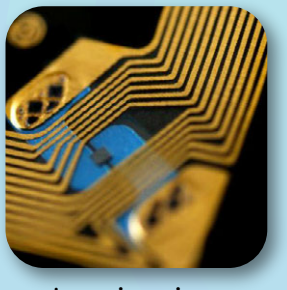


Automotive Electronics



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needing grounding being routed directly to the ground plane on another layer. However, this is a simplistic approach. One should also consider the presence and interaction of the power distribution network (PDN) and how and where the return current flows. A logic schematic diagram masks details crucial to the operation of unintentional signal pathways vital to your understanding of signal performance, crosstalk, and electromagnetic emissions.

When you plan your stackup, be aware of which plane(s)—either power or ground)—will be the return path for your critical signals, and ensure there is an unobstructed return path. The best way to think of this is to imagine routing a return trace adjacent to each signal trace on the reference plane. Where will the current flow, and is it unobstructed? The reference plane adjacent to each signal layer allows the return current to flow as closely as possible to the signal trace reducing inductance and loop area.

9. PDN and Capacitor Selection, Parts 1 and 2

This two-part column focused on capacitor selection and three alternative approaches to analyzing the PDN:

1. Target frequency
2. One-value capacitor per decade
3. Optimized value capacitor

The target frequency approach has been traditionally used. This method targets a precise frequency and is used to reduce AC impedance as well as EMI within a specific band. The alternatives of using either a one-value capacitor per decade or many optimized capacitors are used in an attempt to level out the AC impedance at the desired impedance over a broad frequency band (Figure 1).

8. Signal Integrity, Parts 1-3

As system performance increases, the PCB designer's challenges become more complex. The impact of lower core voltages, high frequencies, and faster edge rates has forced us into the high-speed digital domain. But in reality, these issues can be overcome by experience and good design techniques. If you don't currently have the experience, then listen up. This three-part series on signal integrity covered the following topics:

- How advanced IC fabrication techniques have created havoc with signal quality and radiated emissions
- The effects of crosstalk, timing, and skew on signal integrity
- Where most designer's go wrong with signal integrity, and how to avoid the common pitfalls

7. Plane Crazy, Parts 1 and 2

A high-speed digital PDN must provide a

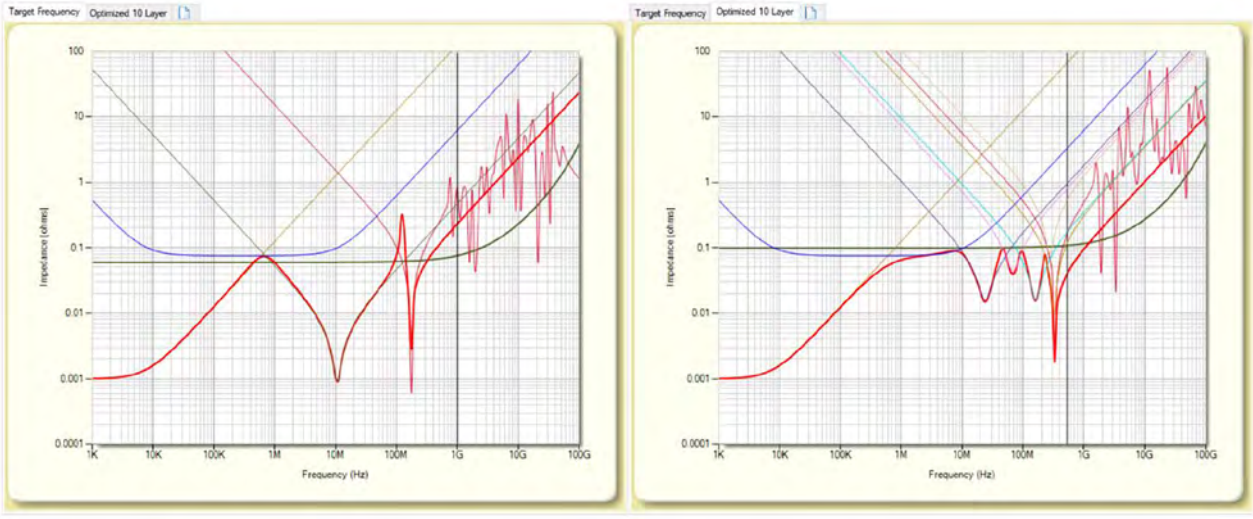

Figure 1: Target frequency vs. optimized value approaches (iCD PDN Planner).

low-inductance, low-impedance path between all ICs on the PCB that need to communicate. To reduce the inductance, you must also minimize the loop area enclosed by the current flow. The most practical way to achieve this is to use power and ground planes in a multilayer stackup. In this two-part column, I looked at the alternatives to planes, why planes are used for high-speed design and the best combination for your application.

6. DDR3/4 Fly-by Topology: Termination and Routing

DDR3/4 fly-by topology is similar to daisy-chain or multi-drop topology but has very short stubs to each memory device in the chain to reduce the reflections. The advantage of fly-by topology is that it supports higher-frequency operation and improves signal integrity and timing on heavily loaded signals. If you are employing high-frequency DDR4, then the bandwidth of the channel needs to be as high as possible. However, with today's extremely fast edge rates, the sequencing of the stubs and the end termination and the associate load can make a measurable difference in signal quality. In this column, I explored how best to route DDR3/4 fly-by topology (Figure 2).

For more background reading, check out my two-part series on "PCB Design Techniques for DDR, DDR2, and DDR3" [2].

5. Microstrip Coplanar Waveguides

The classic coplanar waveguide (CPW) is formed by a microstrip conductor strip separated from a pair of ground plane pours, all on the same layer affixed to a dielectric medium. In the ideal case, the thickness of the dielectric is infinite. But in practice, it is thick enough so that electromagnetic fields die out before they get out of the substrate. A variant of the coplanar waveguide is formed when a ground reference plane is provided on the opposite side of the dielectric. This is referred to as a conductor-backed or grounded CPW. CPWs have been used for many years in RF and microwave design as they reduce radiation loss at extremely high frequencies compared to traditional microstrip. As edge rates continue to rise, they are coming back in vogue. In this column, I described how conformal field theory could be used to model the electromagnetic effects of microstrip coplanar waveguides.

4. The Dark Side: Return of the Signal

All PCB designers should be aware of the impact of crosstalk on signal integrity. As signal traces come into close proximity of an aggressor signal, part of that signal is unintentionally electromagnetically coupled into the victim trace as noise. I have mentioned before that current flow is a roundtrip; the current must return back to the source to complete the loop.

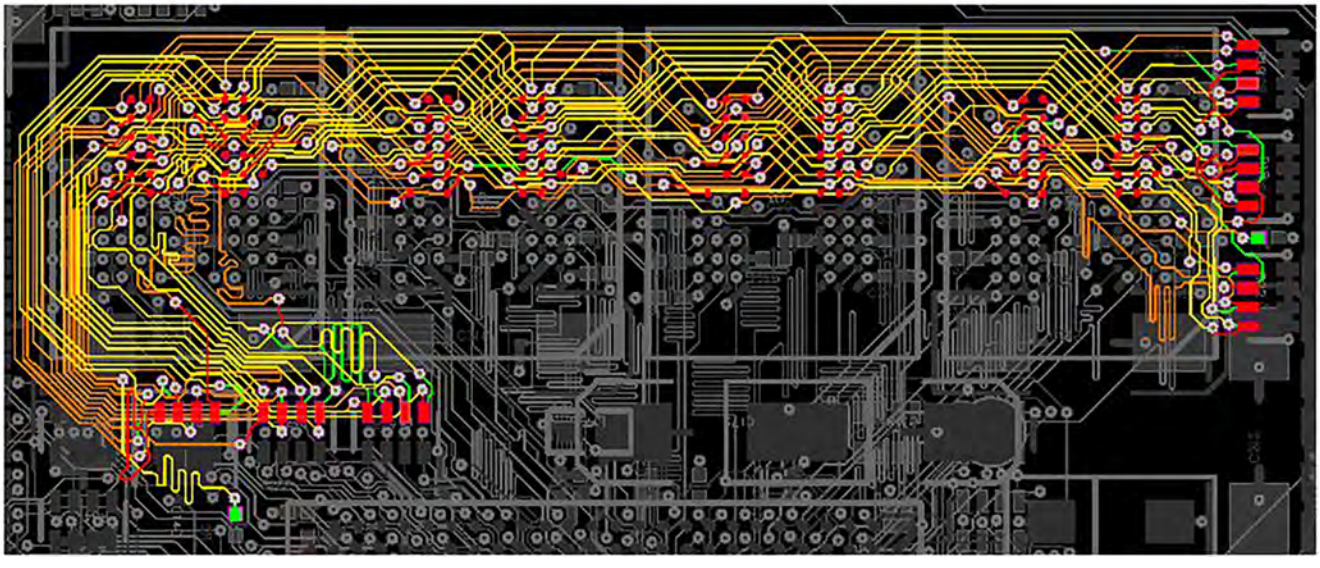

Figure 2: Fly-by topology for clock, address, command, and control routing.

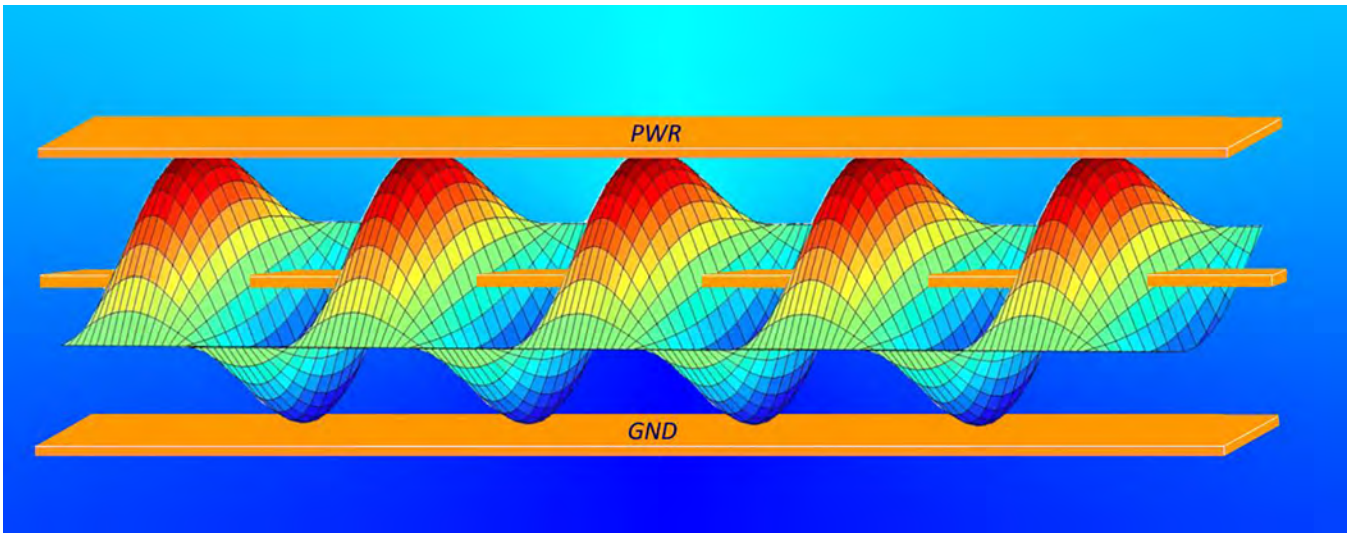

Figure 3: Digital signals travel as a wave of electromagnetic energy in a multilayer PCB.

So, what about crosstalk in the return path of the reference planes as the current weaves its way back through the expansive wasteland of copper? This column followed my previous column "Return-Path Discontinuities" [3] and elaborated on crosstalk in the unseen "dark side" of the signal.

3. Next-gen PCBs: Substrate-integrated Waveguides

As PCB transmission frequencies head toward 100 GHz and beyond, the current mainstream PCB technology—the copper interconnect—is reaching its performance threshold. Ultimately, it is dielectric loss, copper roughness, and data transfer capacity that are the culprits. However, the biggest performance restriction for PCB interconnects is the size of the conductor. Metallic waveguides are a better option compared to traditional transmission lines, but they are bulky, expensive, and non-planar in nature.

Recently, substrate integrated waveguides (SIW) structures have emerged as a viable alternative and are ideally suited to the high-speed transmission of electromagnetic waves. SIW are planar structures fabricated using two periodic rows of PTH vias or slots connecting the top and bottom copper ground planes of a dielectric substrate. In this column, I reviewed the substrate integrated waveguide and its incorporation with the microstrip transmission line.

2. Stackup Planning, Parts 1-5

Design methodologies change over time, particularly in the ways to simulate electromagnetic fields and return current paths. In my first four columns on stackup planning, I described the traditional stackup structures that use a combination of signal and power/ground planes. But to achieve the next level in stackup design, one needs to not only consider the placement of signal and plane layers in the stackup but also visualize the electromagnetic fields that propagate the signals through the substrate. Part 5 covers all of the latest concepts in stackup design (Figure 3).

1. The 10 Fundamental Rules of High-speed PCB Design, Parts 1-5

Over the years, in a plethora of published technical articles, I have focused on high-speed design, signal and power integrity, and EMC design techniques. All of these have key points to consider and present a tremendous amount of information to absorb. In this five-part series, I reflected on the 10 most important considerations to embrace to achieve a successful high-speed PCB design that performs reliably to expectations. These 10 golden rules should be the prime checklist for all high-speed PCB designers (Figure 4).

Moving forward, does anyone have a suggestion for the theme of my 101st column? How about "Signal Integrity 101"? Feel free suggest

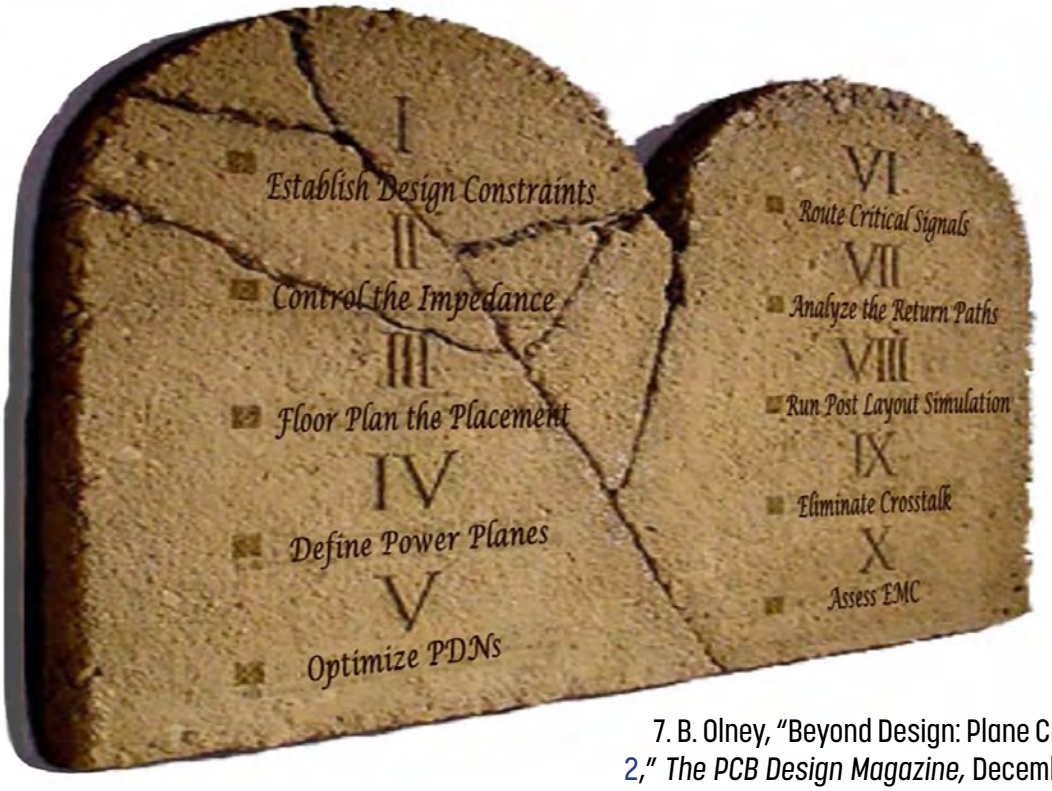

Figure 4: The 10 fundamental rules of high-speed PCB design.

a topic through the link on my columnist page (left side). **DESIGN007**

Editor's Note: The references correspond with the numbered headings, and the further reading suggestions correspond with the superscripts throughout the column.

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Barry Olney is managing director of In-Circuit Design Pty Ltd. (iCD), Australia, a PCB design service bureau that specializes in board-level simulation. The company developed the iCD Design Integrity software incorporating the iCD Stackup, PDN, and CPW Planner. The software can be downloaded www.icd.com.au. To read past columns or contact Olney, click here.

Recent IPC DC Chapter Activities

The Digital Layout

by Stephen V. Chavez, MIT, CID+, IPC DESIGNERS COUNCIL

We're onto the second half of the year now, and we've seen lots of activities within our local Designers Council (DC) Chapters, including a few international chapters as well. It's great to see and hear of the continued activities from professional development to knowledge sharing and networking taking place at various industry events. Here is a snapshot of what has taken place so far from several of our active chapters.

If you are involved in discussions, whether it is in a small or a large group, about industry content regarding PCB design, fabrication, or assembly, but you are not part of IPC, then I highly recommend you contact me so that I can assist you in joining the IPC collective. It's totally free and well worth it! And if you are an industry veteran with lots of experience, yet not active in IPC, or simply a college student starting your career, this is a great group to join and get plugged in. I hope to hear from those who are not part of IPC, especially within a DC Chapter.

Silicon Valley Chapter, California

Chapter Leader: Bob McCreight

Bob McCreight

Around 32 people attended our Q3 meeting on July 25. Many thanks to Altium, Amazon, and the guest speakers. To start the meeting, we were treated to a nice greeting from Umar Shah and Charles Rusch from Amazon Lab126. Then, we went around the room, and each attendee introduced themselves. It was nice to put faces with the names. Stephen Golemme followed with a quick presentation about the IPC-2231

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standards committee he is part of. Next, Judy Warner talked about AltiumLive 2019 and her OnTrack podcast.

The feature presentation by Vincent Himpe of Tesla was well received and sparked some lively discussion. His talk, "What's in a Name: Making Sure There Is No Ambiguity When Exchanging Data," explored several key items. He touched on schematic symbols, reference designators, footprints, net names, component values, and file names.

Our next meeting will be October 24 in San Jose. Zuken will host, and Pal Pilot will sponsor lunch.

Scott Nuance from Optimum Design Associates will present "Best Practices for RF and Mixed Technology PCB Design." I will be setting up the invitation in a few weeks, so save the date.

Cascade Chapter (Seattle), Washington

Chapter Leader: Tim Mullin


Tim Mullin

In addition to my role as the Cascade Chapter president, other board members include Paul Brendt (VP), Jerome Larez (treasurer), Aubrey Moore (secretary), Cherie Litson (education chairperson), and Cory Grunwald (webmaster).

Held at the Lake Washington Institute of Technology, we had our Q1 meeting in April. Dinner was sponsored by Aerotek, and speakers included Cherie Litson, Tim Mullin, and Jerome Larez. The roundtable discussion covered three topics: cutting-edge technologies, IPC standards, and materials and processes. Held in June, Mentor was the dinner sponsor for the Q2 meeting, and the guest speaker was Robert Hanson, who discussed "Achieving Signal Integrity and Meeting EMI Radiation Requirements."

The speakers and topics are still to be determined, but our Q3 meeting will be held on September 18, and the Q4 meeting will be December 4, both at the Lake Washington Institute of Technology. Mark your calendars!

Research Triangle Park (RTP) Chapter, North Carolina

Chapter Leader: Tony Cosentino


Tony Cosentino

The Research Triangle Park (RTP) Chapter supports the Raleigh-Durham area, and we held our first meeting at the end of January, including an election for the new slate of leaders: myself as president, Randy Faucette (VP), Steve Trasatto (treasurer), Ian Jackson (secretary), and Lance Olive (membership). Hosted by Protolabs in Morrisville, North Carolina, the guest speaker was Eric Utley, applications engineer at Protolabs, who spoke on "3D Printing: Beyond Prototyping." The 24 attendees also toured the Protolabs facility.

Our March meeting including 20 attendees and was hosted by CertifiGroup in Cary, North Carolina. Josh Hunt, field service manager at CertifiGroup, addressed "Environmental Testing for Reliability of Products and Components." There was also a site tour of the CertifiGroup facility.

In June, there were 25 attendees. Ian Jackson, the elected secretary, dropped out of office due to workload issues, and the position is open and being backfilled by Steve Trasatto, the current treasurer. Hosted by Ixia, a Keysight Business, in Morrisville, North Carolina, guest speakers Shruthi Soora and Dr. Mike Barts from the Wireless Research Center addressed "PCB Antenna Considerations From Concept to Certification."

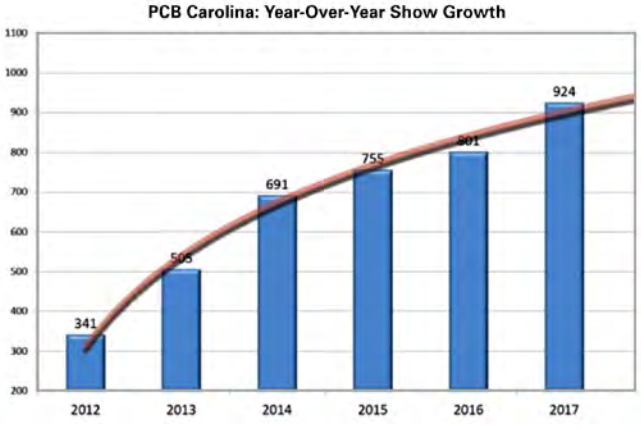
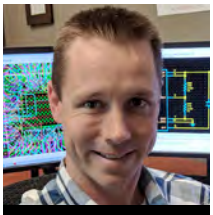


Figure 1: Year-over-year growth for PCB Carolina.

July and August served as a summer break for the chapter, and the date and details for the September meeting will be announced soon. In addition, PCB Carolina 2019 is approaching and will be held November 13 at the McKimmon Center at North Carolina State University in Raleigh. It's free to all attendees and includes a keynote and 16 technical sessions. Based on last year, the projected attendance is 1,000 attendees, and the vendor floor is already sold out (Figure 1).

San Diego Chapter: California

Chapter Leader: Luke Hausherr


Luke Hausherr

Our last meeting was held at the Del Mar Electronics show with around 35 attendees. Altium paid for everybody's lunch. I made my debut as the new chapter president since Bob Griffith has retired. I gave a short speech thanking the community for their support and explained my objectives to increase membership. John Carney from Cadence is now the secretary, and Judy Warner from Altium joins the team as education chair.

Gerry Partida—the director of engineering for Summit Interconnect in Anaheim, California—spoke on "CAD to PCB: Your Data and What I Actually Do With It." His presentation provided a great overview in understanding the input and data review process of your design data in front-end engineering departments at PCB fabrication companies. We then had a raffle where we gave away a bunch of vendor- and chapter-sponsored items.

Our next meeting will be held at San Diego PCB in September. Jeffrey Jenkins, PCB chief technologist at L3 Communications, will be giving a presentation about conformal coating, what is it, and why to use it.

Orange County Chapter, California

Chapter Leader: Scott McCurdy

We had our latest "lunch 'n learn" chapter meeting on July 18 at JT Schmid's Restaurant banquet room in Anaheim, California. We had a very well-attended event with 68 designers and PCB professionals in the audience. The topic was "How Fabrication Processes Determine DFM Guidelines" presented by Julie Ellis, field applications engineer at TTM Technologies Inc. She gave a detailed look at fabrication realities to help designers understand capabilities and tradeoffs. It was very educational and generated lots of questions from the audience.


Scott McCurdy

I wish to thank Altium for sponsoring much of the lunch cost of the meeting and also for providing a three-day pass to their upcoming AltiumLive event in San Diego as one of our door prizes. PCB Libraries provided a generous grand prize for a one-year Cloud License of their full-featured PCB Library Expert Enterprise tool. We also had other raffle prizes donated by Mentor and Freedom CAD Services.

International Chapters

Our international chapters continue to be very active, two of which have been showcased in recent columns. The Monterrey Chapter is led by Luis Saracho, and the Sonora Chapter is headed by Robert Ivan Villalba Gonzalez.

IPC CID/CID+ Certification Success

by Stephen V. Chavez, MIT, CID+

We continue to have successful IPC CID and CID + certifications classes to date, resulting in many new and seasoned engineers and designers successfully achieving their certifications. Congratulations to all who have recently successfully achieved their new IPC CDI/CDI + certification! Welcome to the family!

In the next section, you will find the remaining training sessions to take advantage of as well as upcoming PCB design events.

2019 Training and Certification Schedule

IPC Certified Interconnect Designer (CID)

- September 19–22: Schaumburg, IL
- October 8-11: Carmel, IN
- October 21–24: Anaheim, CA
- November 2–5: Raleigh, NC
- November 5–8: Dallas, TX

IPC Advanced Certified Interconnect Designer CID+

- September 10–13: Kirkland, WA
- September 17–20: Schaumburg, IL
- October 21–24: Anaheim, CA
- November 2–5: Raleigh, NC
- December 3–6: Manchester, NH

Note: Dates and locations are subject to change. Contact EPTAC Corporation to check current dates and availability. A minimum enrollment of seven students is required for a class to be held.

PCB Design Events

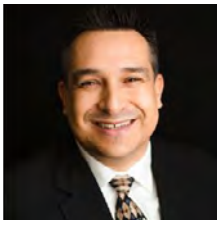
AltiumLive 2019

- October 9–11: San Diego, CA

PCB Carolina 2019

- November 13: Raleigh, NC

The IPC Designers Council is an international network of designers. Its mission is to promote printed circuit board design as a profession and to encourage, facilitate, and promote the exchange of information and integration of new design concepts through communications, seminars, workshops, and professional certification through a network of local chapters. **DESIGN007**



Stephen Chavez is a member of the IPC Designers Council Executive Board and chairman of the communications subcommittee. To read past columns or contact Chavez, click here.

Spreading Light Over Quantum Computers

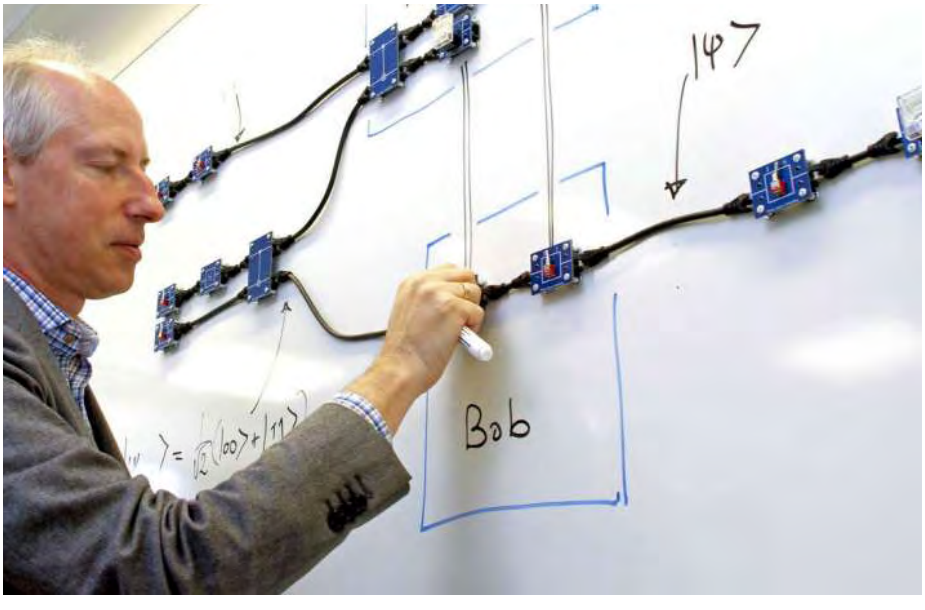
Researchers at KU Leuven and imec have successfully developed a new technique to insulate microchips. The technique uses metal-organic frameworks, a new type of materials consisting of structured nanopores. In the long term, this method can be used for the development of even smaller and more powerful chips that consume less energy. The team has received an ERC Proof of Concept grant to further their research.

Computer chips are getting increasingly smaller. That's not new: Gordon Moore, one of the founders of chip manufacturer Intel, already predicted it in 1965.

But this continued reduction in size also brings with it a number of obstacles. The switches and wires are packed together so tightly that they generate more resistance. This, in turn, causes the chip to consume more energy to send signals.

A study led by KU Leuven professor Rob Ameloot (Department of Microbial and Molecular systems) shows that a new technique might provide the solution.

"We're using metal-organic frameworks (MOFs) as the insulating substance. These are materials that consist of metal ions and organic molecules. Together, they form a crystal that is porous yet sturdy," says Ameloot. "Now, we just have to refine the finishing. The surface of the crystals is still irregular at the moment. We have to smoothen this to integrate the material in a chip."



Once the technique has been perfected, it can be used to create powerful, small chips that consume less energy.

(Source: Linköping University)

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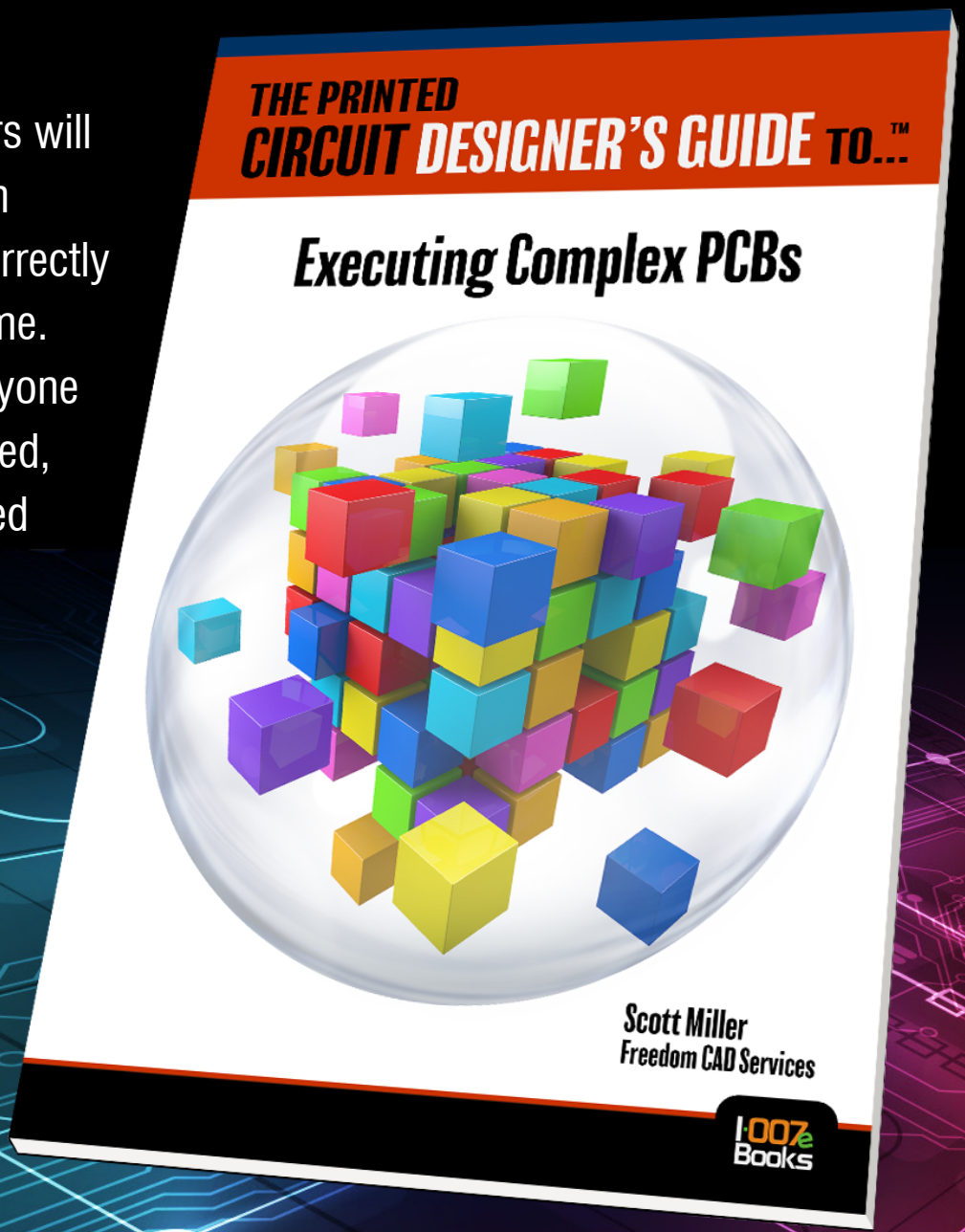

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A Proactive Approach to Controlled Impedance

Connect the Dots

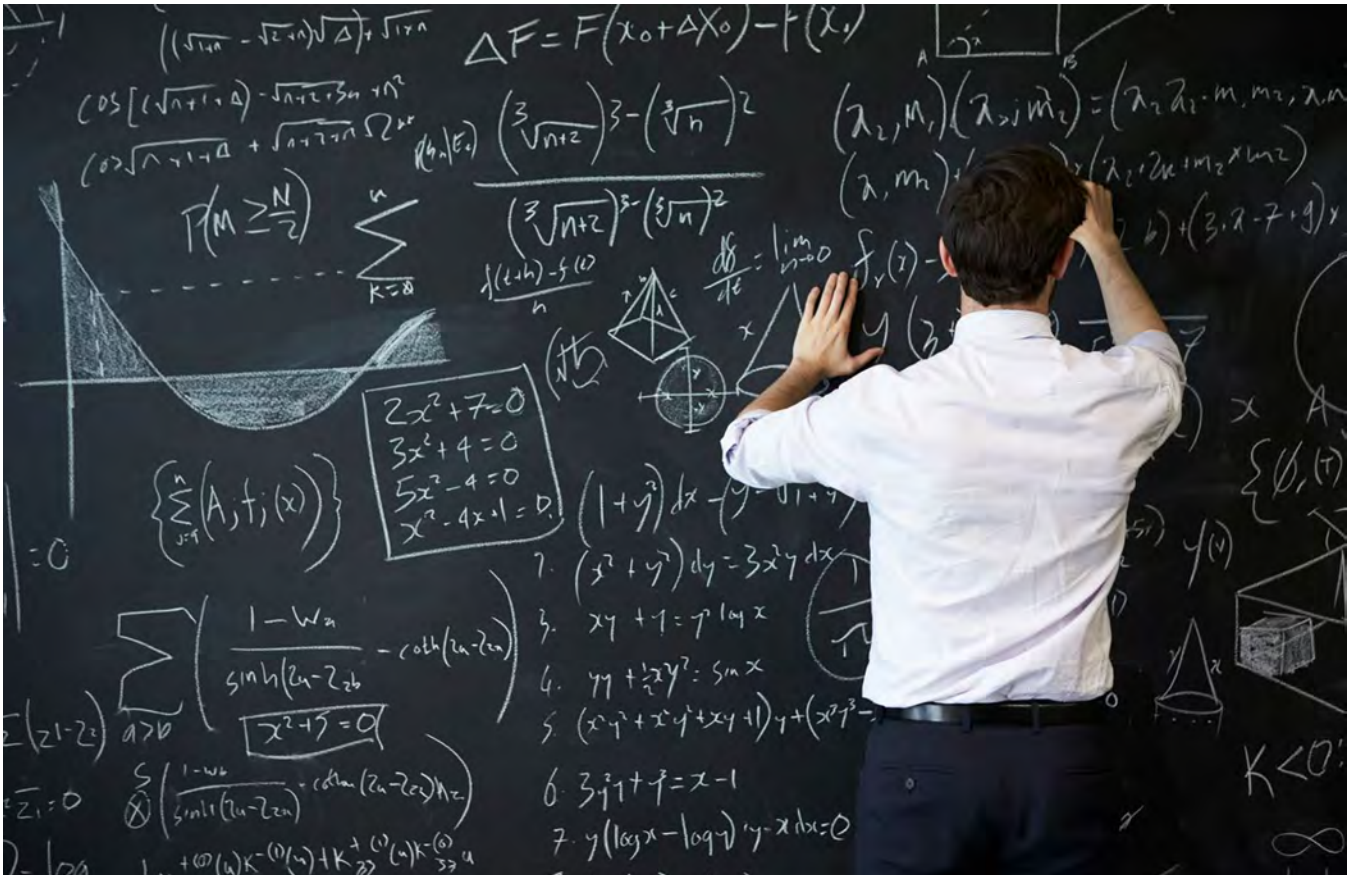
by Bob Tise, SUNSTONE CIRCUITS

Most can agree that controlling impedance is critical to signal integrity and board performance in devices powering high-speed digital applications, telecommunications, or RF communications. How to do so is another matter. It is common practice to include impedance-related notes with a PCB design and rely on the manufacturer to determine the proper trace parameters. This inherently passive methodology often leads to delays, cost overruns, and even batches of useless boards.

PCB trace impedance is determined by its inductive and capacitive reactance, resistance, and conductance, usually ranging from 25–125 ohms. Factors dictating impedance include:

- The distance from other copper features
- The width and thickness of the copper signal trace
- The thickness of material on either side of the copper trace
- The dielectric constant of board material

You can save time, money, and effort if you are aware of the impedance math when you sit down to design your board. Gain this aware-



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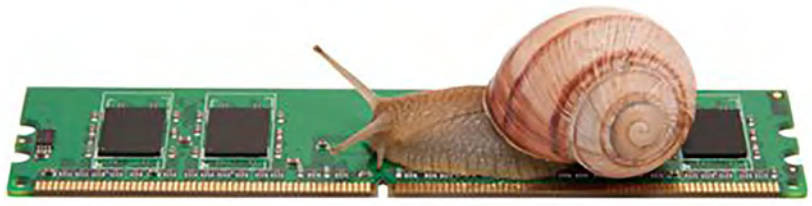

Figure 1: Assumptions can slow you down.

ness by using a good impedance calculator, and you can build the right tolerances into your design. Impedance testing becomes a double-check of your work instead of the tool you rely on to tell you if your documentation is correct. Documenting impedance requirements properly is more onerous than most people realize. Though it seems simple (e.g., state your target impedance, trace requirements, and material tolerances), PCB documentation is a details game that often leaves knowledge gaps for your manufacturer.

For example, picture a design for a four-layer board with two signal layers and two planes and a seemingly complete set of drawing notes. Now, let's say the documentation doesn't specify if both signal layers and trace widths require impedance control. In this case, the board manufacturer makes assumptions and heads for production or kicks it back to the designer for clarification. One scenario slows you down, and the other risks manufacture of boards that may not work properly (Figure 1).

At Sunstone, we believe that a proactive design method, not reliance on testing, is the best way to control impedance and set the stage for an efficient production of quality boards, which is just as important. PCB impedance callouts are helpful, but they are not as foolproof as simply crafting a design with the right distance to the reference plane, trace widths, and materials tolerances. Incomplete or incorrect impedance-related notes are common and can directly impact both board cost and performance. Delays result when notes do not match design, there are two trace widths for the same impedance on the same layer, or each signal layer does not have its own impedance requirements. Sometimes, the adjustments required are not possible because they cause interference with other features.

Lack of specificity in the notes can result in extra effort when you transition from design to manufacture. The documentation typically defines the impedance, not the trace size, or gives a trace width that covers the whole board. Determining the trace size, in this case, falls to your manufacturer. They can vary trace width, height, and thickness to ensure the correct impedance, but they cannot read minds.

More often than not, manufacturers will not know for sure what type of product the board will be used in or if there are underlying reasons why the trace size is just as critical as the defined impedance. At Sunstone, we much prefer it when the design shows us what the trace sizes should be versus working backward from the impedance-related notes.

The math is the math when it comes to controlled impedance, and it has to be done at some point. Why not do it during the design phase rather than after it? If you know the right trace width, draw it in; it doesn't have to be hard work. There are a variety of free online controlled impedance calculators available to make the math easy. There's no point in solving a quadratic equation (if it were only that easy) with a pencil and paper if there's a button on your calculator that will do it in less than a second.

$$Z_0 = \frac{\eta_0}{2\pi\sqrt{2}\sqrt{E_r+1}} \cdot \ln\left(1 + 4 \cdot \left(\frac{h}{w_{eff}}\right) \cdot (X_1 + X_2)\right)$$

Where

$$W_{eff} = W + \left(\frac{t}{\pi}\right) \cdot ln\left\{\frac{4e}{\sqrt{\left(\frac{t}{h}\right)^2 + \left(\frac{t}{w\pi + 1.1t\pi}\right)^2}}\right\} \cdot \frac{E_r + 1}{2 \cdot E_r}$$

$$X_1 = 4\left(\frac{14E_r + 8}{11E_r}\right)\left(\frac{h}{W_{eff}}\right)$$

$$X_2 = \sqrt{16 \cdot \left(\frac{h}{W_{eff}}\right)^2 \cdot \left(\frac{14 \cdot E_r + 8}{11 \cdot E_r}\right)^2 + \left(\frac{E_r + 1}{2 \cdot E_r}\right) \cdot \pi^2}$$

Figure 2: Example controlled impedance equation.

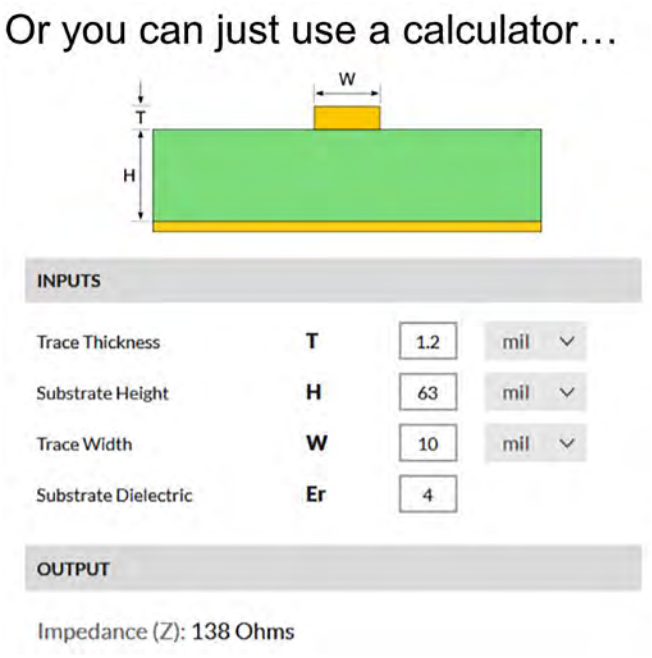

Figure 3. The same equation, using a calculator. (Source: EEWeb)

If you feel like breaking out the papyrus and doing the math yourself, Figure 2 shows one of the simpler equations. Otherwise, you can just use a calculator (Figure 3).

Conclusion

Your documentation should not be a confusing ambiguity. When you design for controlled impedance, the documentation instead becomes a double-check that can help speed your design through the manufacturing process. If you design your board to hit the exact impedance number that would otherwise be called out in the documentation, you should be well within the manufacturer's tolerance range.

I recognize that testing is important in many instances, such as when there are high performance or special materials requirements. In any case, tests are far more enjoyable when you know the answers to the questions beforehand. When you integrate impedance math into your design process, you get quality boards faster and more efficiently. **DESIGN007**

Bob Tise is an engineer at Sunstone Circuits. To read past columns or contact Tise, click here.

Researchers Develop Rapid, Low-cost Method to 3D Print Microfluidic Devices

Microfluidics is the manipulation and study of sub-microscopic liters of fluids. The current gold standard for the fabrication of microfluidic devices is soft lithography where elastomeric materials are casted on a mold fabricated in a cleanroom.

3D printing emerged as an attractive alternative to soft lithography. 3D printers turn a design into working prototypes in the order of hours, and the recent introduction of low-cost 3D printers make 3D printing more accessible in general to researchers. Current 3D printing technologies for the fabrication of microfluidic devices have a few limitations: available materials for 3D printing, achievable dimensions of microchannels by commercial 3D printers, and integration of 3D-printed microfluidics with functional materials or substrates.

To overcome these challenges, researchers from the Singapore University of Technology and Design's (SUTD's) Soft Fluidics Lab have developed an alternative method to apply 3D printing for the fabrication of microchannels. The researchers applied direct ink writing (DIW) 3D printing of fast-curing silicone sealant to fabricate microfluidic devices rapidly on various substrates. The design of fluidic channels is determined by the patterned silicone sealant while the top and bottom transparent substrates seal the channels.

"Our approach to apply DIW 3D printing allows direct patterning of microchannels essentially on any flat substrate," said Assistant Professor Michinao Hashimoto, the principal investigator of the project. The team also demonstrated the ease of patterning of silicone barriers directly on an off-the-shelf PCB, immediately integrating electrodes into the microchannels that would function as real-time flow sensors.

(Source: SUTD)

Six Key Points for Designing a Defect-free Conformal Coatings Process

Sensible Design
by Phil Kinner, ELECTROLUBE

In my last column, I gave a summary of essential factors to consider when embarking on conformal coating selection and looked at those all-important considerations to get the best performance for your application. In this column, I cover six commonly asked questions about conformal coatings that every design engineer should be mindful of when specifying the coating process. Identifying potential production problems at the design stage will always be favourable and far easier than trying to fix problems or concerns following the conclusion of the engineering drawings. So, let's return to our trusted Q&A format and explore these key points in more detail, which I hope will help you achieve the best outcomes for your coating processes and make new production friends in the meantime!

1. How Important Is the Reworkability Characteristic of a Coating?

Believe it or not, the reworkability of a coating can often be a very important consideration in the selection of a conformal coating, especially when boards are of high value and have long service-life expectancies (e.g., military and aerospace assemblies). A coating may display many favourable characteristics that make it superior for assembly protection in the field, but it might also make the assembly very difficult to rework in the factory or repair in the field. A difficult-to-rework coating will not only make repairs and upgrades time-consuming but also add cost and complexity to the product.

If the assembly is likely to require repairs, modifications, or upgrades, then consideration

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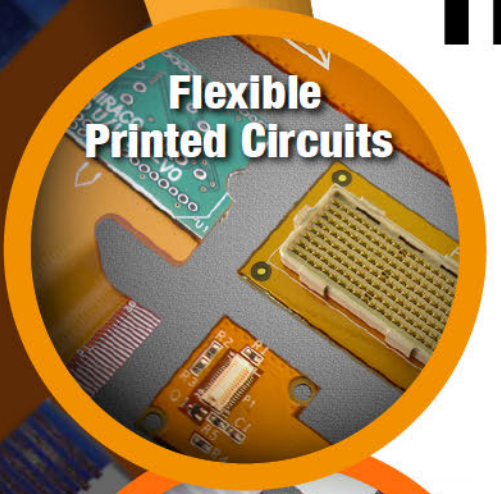

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should be given to the ease of removal of the coating. During the rework or repair process, it is likely that components will be replaced. Thus, it is highly advantageous that the coating can be easily and cleanly removed from the required areas to facilitate these repairs and that the coating has good adhesion to itself to ensure that an effective and permanent seal can be made to the repaired area. Complex issues can be avoided entirely if the reworkability factor is accounted for during the coating selection process. Manufacturers like us offer products for the effective removal of conformal coatings, including those that are solvent-resistant, but with the right conformal coating product for your application, it can be easy to completely remove the entire conformal coating prior to repair. Keep reworkability in mind when selecting your coating product to save yourself a lot of aggravation in the long term.

Keep reworkability in mind when selecting your coating product to save yourself a lot of aggravation in the long term.

2. Does a Thicker Level of Coating Coverage Equal Greater Protection?

This is a good question that we get asked a lot, and the simple answer is, "It depends." Thicker coating coverage can achieve greater protection of your assembly from an end-use environment. However, it is not unusual for end users to push the limits on coating thickness, favouring thicker films of coating for a number of reasons, such as protecting the assembly from a harsh environment or simply for additional peace of mind. That being said, conformal coatings should not be applied in thicknesses greater than necessary nor exceed the thickness they were designed to be applied at.

In fact, very thick application of conformal coatings can actually result in harmful levels of stress on components, vastly extend the manufacturing/curing times, and depending on the cure method, cause inadequate adhesion to the substrate. Designers should not specify coating fillets around bottom-terminated components (BTCs)—such as ball grid arrays (BGAs) or quad flat no-leads (QFNs)—as capillary forces will pull conventional coatings under the part, which may result in reduced solder joint lifetime, especially during thermal transitions. Conformal coatings are normally applied to circuit boards by dipping or spraying, typically at a thickness of 20–50 microns, although conventional silicone and other specialist coatings can be applied at up to 200 microns.

However, we have created an interesting option for the industry by developing the two-part (2K) coatings range, which can be applied at much greater thicknesses, from 100–300 µm greater than the average coating. But there is a reason for this. 2K conformal coatings are solvent-free and have been formulated to perform at these greater thicknesses with the same ease of application as a conventional conformal coating and are particularly suitable for protection against harsh, condensing environments. So, there certainly won't be any need for angst over coating thickness with 2K coatings!

However, to obtain the maximum levels of protection available from the coating, it is imperative that the coating is applied in the ranges of thickness specified on the datasheet. If you are in any doubt about appropriate coating thickness, always consult the datasheet or get the advice of a reputable supplier; they have laboured hard to establish optimum coating thicknesses for their products in all kinds of operating environments. You really don't need to apply coatings any thicker than specified for additional protection or it could result in diminishing returns later on. Instead, work on achieving the very best degree of coverage for a given thickness range. Coverage is often more important than thickness, except in the harshest environments.

3. How Can Designers Ensure a Smoother Production Process?

For example, how do they indicate whether it really doesn't matter if a component is coated or not? When design and production work seamlessly well together, the outcome will nearly always be successful, particularly when a designer understands the intricacies of conformal coatings. One area where designers can help their production colleagues is to specify where coatings are optional, or where there are "don't care" areas, in the engineering drawing.

For instance, consider LEDs on a circuit board. When the spectral output of the LED is important to the product function, and coating the LED would interfere with that function, then the LED should not be coated. If the LED is on the assembly as a test select, and the presence of conformal coating (assuming transparency) does not interfere with the assembly function, then it may be coated. In specifying the optional coating, the designer provides more flexibility to the coater in assembly operations. It is best practice to specify the areas that need to be coated and the areas that don't as well as the "don't care" areas to help the coating process run as smoothly as possible.

4. Can a Designer's Instructions Be Easily Misconstrued?

We might need to duck for cover here, but the answer is yes! Engineering drawings should avoid specifying "100% coverage," as this means numerous things to different people. The only real way to get 100% coating is to have assemblies with no connectors or uncoated components, and they must be either dip-coated or vapor-deposited. In practice, you can only inspect coatings in areas that are visible to the inspectors. Inaccessible areas cannot be inspected.

5. How Is Coating Thickness Specified?

Cured conformal coating thickness varies by chemistry. It's also advisable to be aware of what these coverage requirements do to your resulting application method. Adequate coverage—particularly on corners, sides, or under leads—can be a challenge in thin-film applications; meanwhile, thick-film processes can increase the flow characteristics of a coating application and can be more difficult to manage around no-coat areas.

When specifying the thickness of a coating on an engineering drawing, the industry practice is to measure coating on a flat, unencumbered area of the assembly, and not on items like component leads. As many modern assemblies are very component-dense, it is often difficult to find a flat, unencumbered area of the assembly. Consequently, it is a common and accepted practice to use witness or process control coupons for such measurement.

Designers will need to know that the nominal thickness measured on flat, unencumbered areas or witness coupons will have no relation to the thickness of coating achieved on the corner of a discrete, or the leads of ICs, where the thickness might be one micron or less with a nominal thickness of 25 or 50 microns. In a recent study performed by the IPC titled "Conformal Coating: State of the Industry," there were some very eye-opening results for many folks who assumed they were getting 25 microns everywhere. Again, the key takeaway is nominal coating thickness is a process indicator only; the actual coverage on leads and components is far more important to the reliability of the assembly, which should be understood by all parties. The goal is the greatest degree of coverage possible, and cross-sections should be performed to understand how the application process is delivering this critical to success parameter. The witness coupon will only tell you if your process has changed significantly.

6. How Is the Best Method of Application Determined?

There isn't necessarily a best method to apply a conformal coating. Choosing the most pertinent application method for a particular assembly will depend on which existing equipment is available to the manufacturer, the coating processes in use, the average time interval between the start of production of one unit, and the start of the next and the overall design

of the assembly, which will dictate what can and cannot be achieved. This includes those areas of the circuit that must be coated and those that must not (e.g., connectors, switches, test points, RF shielding, etc.). The best application method would ensure that each board to be coated receives coating coverage on all required metal surfaces at a sufficient thickness to afford protection against the environment. These requirements will change from board design to board design, and environment to environment; invariably, they need to be tested and verified ahead of the production run.

Conclusion

Implementing a defect-free conformal coating process is a fine balance of material selection, understanding the engineering requirements for coverage (coat, no-coat, and "don't care" areas), and thickness as well as choosing a suitable application method. Understanding the subtleties of conformal coatings will pay huge dividends in providing an engineering drawing that isn't prone to misinterpretation and making the production team's lives easier.

When it comes to designing for conformal coating, there's a great deal more to discuss. Over the following months, I hope to provide more useful tips and design advice that will help you accomplish reliable circuit protection. At Electrolube, we talk solutions every day, so if you have any questions about conformal coating selection, performance, thickness, coverage, etc., please do talk to us. **DESIGN007**

Phil Kinner is the global business and technical director of conformal coatings at Electrolube. To read past columns or contact Kinner, click here. Kinner is also the author of *The Printed Circuit Assembler's Guide to... Conformal Coatings for Harsh Environments*. Visit I-007eBooks.com to download this and other free, educational titles.

At the Edge of Chaos, Powerful New Electronics Could be Created

A phenomenon that is well known from chaos theory was observed in a material for the first time ever, by scientists from the University of Groningen, the Netherlands.

A team of physicists at the University of Groningen, led by Professor of Functional Nanomaterials Beatriz Noheda, made their observation in thin films of barium titanate ($BaTiO_3$), a ferroelastic material. Ferroic materials are characterized by their ordered structure, in shape (ferroelastic), charge (ferroelectric) or magnetic moment (ferromagnetic), for example. "These materials are always crystals in which the atoms are arranged with characteristic symmetries," Noheda explains.

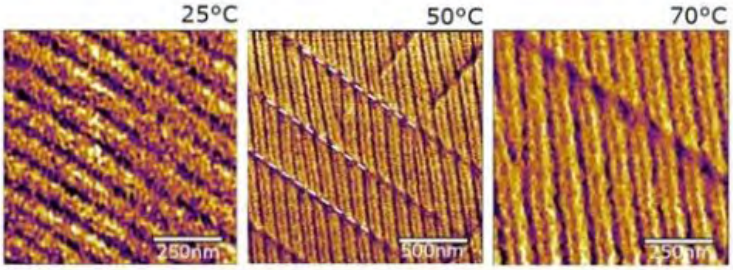
Electric or magnetic dipoles are aligned within domains in the crystals. However, the dipoles could be pointing up or down, as both states are equivalent. As a result, crystals of these materials will have both types of domains. The same goes for ferroelastic materials, best known for their shape memory. In this case, however, the situation is a bit more complicated.

Noheda explains, "The unit cells in these crystals are elongated, which means that domains of the different unit cells do not easily match in shape. This creates an elastic strain that reduces the crystal stability."

Increasing the temperature increases the disorder (entropy) in the material. When the transition starts, domain walls of the new phase appear gradually and both phases exist together at intermediate temperatures (30°C to 50°C).

Thus, a ferroelectric material at the edge of chaos could give a highly diverse response over a small range of input voltages. The paper in *Physical Review Letters* is a proof of principle, showing how a material can be designed to exist at the edge of chaos, where it is highly responsive.

(Source: University of Groningen)



Domain walls in barium titanate at increasing temperature (please note different scales). (Image: Noheda lab)

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MilAero007 Highlights

The Government Circuit: Trump Praises Industry on Workforce Issues, IPC Launches Grassroots Platform ▸

This summer has been productive for IPC on the government relations front. Most notably, IPC's workforce development efforts were recognized at the White House in Washington and on a factory floor in Michigan. On another front, we've launched an online platform that makes it easier for our members to contact their elected officials, and we're using it to seek more R&D funding for an important industry project.

Artificial Intelligence and Space Exploration ▸

From utilizing machine learning to advancing space exploration, optics technology leads the chart toward our scientific and outer-space frontiers.

National Security in a Quantum World ▸

Imperial College London's security institute recently hosted an event on how quantum technology will impact national security. Advances in quantum technology, which applies quantum science in real-world applications, are poised to have a huge impact on national security.

Extending Field of View in Advanced Imaging Systems ▸

The military relies on advanced imaging systems for a number of critical capabilities and applications—from Intelligence, Surveillance, and Reconnaissance (ISR) and situational awareness to weapon sights. These powerful systems enable defense users to capture and analyze visual data, providing key insights both on and off the battlefield.

Innovators from NASA, Lockheed Martin Space, and Lenovo to Keynote SMTA International 2019 ▸

The SMTA is pleased to announce three inspiring keynote presentations scheduled during SMTA International, September 22–26, 2019 in Rosemont, Illinois, USA.

iNEMI Publishes Product Sector Chapters from the 2019 Roadmap ▸

The International Electronics Manufacturing Initiative (iNEMI) today announced the release of four of the seven Product Emulator Group (PEG) chapters of the 2019 Roadmap.

Raytheon Developing Advanced Laser Systems for U.S. Air Force Deployment ▸

Raytheon Company will build two prototype high energy laser systems to be deployed to troops overseas under a U.S. Air Force contract. Soldiers will use the HEL system to destroy hostile drones.

MDA Awards Lockheed Martin $240M Contract to Support Ballistic Missile Defense Modeling and Simulation ▸

The Missile Defense Agency (MDA) awarded Lockheed Martin a $240 million contract to support the modeling and simulation framework for the Ballistic Missile Defense System (BMDS).

Missile Defense Agency's Long Range Discrimination Radar Reaches Major Milestone ▸

The radar system will serve as a critical sensor within MDA's layered defense strategy to protect the U.S. homeland from ballistic missile attacks.

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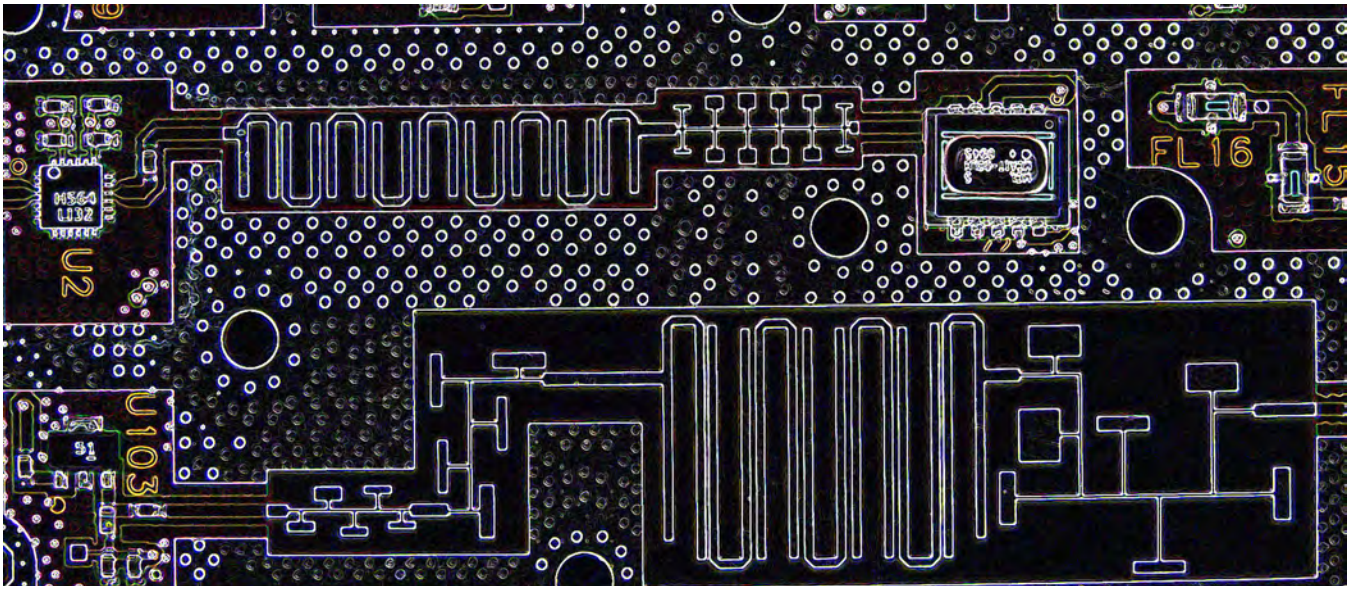

Insertion Loss Performance

Differences Due to Plated Finish and Circuit Structure

Article by John Coonrod
ROGERS CORPORATION

Abstract

Many final plated finishes are used in the PCB industry, each with its own influence on insertion loss. The impact of an applied finish on insertion loss generally depends on frequency, circuit thickness, and design configuration. This article will evaluate the effects of final plated finishes on the insertion loss of two popular high-frequency circuit design configurations: microstrip transmission-line circuits and grounded coplanar-waveguide (GCPW) transmission-line circuits.

Data will be presented for loss versus frequency for six plated finishes commonly used in the PCB industry, and opinions will be offered as to why the loss behavior differs for the different plated finishes and for the various circuit configurations. Because the insertion loss of high-frequency circuits also depends on substrate thickness, circuits fabricated on substrates with various thicknesses will be evaluated to analyze the effects of substrate thickness on insertion loss using various plated thicknesses.

This article will also explore many aspects of the final plated finishes on PCB performance. The nickel thickness in electroless nickel immersion gold (ENIG) finishes normally has some variations; data will show the effects of these variations on the RF performance of a PCB. Immersion tin is often used to minimize thickness variations and analysis will show the effects on RF performance for different thicknesses of immersion tin. The effects of plated finish on PCB performance can vary widely over frequency, and those effects will be shown for a wide range of frequencies from 1 to 100 GHz.

Insertion Loss Overview

The insertion loss of a high-frequency PCB circuit can decrease the usable signal levels of a system, whether in a receiver or a transmitter. Details on insertion loss can be found in a previous IPC paper [1], although a simple review of insertion loss might be helpful before examining the data on PCB final plated finishes. The total insertion loss (αT) is comprised of four loss components:

$$\alpha_T = \alpha_C + \alpha_D + \alpha_R + \alpha_L$$

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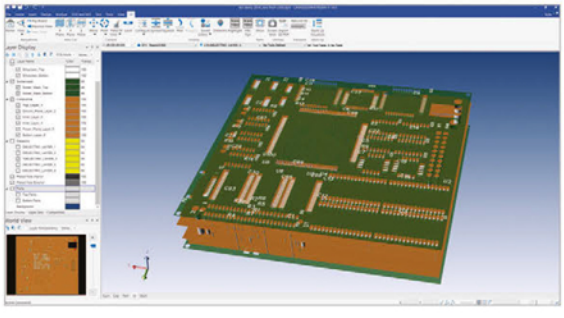

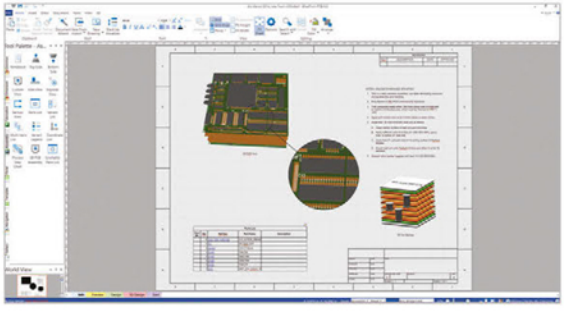

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Where α_C = conductor loss, α_D = dielectric loss, α_R = radiation loss, and α_L = leakage loss.

Leakage loss (α_L) is typically ignored when using high-frequency substrates due to the very high-level volume resistivity of the circuit material. If the material is semiconductor grade where volume resistivity is not high, leakage losses may be a concern. Leakage loss is more of a concern for certain applications, although those are typically high-power circuits. The evaluations in this article are for low-power circuits.

Radiation loss (α_R) can be difficult to assess because it depends on many factors. It will be ignored in the present article because the circuits under study are relatively low in radiation loss. However, readers interested in radiation loss can learn more from a previous IPC paper. [2]

To evaluate the effects of final plated finish on PCB performance, this study will focus on conductor loss and dielectric loss as are graphically depicted in Figure 1.

As Figure 1 shows, a circuit using a thinner substrate will have higher insertion loss than a circuit on a thicker substrate, largely due to conductor loss. For the 30-mil circuit material at the far right (the thickest substrate), the insertion loss is relatively low, and the dominant loss component is dielectric loss, largely due to the dissipation factor (Df) of the circuit material. In general, circuits fabricated on thinner substrates are more sensitive to differences in the conductor. Plated finishes will have an impact on a cir-

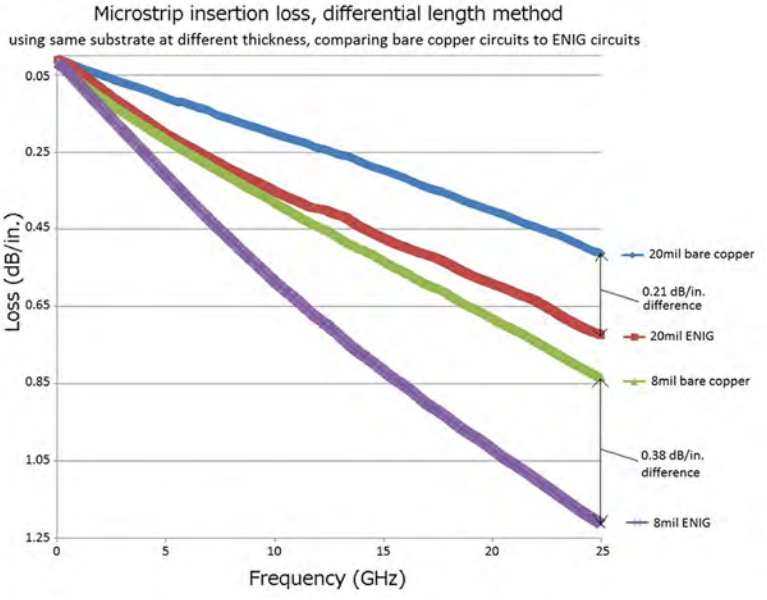

Figure 2: These plots of loss versus frequency for the same circuit material with different thicknesses and with and without ENIG finish show that circuits on thinner substrates are more impacted by loss than circuits on thicker substrates.

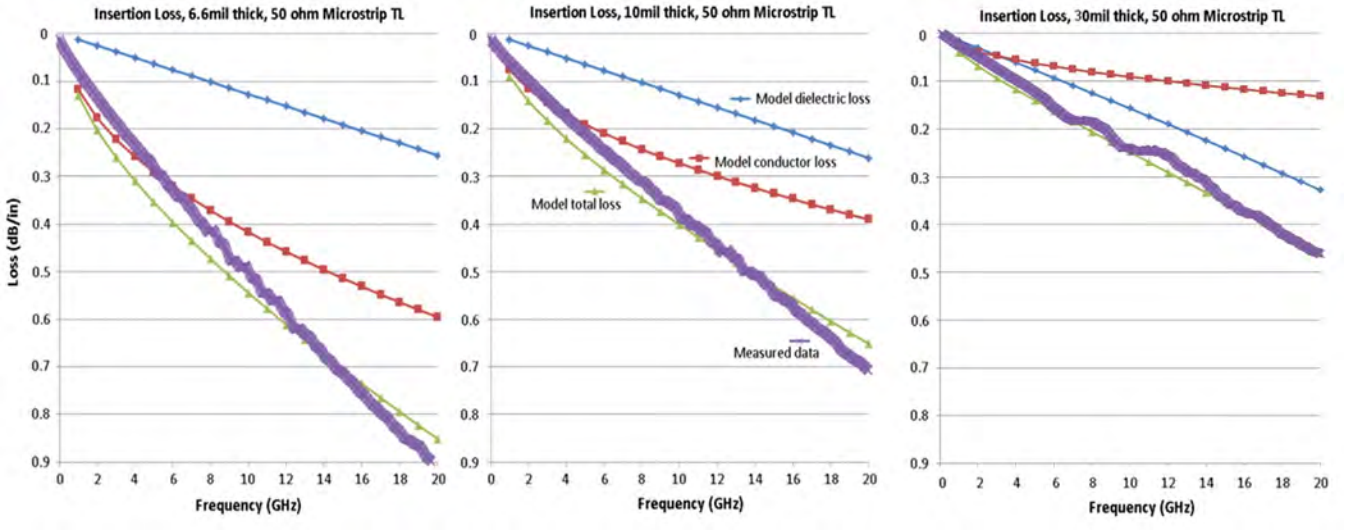

Figure 1: These plots of insertion loss versus frequency compare three sets of circuits on three different thicknesses of the same circuit material.

cuit's conductor loss. Thinner circuits will be more impacted by lossy plated finishes than thicker circuits (Figure 2).

Figure 2 compares 50-Ω microstrip transmission-line circuits, using the same substrate at different thicknesses and comparing insertion loss of a circuit with bare copper conductor and the same circuit with ENIG finish. As the plots of loss versus frequency show, the difference in insertion loss between bare copper and ENIG is more dramatic for a thin circuit (an 8-mil substrate) than for a thick circuit (20-mil substrate). The ENIG finish results in additional conductor loss and a thinner circuit is more affected by differences in conductor loss than a thicker circuit.

Loss Mechanisms for Plated Finishes

Considering a cross-sectional view of a microstrip transmission-line circuit, the concentration of electric fields and the current density between the bottom edge of the signal conductor and the top edge of the ground plane can be readily visualized (Figure 3). The opposing metal faces of the top copper (signal) plane and the bottom copper (ground) plane have a concentration of electric fields. However, there is also a high concentration of electric fields and current density to be found at the edges of the signal conductor as can be seen in Figure 3.

The depiction of a microstrip transmission-line conductor in Figure 3 is not meant to be overly rigorous, although great care was taken to show the appropriate field lines and current density for a typical microstrip transmission line circuit. It is a general representation of the electric fields and current density for a microstrip circuit; the left sidewall and right sidewall of the signal conductor will have higher current density near the base of the conductor. Final plated finishes cannot penetrate the signal conductor and are typically applied to the three edges of the conductor other than the copper-substrate interface. The additional conductor loss from a lossy plated finish is typically an edge effect, coming from the left and right conductor sidewalls with the plated finish. Conductor losses will increase due to the finish having lower conductivity than copper. This lossy edge effect is accumulative: a circuit with short length will suffer minimal additional loss due to the plated finish while a circuit with long length will exhibit significantly higher loss as a function of length.

The increased loss due to final plated finish is also dependent on circuit design, and a grounded coplanar waveguide (GCPW) transmission-line circuit will suffer more loss due to a plated finish than a microstrip circuit with a plated finish. The GCPW configuration results in more of the lossy finish being part of the signal path than in a microstrip circuit (Figure 4).

As with the image in Figure 3 for microstrip, the drawing of GCPW in Figure 4 may not be exact, but much diligence was applied to show

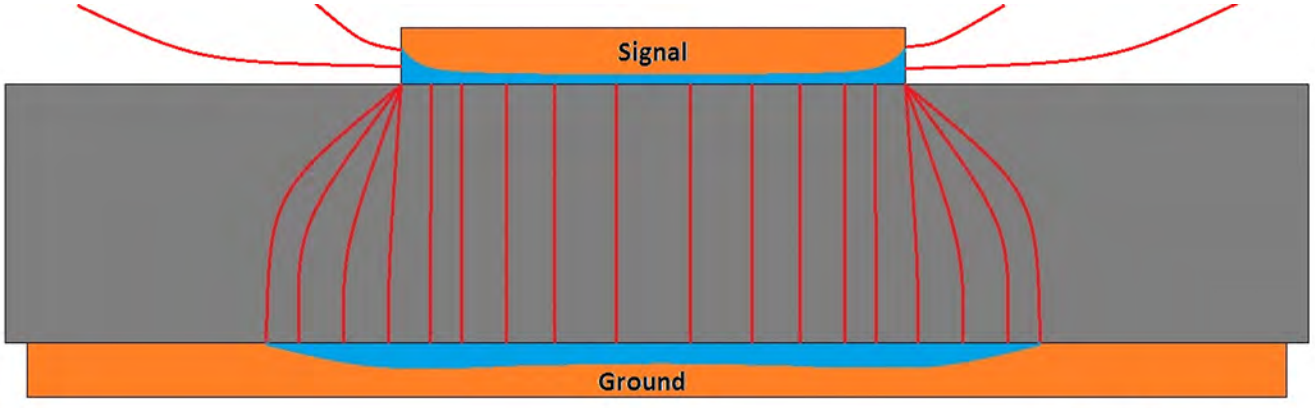

Figure 3: This cross-sectional view of a microstrip transmission line circuit shows the electric fields and current density between the two metal faces of the PCB.

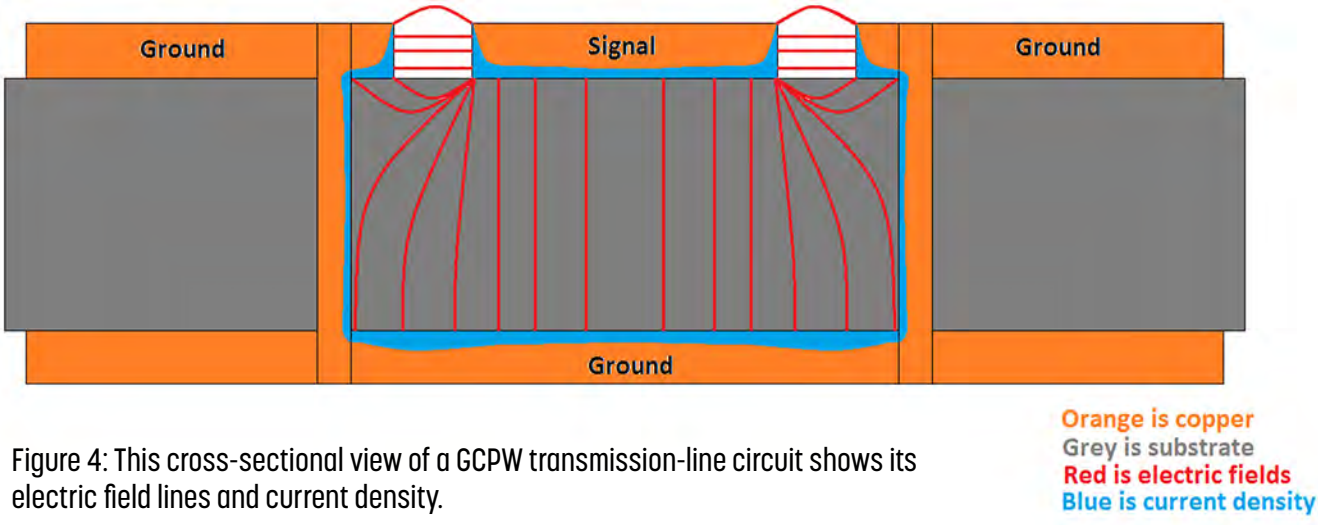

Figure 4: This cross-sectional view of a GCPW transmission-line circuit shows its electric field lines and current density.

the appropriate electric field and current density configurations for a typical GCPW circuit. As was the case for the microstrip circuit, the final plated finish cannot impact the copper-substrate interface; however, the coplanar sidewalls will be plated with the finish. In the case of a GCPW circuit, there are four sidewalls where the plated finish will be applied, and significant current density occurs in those areas. A lossy plated finish will cause a more significant increase in conductor loss for a GCPW circuit as compared to a circuit based on microstrip transmission lines.

The GCPW circuit in Figure 4 is considered tightly coupled. This means that the space between the ground-signal-ground (GSG) plane on the coplanar layer is relatively small compared to the substrate thickness. If a loosely coupled GCPW (with large GSG coplanar spacing) was drawn, there would be much less current density along the sidewalls. The impact of final plated finish on this circuit configuration would be considerably less than on a tightly coupled GCPW circuit configuration. In general, the loss of a microstrip transmission-line circuit will be less impacted by the final plated finish than a GCPW circuit, as illustrated by Figure 5.

As can be seen in Figure 5, the increase in insertion loss due to a lossy (ENIG) plated fin-

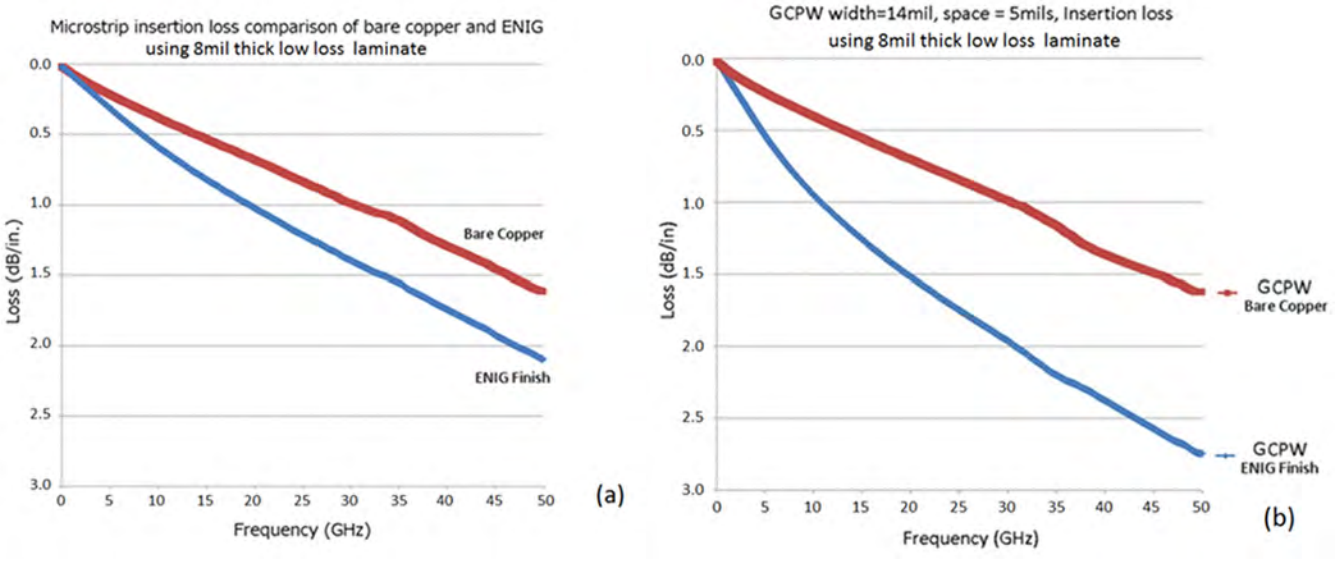

Figure 5: For the same circuit laminate, the differences in loss can be seen for bare copper conductors and conductors with ENIG plated finish for (a) microstrip and (b) GCPW circuits.

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ish is greater for a GCPW circuit than for a microstrip circuit. In this case, the comparison is between a tightly coupled GCPW circuit (Figure 5b) and a microstrip circuit (Figure 5a). If the comparison had been between a loosely coupled GCPW circuit and microstrip, the results would have been somewhere between the microstrip and GCPW responses shown in Figure 5. A very loosely coupled GCPW circuit can behave very much like a microstrip circuit in terms of loss behavior.

Trying to account for the losses of a final plated finish as a function of frequency can be rather difficult because many loss mechanisms for these circuits are frequency-dependent as is the loss impact of the final plated finish. One frequency related issue is skin depth and that is how much of the conductor will be used by the RF current at a given frequency. When the frequency increases, the skin depth will get thinner, and that will naturally cause more conductor loss. Skin depth is also impacted by the conductivity of the metal conductor. Copper has excellent conductivity, but most final plated finishes have less conductivity than copper. The following function gives a reference to the skin depth formula and the conductivity of different metals:

Skin depth (δ)

$$\delta = \sqrt{\frac{1}{\pi f \mu \sigma}}$$

f = frequency
μ = permeability
σ = conductivity

Approximate conductivities (σ) of metals

Silver	6.301×10^7 S/m
Copper	5.817×10^7 S/m
Gold	4.520×10^7 S/m
Nickel	1.500×10^7 S/m
Tin	0.870×10^7 S/m
Solder	0.700×10^7 S/m

As the skin depth formula suggests, an increase in frequency results in a decrease in skin depth. A decrease in conductivity will cause an increase in skin depth. Finally, an increase in permeability results in a decrease in skin depth.

The effects of a lossy plated finish on the composite conductivity of the sidewalls of a signal conductor can be difficult to estimate, especially considering changes with increased frequency and how skin depth decreases with frequency. But it can be remembered that at lower frequencies (less than 500 MHz), the composite conductivity at the sidewalls of a signal conductor is a combination of copper-nickel-gold. As frequency increases, the skin depth will decrease, and the composite conductivity at the sidewalls will be a combination of nickel-gold. At much higher frequencies with very thin skin depth, the composite conductivity will be dominated by the gold. So far, the plated finishes for PCBs have been referred to as "lossy plated finishes" because they increase the loss of a copper conductor beyond its unplated performance. A plated finish that would not be considered lossy would be one that does not increase the loss of a copper conductor, such as immersion silver (with conductivity higher than copper).

For ENIG, nickel exhibits about one-quarter the conductivity of copper; since it is less conductive than copper, it will suffer greater conductor losses. The presence of nickel can cause a doubling or even a tripling effect on conductor losses. First, the nickel will cause more conductor loss due to its conductivity being less than copper. Second, with increased skin depth in nickel, the RF current will use more nickel, resulting in greater loss. A third factor has to do with the ferromagnetic nature of nickel and how it will normally suffer some amount of magnetic loss in combination with the other two loss components.

The potential ferromagnetic effects of nickel are difficult to quantify. In general, ferromagnetic properties change dramatically with frequency, from lower microwave frequencies to a few GHz. The higher relative permeability (μr) of nickel will result in some decrease in skin depth, somewhat offsetting the increased skin depth of nickel due to poor conductivity. In addition to these complications, the nickel used in ENIG is not pure nickel but is typically doped with phosphorous. Suppliers of ENIG will adjust different characteristics of the nickel alloy for different reasons. Due to the many issues associated with the magnetic properties of nickel, it can make a correlation between models (for simulation) and measurements less accurate.

Measured Results and Discussion

I have conducted several studies on plated finishes over the past few years with the cooperation of two ENIG suppliers and a PCB fabricator. Before reviewing some of the measurement results of those studies, it is helpful to detail the test vehicle used for the measurements. The preferred test vehicle consisted of a 50-Ω microstrip transmission-line circuit on a selected circuit material as the device under test (DUT) with measurements made per the differential length method [3].

The microstrip circuits were fabricated on thin, low-loss substrates with smooth copper. These material characteristics help minimize dielectric losses while exaggerating any conductor loss differences among different plated finishes used on the DUTs. It should be noted that all copper foils used in the PCB industry have some normal surface roughness variations which result in variations in conductor losses from one circuit to another when using the same circuit laminate. Copper surface roughness and its variation will impact insertion loss and the phase response of a circuit [4]. By using smooth rolled copper, the surface roughness variations were minimized as much as possible.

Microstrip circuits were used in the measurements instead of GCPW even though GCPW might have been thought to be more sensitive to loss differences among circuits with different plated finishes. But studies have shown [1, 5] that GCPW suffers more performance variability due to PCB fabrication processing and normal copper plating thickness variations, and conductor trapezoidal effects can cause significant loss variations from circuit-to-circuit when using the same substrate, making it more difficult to separate the effects of final plated finishes from the fabricated circuits. Microstrip circuits are less impacted by PCB fabrication variables, making microstrip a more suitable choice of transmission-line format to study the effects of plated finishes on circuit loss.

Initial studies were performed using 50-Ω microstrip transmission-line circuits based on 5-mil, ceramic-filled PTFE laminate with a Dk of 2.94, Df of 0.0012, and rolled copper with an average surface roughness of 0.35-µm RMS. Multiple plated finishes were used with a summary of the insertion-loss curves for the different finishes provided in Figure 6.

The reference (top) curve in Figure 6 is for a microstrip circuit with bare copper. As can be seen, the loss curves for the OSP and immersion silver finish are approximately equivalent to the circuit with bare copper. Other studies have shown similar results, where OSP and immersion silver do not significantly influence the insertion loss. The ENIG plated finish shows the greatest amount of loss, and these results have been confirmed in other studies of this nature. The electroless nickel electroless palladium immersion gold (ENEPIG) plated finish has less loss at higher frequencies; however, at lower frequencies, this finish and ENIG exhibit similar effects on loss. Other studies have confirmed this trend. A plausible reason for the frequency-loss relationship is that ENEPIG finishes use thinner nickel than ENIG finishes.

Since conductivity is a composite effect and changes with frequency, there is a range of

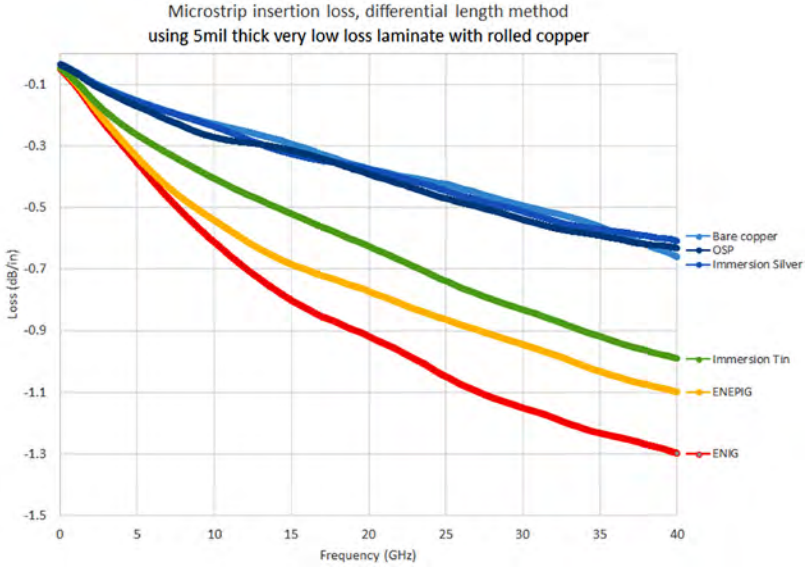
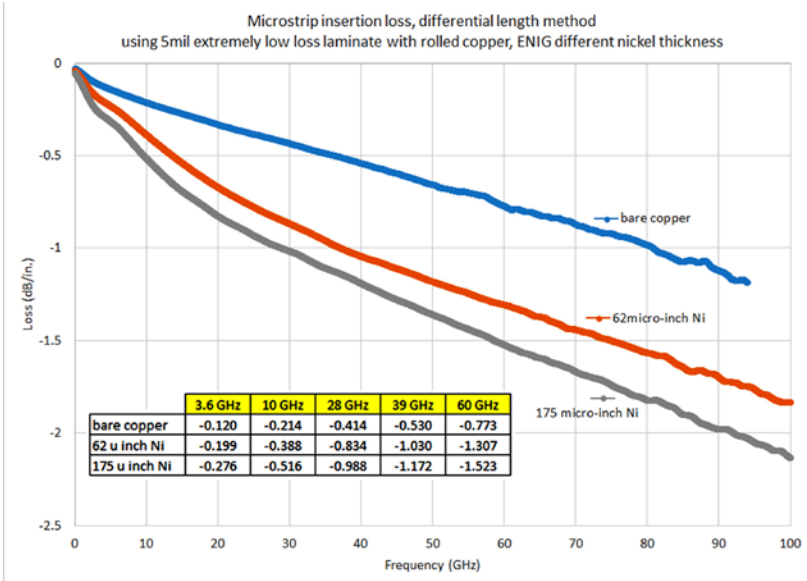


Figure 6: Insertion loss curves of multiple final plated finishes using the microstrip differential length method.

frequencies where the composite conductivity of ENEPIG and ENIG are basically the same due to the skin depth using about the same amount of copper-nickel-gold, or at slightly higher frequencies, the same thickness of nickel-gold. Once the frequency increases to the point where the nickel is contributing less for ENEPIG, the nickel will still be a significant factor for the ENIG because ENIG has thicker nickel.

As Figure 6 shows, finishes with ENEPIG and ENIG both have more loss than a finish with immersion tin. Reviewing the metal conductivities presented earlier, it would be expected that immersion tin would have greater loss than these other finishes. The insertion-loss relationship between ENEPIG and ENIG has been confirmed by other studies; it has been assumed that the added magnetic losses of nickel used with ENEPIG and ENIG finishes makes them lossier than an immersion-tin finish. However, it is possible that the loss differences are related to thickness and/or skin-depth effects; immersion tin is extremely thin and skin-depth effects would not be significant until much higher frequencies.



	3.6 GHz	10 GHz	28 GHz	39 GHz	60 GHz
bare copper	-0.120	-0.214	-0.414	-0.530	-0.773
62 u inch Ni	-0.199	-0.388	-0.834	-1.030	-1.307
175 u inch Ni	-0.276	-0.516	-0.988	-1.172	-1.523

Figure 7: These insertion loss curves compare microstrip circuits with bare copper to microstrip circuits with ENIG finishes with different nickel thicknesses.

Microstrip circuits have other components of loss which result in increased loss with increasing frequency, and these loss components can make it difficult to separate the effects of immersion tin on loss. Some of the loss components not related to plated finish include the fact that the Df of the substrate material increases with increasing frequency and the radiation loss increases and the electric fields condense more at higher frequencies. Condensed fields will cause a narrower ground return path which increases the conductor loss, adding to the total loss behavior of the circuit at higher frequencies.

The impact of variations within the plated finish on loss must also be considered. The nickel layers used in ENIG finishes can suffer large circuit-to-circuit thickness variations: it is possible for the nickel layer to vary from 50 to 250 µin. (1.27 to 6.35 µm). A study targeted finishes with low and high nickel thickness and everything else remaining the same. The test vehicle remained the same for this study, but a different material was used with low loss and rolled copper. The material was a ceramic-filled PTFE laminate with a Dk of 3.0, Df of 0.001, and copper surface roughness of 0.35 µm.

The microstrip insertion loss curves shown in Figure 7 depict significant differences in insertion loss with variations in nickel thickness that is within the thickness range which could occur from one circuit build to another. ENIG is typically not used above 60 GHz; however, as can be seen in the table of Figure 7, there are significant differences in loss at lower frequencies as well.

As designers transition from applications operating at microwave frequencies to circuits at higher, millimeter-wave frequencies, they often consider the use of GCPW to replace microstrip transmission lines. The benefits of using GCPW at millimeter-wave frequencies include less dispersion, less radiation, and the possibility to suppress spurious wave propagation modes more effectively. However, there are several PCB-related issues which impact the consistency of RF performance for GCPW

circuits. With this in mind, it seemed prudent to show the same information in Figure 7 but using a test vehicle that is a GCPW transmission-line circuit. This comparison is shown in Figure 8.

Several things should be considered when comparing Figures 7 and 8. Different Y-axis scales are used for insertion loss in the two graphs, and the curves for GCPW depict much greater losses than the curves for microstrip. Another item of interest is the differences between the insertion loss for circuits with thin nickel compared to circuits with thicker nickel.

Plated thickness variations for immersion tin will have less impact on variations in insertion loss because the immersion tin is very thin. It is applied by means of a self-limiting process and the typical immersion tin thickness is about 47 µin. (1.2 µm). With such a thin layer, the tin does not have a significant influence on the composite copper-tin conductivity at the sidewalls of the microstrip signal conductor until about 20 GHz.

Figure 9 used the same test vehicle as used for Figures 7 and 8 but with different thicknesses of immersion tin. As is evident, the immersion tin thickness variation has some impact on microstrip insertion loss at higher frequencies, but not as much as the impact of ENIG finishes with varying thicknesses of nickel as can be seen in figure 7. The tin thickness for these circuits was 24 µin. (0.6 µm) for the thin tin plating and 79 µin. (2.0 µm) for the circuits with thick tin plating.

Another study has looked at an electroless palladium immersion gold (EPIG) plating which does not have nickel. The same test vehicle was used for the other finishes, and EPIG plated finish shows an improvement in insertion loss compared to the other finishes. However, a different substrate material was used in the EPIG study, a material with a Dk of 3.2, Df of 0.0033, and copper surface roughness of 0.9 µm RMS. With this material, the bare copper circuit will have more losses than in previous studies in which bare copper circuits have been mentioned. However, the comparison be-

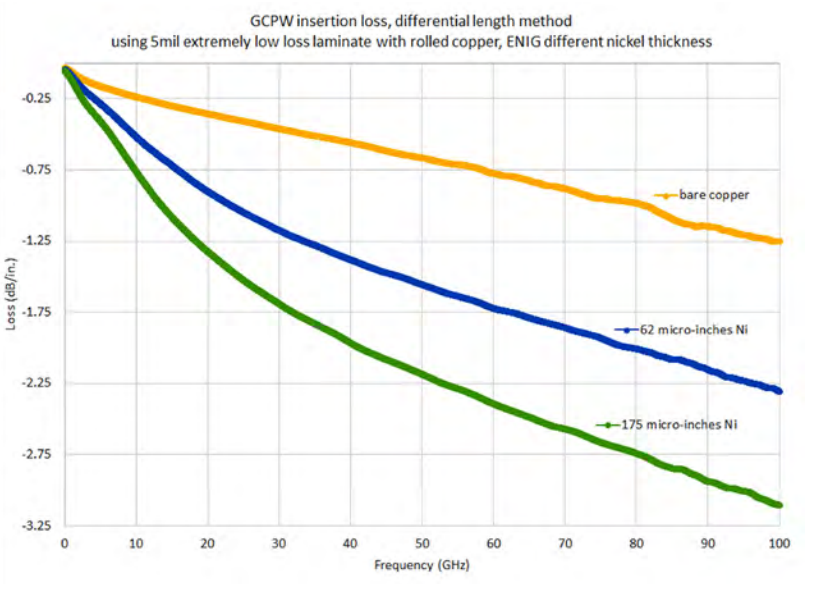


Figure 8: These insertion loss curves for GCPW transmission-line circuits compare circuits with bare copper conductors to circuits with ENIG finishes with different nickel thicknesses.

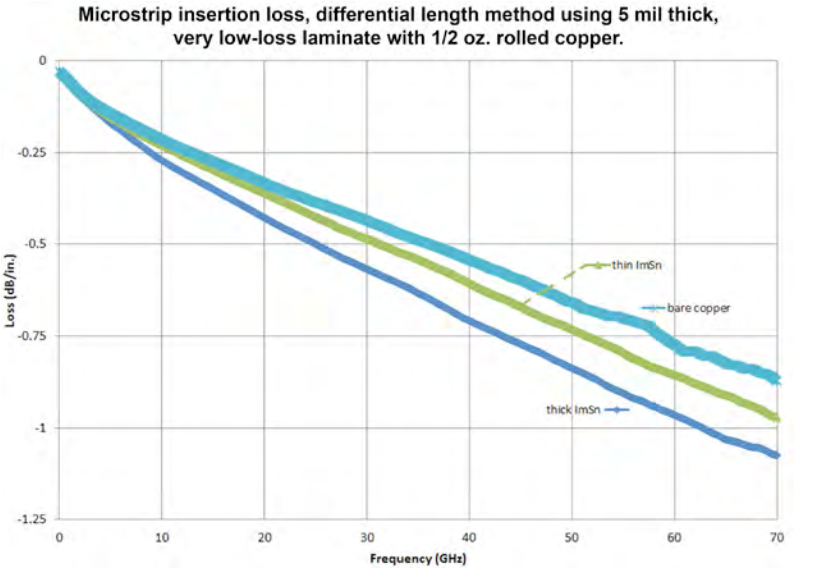


Figure 9: The microstrip insertion loss curves compare circuits with bare copper conductors to circuits with immersion tin (ImSn) finishes with different tin thicknesses.

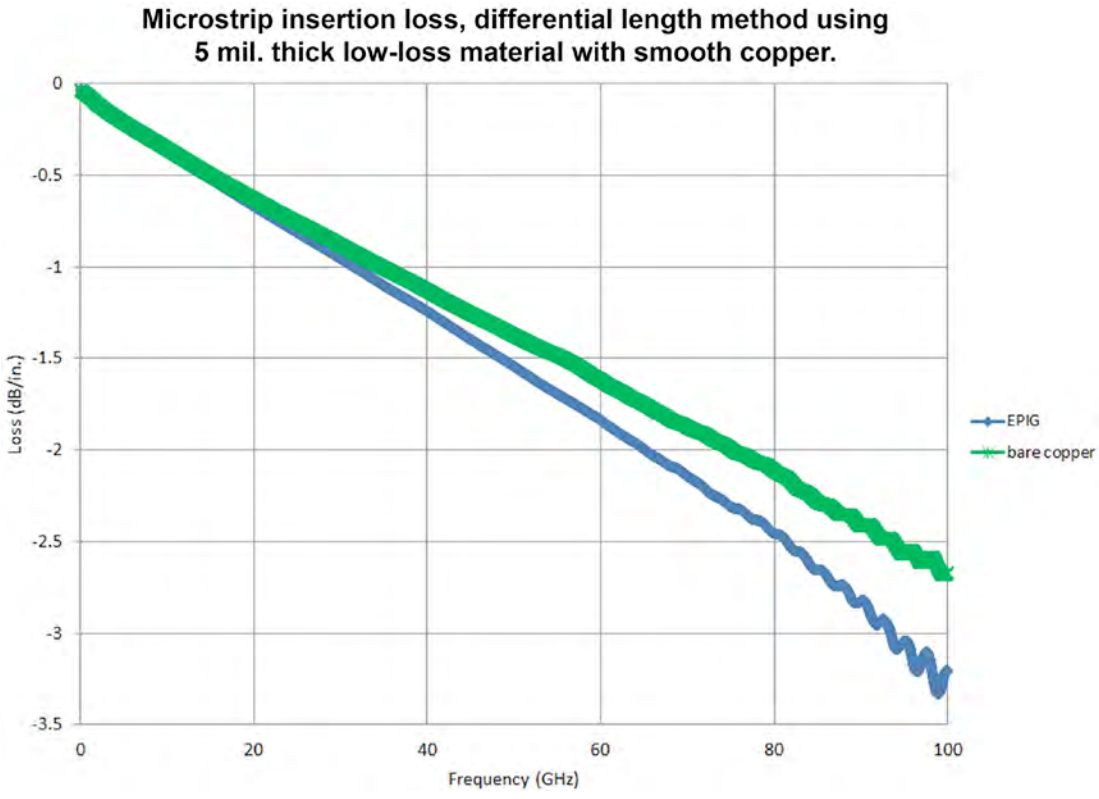


Figure 10: These curves show the insertion loss of microstrip circuits using a gold final plated finish which does not have nickel.

tween the bare copper circuit and the EPIG finish is still noteworthy (Figure 10).

Since the test vehicle was using a slightly higher loss material and the copper surface was slightly rougher, the bare copper circuit loss in this study of EPIG finish is higher than for the bare copper shown in previous studies in this article. The copper was a low-profile, reverse-treated copper with minimal surface roughness variation. The insertion loss difference between the bare copper circuit and the EPIG circuit has the least difference of any other gold finishes shown in this study.

Even though this article has focused on insertion loss, it seemed judicious to mention a slightly different issue which can be important in material characterization and is related to the plated finish study. Microstrip ring resonators are commonly used to characterize materials at microwave and sometimes millimeter-wave frequencies; however, if ENIG is applied, the nickel variation can have an impact on the capacitance in the gap coupled area of a ring resonator. An evaluation was done, in parallel to the evaluation shown in Figures 7 and 8, where gap coupled ring resonators were evaluated using the same sheet of laminate to make the circuits, and it was found that nickel thickness variation does impact the resonant frequency of a ring resonator. This means if this structure was used to calculate the Dk of the material, which is common, the extracted Dk would be altered due to nickel thickness variation. A summary of this information can be seen in Figure 11.

The materials used to make the microstrip ring resonators were made from the same large sheet of material cut in half. One half panel had circuits made with thinner nickel for the ENIG, and the other half panel had circuits made with thicker nickel for ENIG. The nickel variation makes some small differences in the loss, Q, and bandwidth, but makes a pretty significant difference in the center frequency and the extracted Dk. By using the same large sheet of material, that will minimize material differences there is yet an extracted Dk difference of 0.023. The ring resonators having dif-

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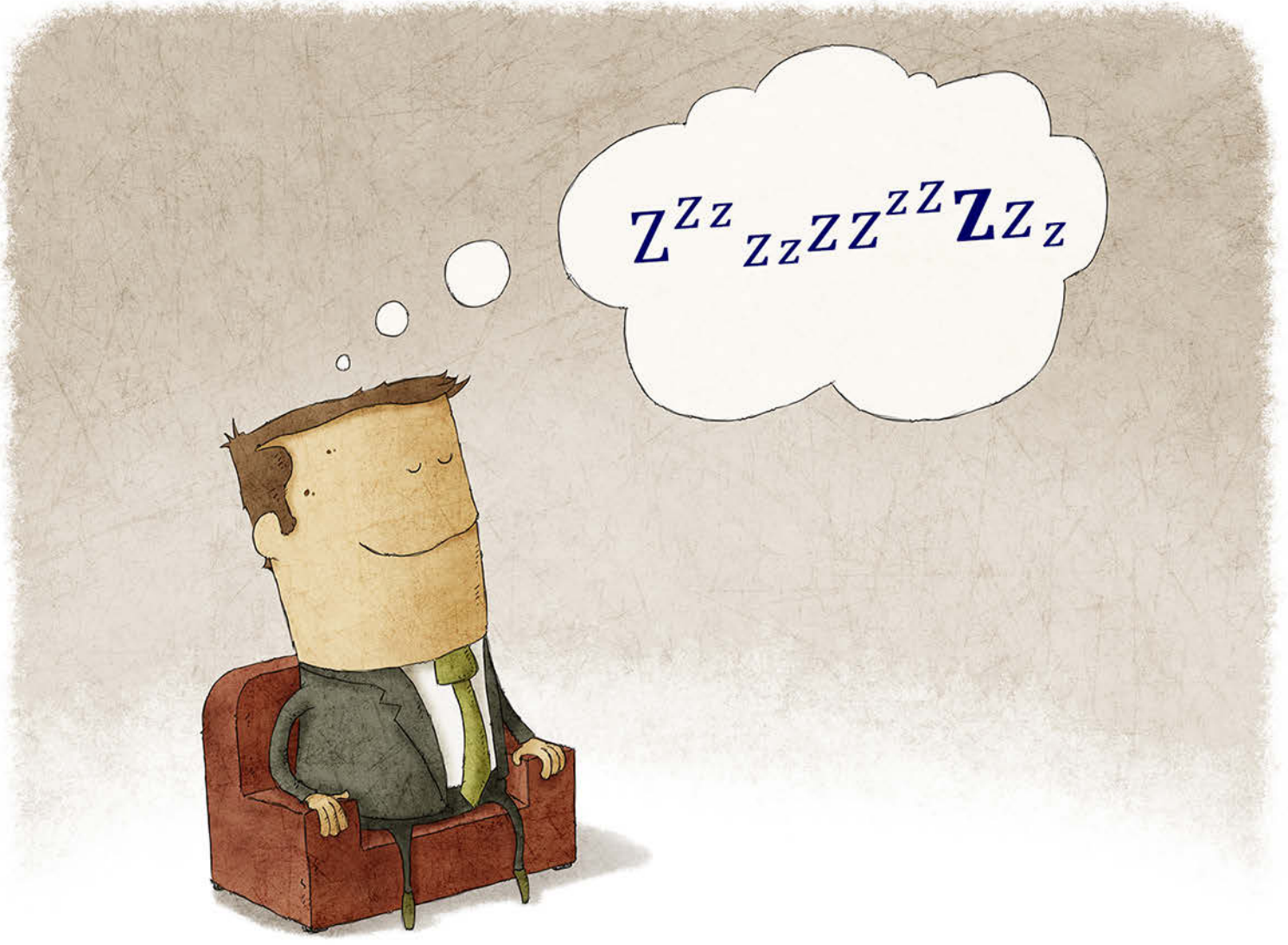

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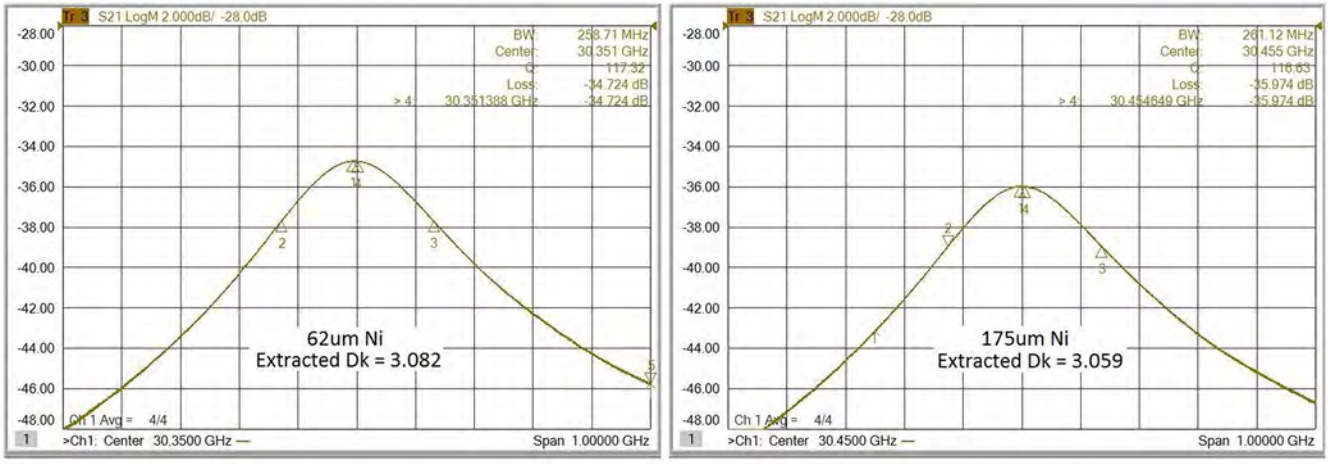

Figure 11: Comparison of Dk extraction using microstrip ring resonator with ENIG plating having different nickel thickness.

ferent nickel thickness were measured for circuit dimension differences and nothing significant found. The thicker nickel will impact the capacitance in the gap coupled area. Thicker nickel decreases the conductivity in the gap coupled area, which is seen as a decrease in capacitance, that will shift the frequency up which relates to a lower extracted Dk. Additionally, if Df was extracted, then the ring resonator with the thicker nickel would report a falsely higher Df than the ring resonator using the thinner nickel, again, while using the same sheet of material.

Conclusions

Conductor loss is one of the components of PCB insertion loss and can be impacted by the final plated finish used for a circuit. There can be a substantial increase in insertion loss due to the final plated finish. This study explored the effects of the final plated finish on circuit insertion loss. Thin substrates were used to achieve good resolution among the different plated finishes used with the test vehicle, although if a thicker circuit was used, the magnitude of the curves shown in this study would be less. As a reference, that effect (of substrate thickness) can be seen in Figure 2. Designers should consider the effects of final plated finish on insertion loss when predicting and simulating circuit performance during the design phase of circuit development and choose final plated finishes according to performance requirements. **DESIGN007**

Acknowledgments

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John Coonrod is technical marketing manager at Rogers Corporation and an I-Connect007 columnist.

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FLEX007
A SPECIAL DESIGN007 MAGAZINE SECTION

Flex Standards in Flux

What the Flex?

by Andy Shaughnessy, I-CONNECT007

We're heading into fall, but the electronics industry is still smoking hot. Most of the players in our industry still haven't seen many real effects of the trade war. And as we head into the holiday season, we can expect the electronics manufacturing—and the overall economy—to keep chugging along.

Flexible circuits are continuing to find their way into almost every type of device—for reliability reasons or just because rigid boards simply won't fit into the shrinking form factors of today's handheld devices. With the advent of 5G and IoT leading PCB designers further into the realm of RF and microwave, flex standards are more critical than ever, especially for rigid board designers who have been forced into designing flexible circuits.

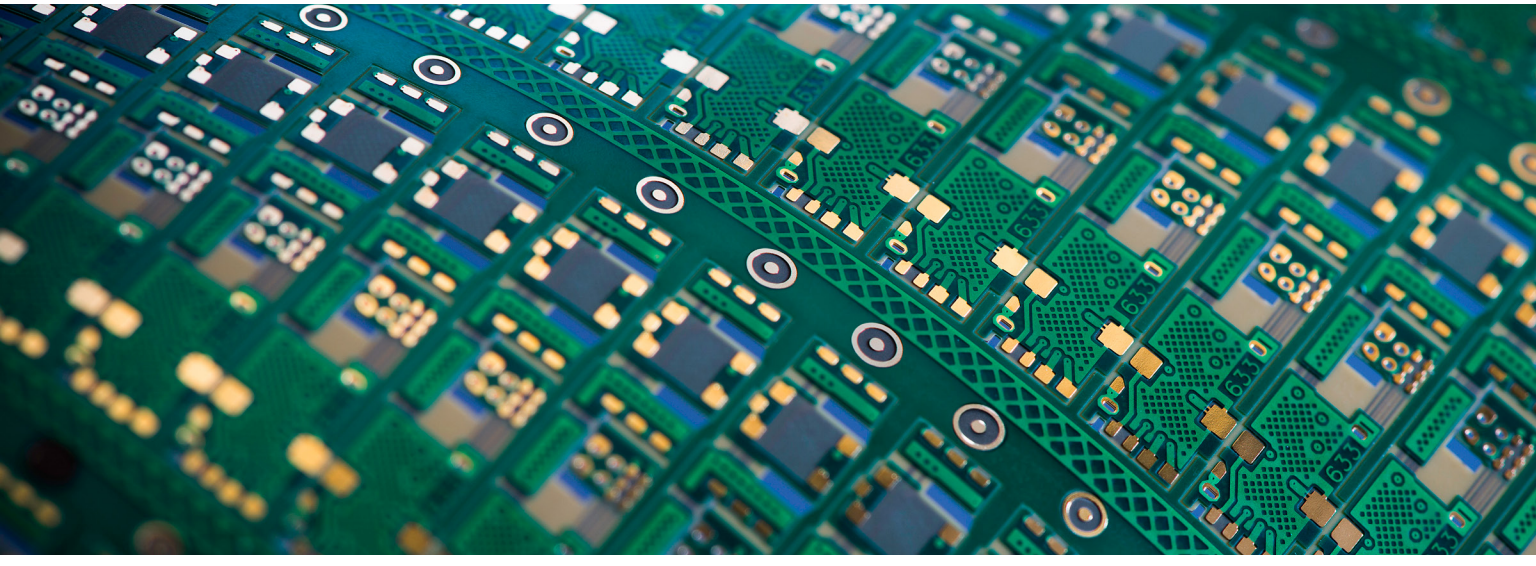
We launch this month's Flex007 section with an interview with Nick Koop of TTM Technologies, the vice-chair of IPC's Flexible Circuits Committee and co-chair of the 6013 Subcommittee. He discusses some of the updated versions of flex standards that are soon to be released—such as IPC-2223 and IPC-6013—and why these committee members must perform a balancing act by incorporating new processes as quickly as possible, but only after they've proven their viability.

Next, columnist Joe Fjelstad of Verdant Electronics breaks down the various types of standards related to flex and rigid circuits and addresses why it's no exaggeration to say that standards are what hold the electronics industry together, in his column "Standards: An Industrial-strength Glue." Then, Dominique K. Numakura of DKN Research follows up with a look at a simple process hailing from Taiwan that creates "monocoque" 3D printed circuits by printing silver-based traces on thermoplastic sheets. The result isn't exactly a rigid or flexible circuit, but a totally novel idea. Expect to hear much more about this in the upcoming months.

Show Time

Show season is upon us, and if you're new to designing flexible and rigid-flex circuits, you're in luck. In the next few months, there are a couple of opportunities to learn about flex design from industry veterans who have been there and done that.

Mark Finstad of Flexible Circuit Technologies will join Nick Koop to teach their popular half-day



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course "Ask the Flexperts—Flexible Circuit Design Through Test With Lessons Learned" at PCB West in Santa Clara, California. This is a class that is built on audience participation. Vern Solberg of Solberg Technical Consulting will present his half-day class "Design and Assembly Process Principles for High-Density Flexible and Rigid-Flex Circuits" at SMTA International in Rosemont, Illinois. And at AltiumLive PCB Design Summit in San Diego, California, Flex007 columnist Tara Dunn of Omni PCB will teach her class "Flex and Rigid-Flex: Real-World Use Case Studies."

But if you can't make it to trade shows this fall, don't worry. We'll be covering the industry from San Diego to Munich and bringing you the flex information you need. See you next month. **FLEX007**

Andy Shaughnessy is managing editor of *Design007 Magazine*. He has been covering PCB design for 19 years. He can be reached by clicking here.

Earwear and Watches Expected to Drive Wearables Market at a CAGR of 7.9%

The market for wearable devices is on track to reach global shipments of 222.9 million units in 2019, growing to 302.3 million units in 2023 with a compound annual growth rate (CAGR) of 7.9%, according to a new forecast from International Data Corporation (IDC) Worldwide Quarterly Wearable Device Tracker. Behind that growth is the propagation of smartwatches and ear-worn devices, which will account for more than 70% of all wearable shipments by 2023.

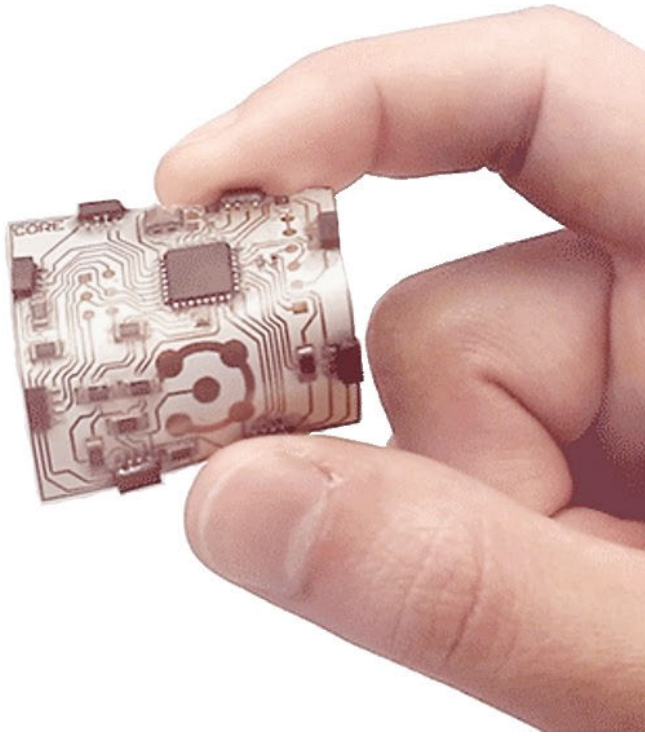
"Not only is the market diversifying in terms of form factors, but it is also diversifying in terms of connectivity and distribution," said Jitesh Ubrani, research manager for IDC's Mobile Device Trackers. "Among all watches, close to half will have the ability to connect to a cellular network by 2023 as consumers along with enterprises and healthcare look to free the watch from the phone and as TELCOs push forward subsidies or financing options for watches with cellular service."

"In addition to the proliferation of devices is the expansion of wearables use cases," said Ramon T. Llamas, research director for IDC's Wearables team. "Smartwatches, as always, will still tell you the time but will move deeper into health and fitness and connect with multiple applications and systems both at work and within the home. Ear-worn devices, while still centered on providing audio, will nudge into other areas like language translation, smart assistant deployment, and coaching."

Watches are forecast to grow from 91.8 million units in 2019 to 131.6 million in 2023 with a five-year CAGR of 9.4%. Apple is expected to lead the way, capturing 25.9% share of all watches in 2023. Beyond Apple will be a variety of brands running different operating systems, including Android, WearOS, Tizen, and others. Not only will smartwatches serve as health and fitness tools for consumers and enterprises, but other use cases, such as parental tracking of their kids' location or the incorporation of watches into the smart home ecosystem, are also expected to proliferate.

Ear-worn devices are expected to grow from 72 million units in 2019 to 105.3 million in 2023. While many of these will be used as the front end to smart assistants or be used to track health-related metrics, IDC also expects brands to push forth added benefits, such as allowing consumers the ability to cope with hearing loss or giving users the ability to fine-tune their daily auditory experience.

Wristbands will see flat shipment growth throughout the 2019-2013 forecast with a CAGR of 0.3%. Chinese brands, such as Xiaomi and Huawei, have been leading this market, and more than half of all wristbands are expected to be shipped in China. Meanwhile, mature markets, such as North America and Western Europe, are expected to see declining shipments as users transition to smartwatches. (Source: IDC)



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Nick Koop

Flex Standards Update With Nick Koop

Feature Interview by Andy Shaughnessy
FLEX007

This month, I interviewed Nick Koop—director of flex technology at TTM Technologies, a veteran "flex guy" and instructor, and a leader of several IPC flex standards committees. Nick provides an update for the committees he's involved with and discusses some of the challenges that he sees as more designers enter the world of flex.

Andy Shaughnessy: Nick, tell us a little about your background and your work with flex and rigid-flex circuits at TTM.

Nick Koop: I've worked in the flex and rigid-flex world since 1985 where my roles have ranged from process engineer to design engineer to general manager of a factory. And I've been with TTM since 2013. It has been a great experience working with such a wide range of customers and programs, solving problems that lead to success for our customers.

Shaughnessy: You're the vice-chair of the Flexible Circuits Committee and co-chair of the 6013 Subcommittee. Give us some updates on the flex committees.

Koop: All of the flex specifications are being reviewed on an ongoing basis. We are close to releasing new versions of IPC-2223 and IPC-6013. They will include more information on microvias, finished copper thickness, and other member-requested updates. I would expect that to happen by early 2020. The supporting material specifications and test methods are also under review. In addition, there is work happening on the T-50 Terms and Definitions Guideline, which is in the middle of a substantial update. So, there is a lot happening on all fronts.

Shaughnessy: We talk to a lot of rigid board designers who are being forced into flex design. Usually, they start with flex standards, and then hopefully, they will call a flex board shop. What advice would you give any rigid folks moving into the flex world?

Koop: We are also seeing dramatic growth in flex use driven by several factors; space, weight, reliability, and cost being some of the most com-

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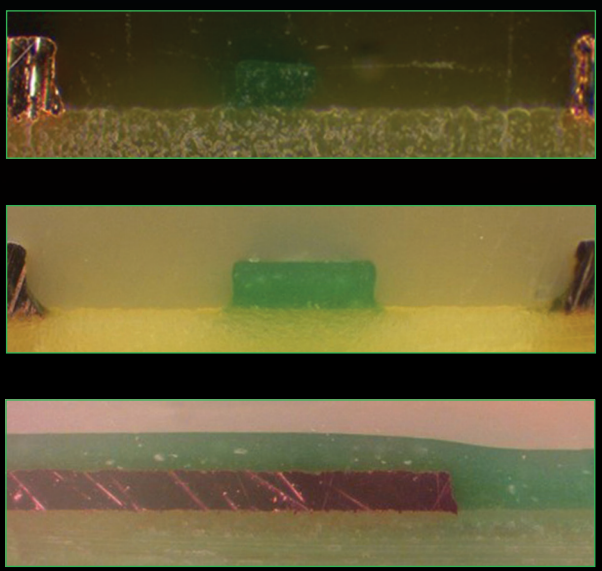

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mon. Flex provides a lot of advantages over a rigid board and discrete wiring. My initial advice would be to gain an understanding of the similarities and differences. The key differences are unique materials and a variation in material movement, which can impact alignment.

I often hear comments like, "But you did it on one of our rigid boards…" This is when we talk about how to adjust the design for flex. And as you noted, talking with a flex fabricator is key. Attending flex seminars can give you a quick head start as well. A good designer understands that flexibility brings advantages, but also some design considerations.

Shaughnessy: Some design teams say that they almost always exceed certain flex standard recommendations, such as for bend radii in 2223. Do you think IPC flex standards will ever "catch up" to where the industry is now or is that not necessarily the standards organization's role?

Koop: Bend radii is probably one of the most commonly exceeded guidelines. The guidelines are intentionally set very conservatively to stimulate a discussion. Every situation is different; in some cases, a very tight bend radius can be very successful, but it may lead to problems in others. Understanding the environment and specifics of the design are key.

I don't know that the standards will ever "catch up," as you mentioned. While we do our best, technology continues to advance quickly. As early adopters, some designers are willing to take risks, but others are not. As new techniques are more widely adopted, they get incorporated into a specification. It is a balancing act, as we do not want to "legitimize" a questionable technique by including it in the specification before we know it is viable. Sometimes, the fabricators are developing process techniques to accommodate designer's needs; some work out, but others do not. We want to see these processes reaching acceptable manufacturing or production readiness levels, and then we incorporate them.

There are times where we hear comments to the effect of, "That will never be done," which tends to be a red flag for me. We are often proven wrong by someone who does it successfully! Overall, I think IPC has done a good job of being a "fast follower" with specifications. Members can be quite anxious to get a new revision out to reflect new needs, and IPC itself is pushing hard to turn revisions more quickly to keep up with the pace of change.

Shaughnessy: You're also a flex instructor at various industry conferences. What are some of the biggest challenges that your attendees are facing with flex and rigid-flex?

Koop: The biggest challenges we see are packaging and component related. As products get smaller and denser, making boards thin enough, and being able to bend or fold them into the final assembly can be a challenge. This leads to making material selections to make the parts very thin and flexible.

BGAs are another challenge. The sub-0.8-mm BGAs are driving smaller pads and holes and microvias. Large form factor BGAs have so many I/O points, which creates big challenges for designers to fan out the entire pattern. This often drives very fine lines and extra circuit layers.

Shaughnessy: Is there anything you'd like to add?

Koop: This is a great industry to be a part of. We get to see all of the latest and greatest technology advances because circuit boards are what makes them happen. I would also encourage more young engineers to get involved. We are seeing the exit of many very experienced and talented designers as they retire. New designers are taking their places but have not had the opportunity to learn from their senior counterparts.

The key to success for new designers will be to reach out both internally and externally to learn. Take advantage of the opportunities to mimic other successes and avoid previous failures. There are lots of resources out there to help.

Shaughnessy: I appreciate your time. Thank you.

Koop: Thanks, Andy. **FLEX007**

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Here are 10 questions to ask yourself when testing the strength of your current partnership with your vendor.

EPTE Newsletter: JPCA Show 2019, Part 4 ▶

Manufacturing a custom product with 100+ processing steps can be tricky enough, but when you add in a highly complex set of design attributes, pour engineering resources into defining the process, and verify that it is repeatable and reliable, that comes with a certain sense of pride and satisfaction.

Flex Talk: When You Do Everything Right and Something Still Goes Wrong ▶

This industry is full of tales describing the work and effort needed to overcome fabrication hurdles to produce a complex design. Tara Dunn shares a case study of one of those types of designs.

Development of Flexible Hybrid Electronics ▶

This article presents a hybrid manufacturing process to manufacture FHE systems with a two-layer interconnect structure utilizing screen printing of silver conductive ink, filled microvias to connect ink traces at the different layers, and use of the traditional reflow process to attach the semiconductor chips to the printed substrates.

Mentor Tools: Optimized for Flex and Rigid-flex Design ▶

With the launch of the new Flex007 section in Design007 Magazine, we asked David Wiens, product marketing manager with Mentor, a Siemens business, to tell us about their tools' flex and rigid-flex design capabilities.

IPC E-Textiles 2019 to Address Real World of Applications for Multiple Markets ▶

IPC E-Textiles 2019—a two-day technical education workshop for innovators, technologists and OEMs/brands to learn about the latest in the converging industries of textiles and electronics—will feature 14 technical presentations, tours of the Drexel Center for functional fabrics, a special interactive session, and an IPC D-70 E-Textiles Committee Standards meeting.

AT&S Stays on Track: Another Important Growth Investment Initiated ▶

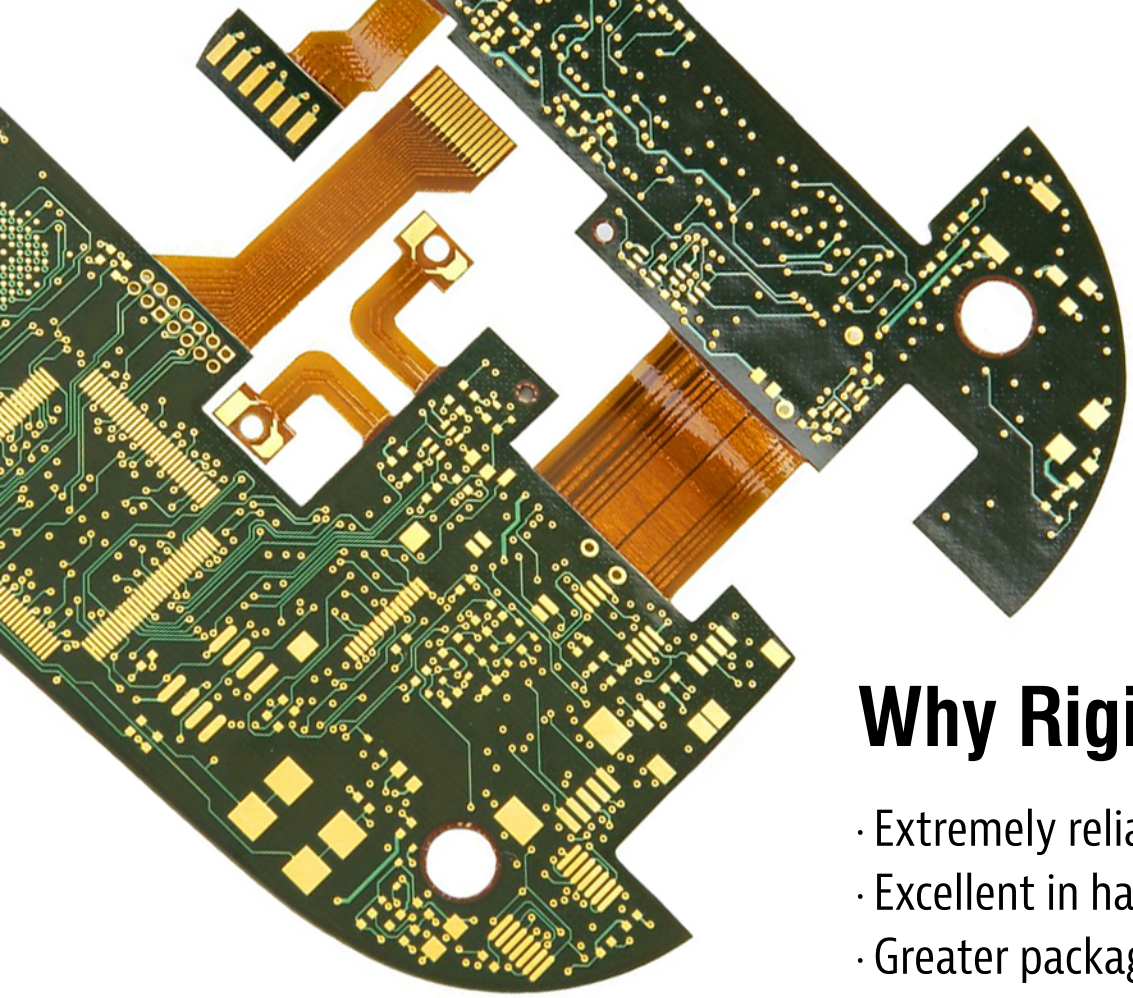
In the first quarter of 2019/20, AT&S recorded a stable development overall, achieving revenue at €222.7 million.

TPCA Releases New Version of Technology Roadmap of Taiwan PCB Industry ▶

The 2019 Technology Roadmap reflects the technology leadership of Taiwan's PCB industry and the gap between Taiwan and its competitive countries. It also enables the industry to review the gap between the technology level among its members and the entire industry.

Ventec Expands Thermal Interface Materials Range ▶

Ventec International Group Co. Ltd has added two new thermally conductive, thin isolation foil materials to its range of thermal interface materials (TIM) under its distribution agreement with EMI Thermal.



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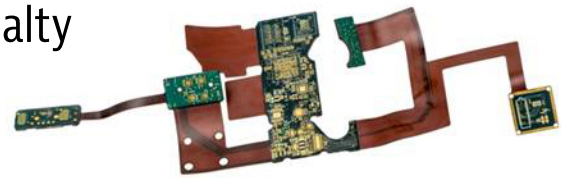

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Standards: An Industrial-strength Glue

Flexible Thinking

by Joe Fjelstad, VERDANT ELECTRONICS

Standards are frequently viewed as cumbersome nuisances and impediments to progress by those pressing for rapid change. The process of writing, getting approval, and promulgating standards can be arduous and frustrating. It has a lot of similarities to the creation and passage of laws in various government bodies in that there are many opinions and interested parties who engage in the process to make sure that it results in a product that does not damage or favor one solution or party over another.

People involved in the generation and passage of legislation have equated it to sausage making. As you can imagine, it's not a very pretty process; however, when done right, can result in a palatable product that presumably can be enjoyed by the greatest number of consumers. You would think that at some point, there would be enough laws. Yet with the changing dynamics of society, there is a near-constant flow of new laws to address our changing needs, and that is no less true for standards for our industry as technology evolves and changes.

And just as there are many government bodies around the globe, there are hundreds of standards bodies around the world with sometimes conflicting missions in terms of the generation and guidance in the enforcement of industrial standards. In this regard, just as laws help to hold societies together, standards serve the vital purpose of holding industries together. They are an industrial-strength glue (if you can tolerate a little tongue-in-cheek metaphor) in that they hold the industry together.

Four Types of Standards

In the world of electronics manufacturing, there is a myriad of standards, covering virtually every aspect of the ubiquitous products our industry

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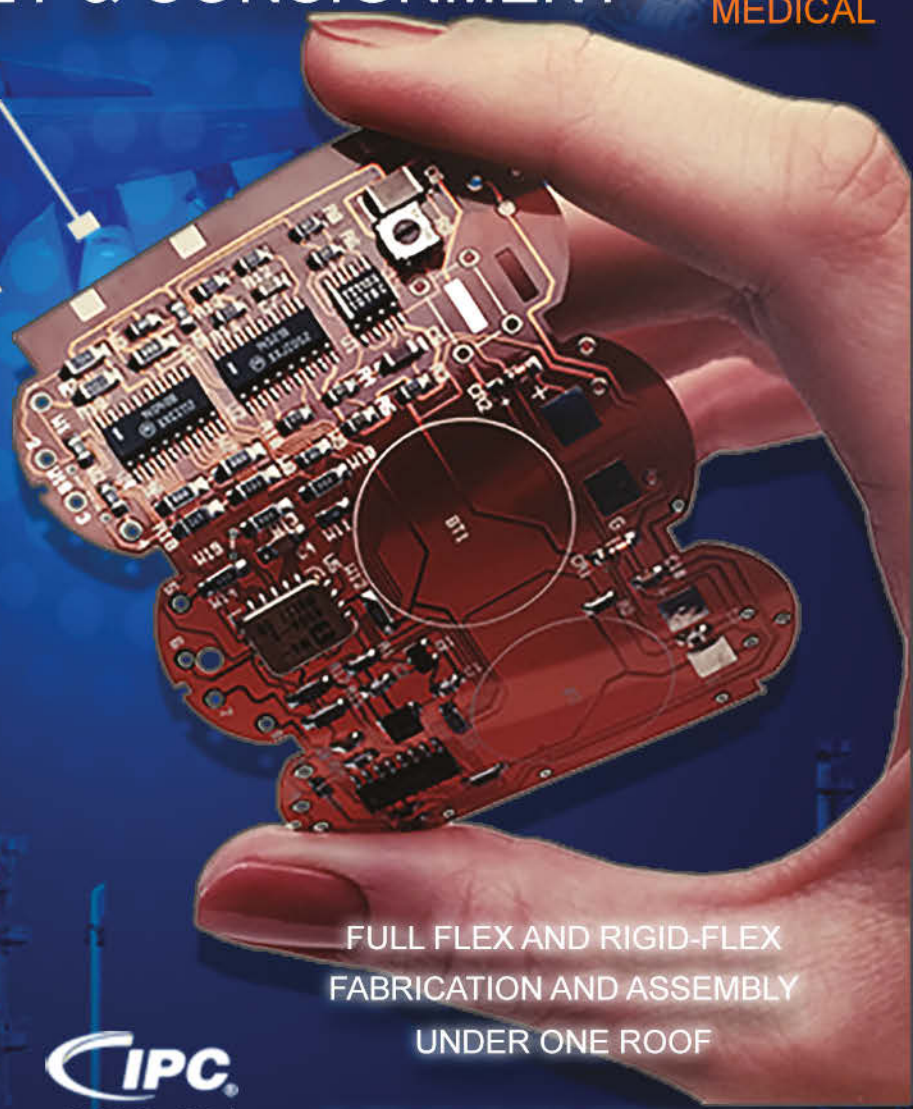

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makes. These standards cover everything from raw materials to production processes and the inspection and test of the numerous discrete and individual products that make up the final product acquired by the consumer or user. Standards come in a number of forms, and here are the four main types.

1. De Jure Standards

You are probably the most familiar with de jure standards, which are standards according to an agreed-upon process. This is often by a committee that is endorsed by a formal standards organization, such as IPC, IEEE, IEC, JEDEC, UL, or JEITA. Each organization ratifies its standards through its own official procedures and gives the standard its stamp of approval.

2. De Facto Standards

De facto standards have come to exist based on commonly accepted practices and have been adopted widely by an industry and its customers much like common law. De facto standards are created when a critical mass likes them well enough to collectively use them. They are often codified and turned into de jure standards by standards bodies when the value is seen or finally recognized (something arguably still in the works for concepts like the Occam process and SAFE technology). Emerging markets often evolve using de facto standards in the early stages because normal standards organizations are wedded to incumbent markets and technologies and typically focus only on the here and now.

3. Proprietary Standards

Proprietary standards are typically owned by a single company and often backed by special intellectual property ownership rights and/or trade secrets such that only the company or its designated customers and partners are allowed to use them. This creates a monopoly for the company, but it also restricts the growth of the underlying technology. However, under some circumstances, it can prove quite lucrative, as one well-known smartphone company has shown.

4. Open-Proprietary Standards

The final types of standards are the so-called open-proprietary standards, which are also developed and owned by a single company(such as Verdant Electronics and its Occam process), but the company will usually allow anyone to use them to help grow the market for the benefit of all. Because the company spent time and money researching and developing the technology covered by their proprietary and patented efforts, there is frequently a licensing fee involved. To be successful, it is generally agreed that the fee is reasonable and non-discriminatory (RAND, in the parlance of the industry).

The company that is openly licensing its proprietary standard is required to maintain and support the standard under license. This also requires time and effort. Such licenses often have grant-back clauses that require any improvements to the basic standard to be included for the benefit of all other licensees that require resources. Again, there may be an agreement that there be some fair and reasonable compensation for the company that made improvements. This is one way to make sure that progress continues for the benefit of all involved.

Standards Approval

Of these four types of standards, formal or de jure standards are clearly the most common. To generate such standards is neither fast nor easy, as it involves the cooperation of many companies that are frequent competitors. However, the participants understand the meaning of the adage, "A rising tide lifts all

boats," and that the standard will serve that purpose by addressing the prospective problems each company might face if the standard did not exist.

Standards bodies that oversee such developments generally serve members by forming committees to work out the details. The task can be arduous and take months or even years to come to a consensus by a vote among users of the standard. To gain approval could require anything from a simple majority to a 75% or even greater approval level before gaining acceptance. Interestingly—or perhaps, unfortunately—because of the rapid changes being experienced by the electronics industry on a seemingly daily basis, the approval of a standard is often marked by the beginning of a revision process to capture those changes.

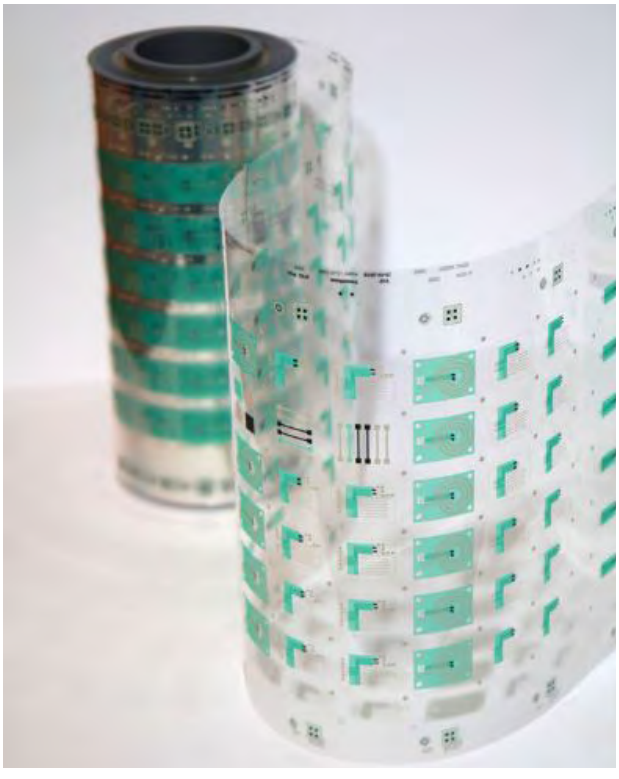
Summary

Standards (and guidelines) are important documents that are required by almost every industry imaginable to maintain a sense of order and ensure that the quality, performance, safety, and reliability of products meet customer expectations. Metaphorically, standards truly are industrial-strength glue. **FLEX007**

Joe Fjelstad is founder and CEO of Verdant Electronics and an international authority and innovator in the field of electronic interconnection and packaging technologies with more than 150 patents issued or pending. To read past columns or contact Fjelstad, click here.

Wearable Sensors Detect What's in Your Sweat

A team of scientists at the University of California, Berkeley, is developing wearable skin sensors that can detect what's in your sweat. They hope that one day, monitoring perspiration could bypass the need for more invasive procedures, such as blood draws, and provide real-time updates on health problems, such as dehydration or fatigue.



According to Ali Javey, a professor of electrical engineering and computer science at UC Berkeley and senior author on the paper, the goal of the project is "'decoding" sweat composition. They used the sensors to monitor the sweat rate and electrolytes and metabolites in sweat. The new sensors contain a spiraling microscopic tube, or microfluidic, that wicks sweat from the skin. By tracking how fast the sweat moves through the microfluidic, the sensors can report how much a person is sweating, or their sweat rate.

Javey and his team worked with researchers at the VTT Technical Research Center of Finland to develop a way to quickly manufacture the sensor patches in a roll-to-roll processing technique similar to screen printing. To better understand what sweat can say about the real-time health of the human body, the researchers first placed the sweat sensors on different spots on volunteers' bodies and measured their sweat rates and the sodium and potassium levels in their sweat while they rode on an exercise bike.

They found that local sweat rate could indicate the body's overall liquid loss during exercise, meaning that tracking sweat rate might be a way to give athletes a heads up when they may be pushing themselves too hard.

(Source: UC Berkeley)

Monocoque Printed Circuits: An Update

EPTE Newsletter

by Dominique K. Numakura, DKN Research LLC

Editor's Note: Dominique Numakura first covered monocoque printed circuits in a column from May 2019.

What would you think if electronic circuits could be built directly on a polyethylene terephthalate (PET) package of strawberries and birthday cakes? It was a dream for electronics engineers to draw 3D circuits directly on the surface of the housing or packages of products. The idea behind molded interconnect device (MIDs) was created about 30 years ago to satisfy this dream. Several new processes, such as laser engraving and inkjet printing, have been proposed to build electronic circuits on 3D-structured objects. Unfortunately, no one was very successful with it as a popular circuit technology because of the technical and economic difficulties.

Wiring with flexible circuits could be a practical solution. Nowadays, most mobile device manufacturers are consuming huge amounts of thin, flexible circuits to attach on the surface of the housing in limited spaces. However, the cost of flexible circuits and assembling them is another headache for device manufacturers because they are not negligible in the whole cost of the devices.

Now, a new idea has been created in Taiwan to build 3D-printed circuits. It looks like an egg of Columbus, and the manufacturing process is very simple. Firstly, a silver-based thick-film circuit is printed on a thermoplastic sheet, such as PET. The baking temperature of the circuit must be lower than the melting temperature. It depends on the capability of the circuit manufacturer, but double-layer circuits with via holes are available (Figure 1).

The second step is to warm the whole circuit and put it in the forming die set. Under an appropriate temperature and pressure, the plastic

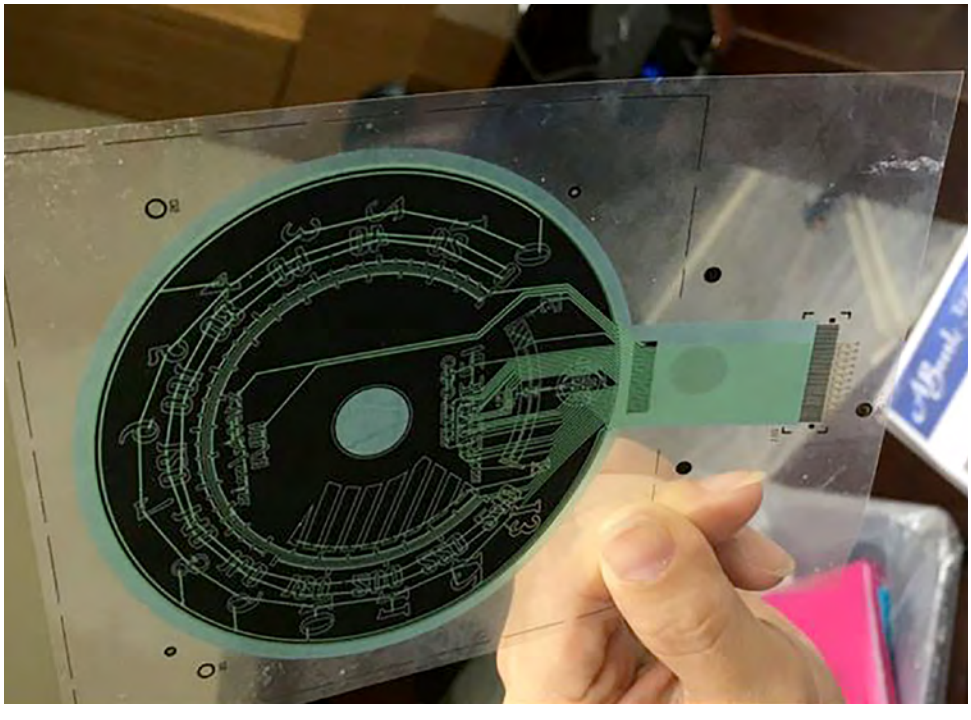
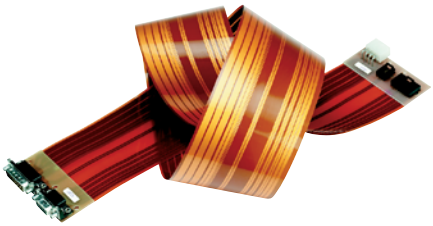


Figure 1: After the circuit is printed.



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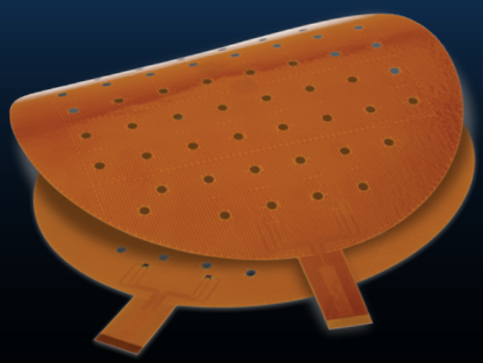

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Figure 2: After thermal forming.

sheet with the silver circuit is formed to desired 3D shape (Figure 2). Lastly, the formed circuit is removed from the die and cooled down. Then, a 3D-printed circuit is ready for the assembling process.

Unfortunately, this soldering process is not available for thermally formed circuits. Instead, a low-temperature SMT process with conductive glue was introduced for the mounting of the components.

Conductive ink could be the key to this technology. As the conductors have serious tensile stress during the thermal formation, the conductor materials have to have appropriate elasticity to avoid cracking. Certainly, standard copper foils cannot withstand the mechanical stress during thermal forming. Silver inks prepared for the thick film could be practical candidates as the conductor of the circuits.

However, the physical properties are not enough as the conductor of the formed circuits; therefore, a new version of the conductive ink has been developed. The new silver ink has higher elasticity and can withstand mechanical stress during thermal formation. But conductor patterns have several limitations, especially in the bent area. Design guides, such as the minimum radius of the corners, should be provided by manufacturers.

As it is still in the development stage, there are not many examples. Right now, most manufacturers are using PET as the substrate material. The trials are showing very promising performances. Manufacturers have been expanding the substrate materials to acrylic resins and polycarbonate resins, which are popular as packaging materials for food. More materials will be tried out in the next few quarters.

Formed printed circuits are not categorized as rigid printed circuits nor flexible circuits. We are calling them monocoque printed circuits because the formed structure works as both the framing of the packages and the substrate of the circuits. This new circuit technology needs a new category. Originally, "monocoque" was a French word used in the design of automobiles. Monocoque structure means a specific construction in which the body also works for framing to support the weight. **FLEX007**

Dominique K. Numakura is the managing director of DKN Research LLC. To read past columns or contact Numakura, click here.

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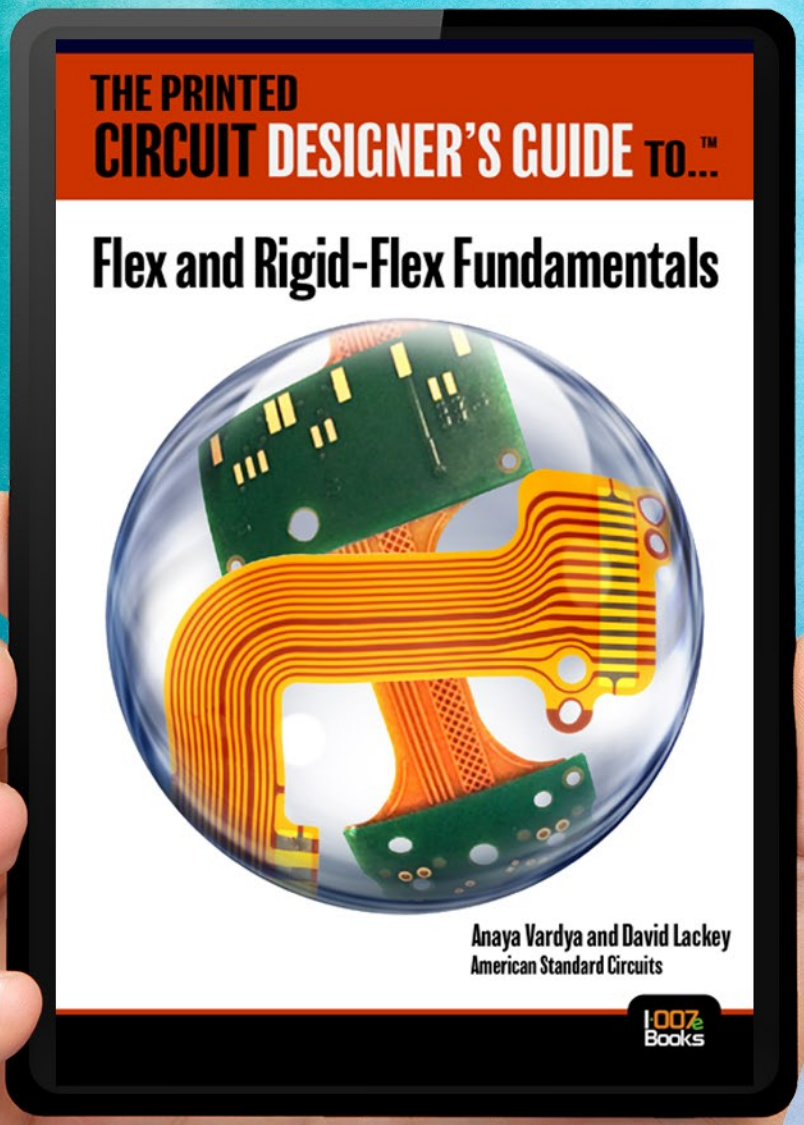

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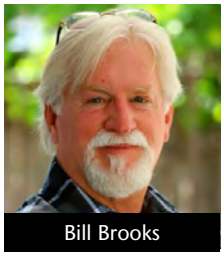
1 Beyond Design: Stackup Planning, Part 5 ▶

Barry Olney describes the traditional stackup structures that use a combination of signal and power/ground planes. But to achieve the next level in stackup design, one needs to not only consider the placement of signal and plane layers in the stackup, but also visualize the electromagnetic fields that propagate the signals through the substrate.

2 Bill Brooks on Teaching PCB Design at Palomar College ▶


Bill Brooks

Bill Brooks of Nordson ASYMTEK recently spoke with the I-Connect007 editorial team about his history in design and his time as a PCB design instructor, the curriculum he developed and taught, and various techniques that might be enacted today to better educate the designers of tomorrow.

3 IPC High-reliability Forum and Microvia Summit Review, Part II ▶

The Microvia Summit provided updates on the work of members of the IPC V-TSL-MVIA Weak Interface Microvia Failures Technology Solutions Subcommittee and opportunities to learn about latest developments in methods to reveal and explain the presence of latent defects, identify causes and cures, and be able to consistently and confidently supply reliable products.

4 Development of Flexible Hybrid Electronics ▶

This article will present a hybrid manufacturing process to manufacture FHE systems with a two-layer interconnect structure utilizing screen printing of silver conductive ink, filled microvias to connect ink traces at the different layers, and use of the traditional reflow process to attach the semiconductor chips to the printed substrates.

5 Denny Fritz: The Difference Between Quality and Reliability ▸


Denny Fritz

Andy Shaughnessy speaks with industry veteran Denny Fritz about the relationship between quality and reliability—two terms that are unequal but often used interchangeably. We also discuss the current state of lead-free solders in the U.S. military and defense market as well as the microvia reliability issues Denny focused on at IPC's High-Reliability Forum and Microvia Summit.

6 The Impact of Inductance on Impedance of Decoupling Capacitors ▸

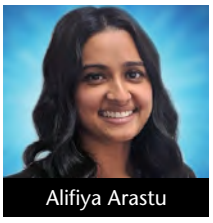

Chang Fei Yee

This article discusses the impact of interconnection inductance on the impedance of the decoupling capacitor, which influences the power integrity of the PCB. The investigation is performed with 3DEM simulation by varying the trace length and height of stitching vias that connect the decoupling capacitor across the power rail and ground.

7 Connect the Dots: Five Best Practices to Ensure Manufacturability ▸

When you send your design for manufacturing, your partner does not know what type of device the board will be part of nor the conditions in which it will have to perform. Be sure your board can tolerate thermal stress or solder joints risk breaking and damaging components.

8 Fresh PCB Concepts: Qualities of Medically Applied PCBs ▸


Alifiya Arastu

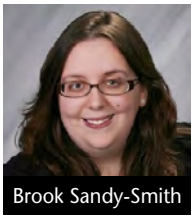
In this inaugural column from NCAB Group, Alifiya Arastu discusses details of PCBs used in medical applications, highlighting some of the differences in terms of demands and how the design must be handled.

9 Focusing on Surface Sensitivity for Reliability ▸

Elizabeth Kidd & Alex Bien

Customer Applications Scientist Elizabeth Kidd and Sales Engineer Alex Bien, both of BTG Labs, discuss with Andy Shaughnessy their presentation at the IPC-High-Reliability Forum and Microvia Summit on the challenges of working with highly sensitive surfaces, such as the risk of contamination. They also talked about the various surface characterization techniques that BTG Labs uses to identify such contaminants.

10 IPC Reliability Forum Wrap-up With Brook Sandy-Smith ▸


Brook Sandy-Smith

At the IPC High-Reliability Forum and Microvia Summit, the speakers and panelists focused on a variety of topics, but one issue that kept popping up was the failure of some microvias on military and aerospace PCBs. Fortunately, some smart technologists are focusing on determining the cause of these via failures. Andy Shaughnessy asked Brook Sandy-Smith, IPC's technical education program manager, for a quick wrap-up of this event.

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- Manage the IPC, military, Bellcore and customer specs
- Measure quality performance
- Employee training, certification, and performance reviews
- Plan & coordinate audits to ensure controls are in place and maintained to continuously improve product yield
- Set QA compliance objectives
- Other duties as assigned

REQUIREMENTS:

- 5 years managerial experience in PCB operation
- Technical degree or equivalent experience
- In-depth understanding of IPC specifications, military specifications and Bellcore requirements
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- Able to analyze non-conformance of product
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- Compile feasibility studies for bringing new products and emerging technologies through manufacturing to the marketplace
- Provide product and manufacturing support
- Provide product quality control and support
- Must comply with all OSHA and company workplace safety requirements at all times
- Participate in multifunctional teams

Required Education/Experience:

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Working Conditions:

- Chemical laboratory environment
- Occasional weekend or overtime work
- Travel may be required

apply now

Assistant Department Manager, Operations, Carson City, NV

This is an entry-level professional management trainee position. Upon completion of a 1-2-year apprenticeship, this position will be elevated to facility/operations manager. Primary functions during training: shadow incumbent staff managers to learn and understand the operations and personnel of the operations department. This position will train and learn, develop, implement, and coordinate strategies related directly to the manufacture of Taiyo products. Additionally, this position will be learning all about the facility, environment, and health and safety functions. Eventually, this position will be responsible for the administration, security and maintenance of the facility and warehouse

Required Experience/Education:

- 4-year college degree in industrial engineering or another similar science discipline combined with work experience in ink or coatings manufacturing
- Ability to read, analyze, and interpret common scientific and technical journals, financial reports, and legal documents
- Ability to respond to inquiries or complaints from customers, regulatory agencies, or members of the business community
- Ability to develop and implement goals, objectives, and strategies
- Ability to effectively present information to top management, public groups, and/or boards of directors
- Ability to apply principles of logical or scientific thinking to a wide range of intellectual and practical problems
- Knowledge of governmental safety, environmental, transportation regulations/laws

Preferred Skills/Experience:

- Bilingual (Japanese/English)
- Toyota Production System (TPS)

Working Conditions:

- Occasional weekend or overtime work

See complete job listing for more information.

apply now

Career Opportunities

eptac

TRAIN. WORK SMARTER. SUCCEED.

Become a Certified IPC Master Instructor

Opportunities are available in Canada, New England, California, and Chicago. If you love teaching people, choosing the classes and times you want to work, and basically being your own boss, this may be the career for you. EPTAC Corporation is the leading provider of electronics training and IPC certification and we are looking for instructors that have a passion for working with people to develop their skills and knowledge. If you have a background in electronics manufacturing and enthusiasm for education, drop us a line or send us your resume. We would love to chat with you. Ability to travel required. IPC-7711/7721 or IPC-A-620 CIT certification a big plus.

Qualifications and skills

- A love of teaching and enthusiasm to help others learn
- Background in electronics manufacturing
- Soldering and/or electronics/cable assembly experience
- IPC certification a plus, but will certify the right candidate

Benefits

- Ability to operate from home. No required in-office schedule
- Flexible schedule. Control your own schedule
- IRA retirement matching contributions after one year of service
- Training and certifications provided and maintained by EPTAC

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INSULECTRO

Technical Account Manager Chicago/Minneapolis

Insulectro, the largest national distributor of printed circuit board materials, is seeking a talented sales superstar for a Technical Account Manager role based out of either our Chicago or Minneapolis office. This role will focus on maintaining the existing customer base and developing new business within the assigned territory in both the printed circuit board and printed electronics industries. We are looking for the perfect fit of education, experience, and attitude that matches our company culture and enhances the service level to our customers.

Qualifications:

- A self-motivated business professional who is driven to succeed with a minimum of 3 years outside sales experience in the PCB or PE industry
- Proven sales/business development record
- Excellent communication and interpersonal skills
- OEM and electronic assembly experience is a plus

We offer:

- Competitive salary and commission plan with a comprehensive benefits package
- A fun, high-energy company with an entrepreneurial spirit
- A great group of people to work with!

apply now

Career Opportunities

Analyst Programmer, Hong Kong

We believe in caring about our people because they are our greatest asset. CML works with multicultural stakeholders daily to achieve more and bring them the best solutions. That's why we continuously invest in optimizing our culture and focus on providing our team with opportunities to develop their skills (e.g., through professional coaching to achieve their highest potential).

The analyst programmer will assist the IT and ERP manager in Hong Kong to support the company's BI systems, ERP systems, and other related IT-landscape applications.

In addition, this post will participate in system development projects and provide support including, but not limited to, user requirement collection and analysis, user training, system documentation, system support and maintenance, enhancement, and programming.

- Develop and enhance related IT systems and applications
- Prepare functional specifications
- Transfer the relevant business and interface processes into IT systems and other applications to get a maximum automation degree and prepare all required business reports
- Conduct function testing and prepare documentation
- Manage help desk/hotline service

CML is a leading provider of printed circuit boards. We develop tailor-made sourcing and manufacturing solutions for our customers worldwide with strong partnerships and reliable connections.

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APCT, Printed Circuit Board Solutions: Opportunities Await

APCT, a leading manufacturer of printed circuit boards, has experienced rapid growth over the past year and has multiple opportunities for highly skilled individuals looking to join a progressive and growing company. APCT is always eager to speak with professionals who understand the value of hard work, quality craftsmanship, and being part of a culture that not only serves the customer but one another.

APCT currently has opportunities in Santa Clara, CA; Orange County, CA; Anaheim, CA; Wallingford, CT; and Austin, TX. Positions available range from manufacturing to quality control, sales, and finance.

We invite you to read about APCT at APCT.com and encourage you to understand our core values of passion, commitment, and trust. If you can embrace these principles and what they entail, then you may be a great match to join our team! Peruse the opportunities by clicking the link below.

Thank you, and we look forward to hearing from you soon.

apply now

Career Opportunities

TAIYO AMERICA

Technical Sales Engineer

San Jose, CA, USA

The technical sales engineer will perform technical audits and help customers troubleshoot and optimize their solder mask process, prepare and deliver technical presentations explaining products or services to customers and prospective customers, collaborate with sales teams to understand customer requirements and provide sales support, secure and renew orders and arrange delivery, and help in researching and developing new products.

Required Education/Experience:
Applicants must have good "hands-on" knowledge of the printed circuit board (PCB) industry and the liquid photo imageable (LPI) solder mask process. Candidates must be self-motivated, capable of managing key accounts and developing new business opportunities that generate new sales.

- College degree preferred with solid knowledge of chemistry
- 3-5 years of work experience in a technical role within the PCB industry
- 3-5 years of work experience in a sales role
- Computer knowledge, Microsoft Office environment
- Good interpersonal relationship skills
- Good English verbal and written skills are necessary

Working Conditions:
Occasional weekend or overtime work. Travel may be 25-50% or greater.

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INDIUM CORPORATION®

Multiple Positions Available

The Indium Corporation believes that materials science changes the world. As leaders in the electronics assembly industry we are seeking thought leaders that are well-qualified to join our dynamic global team.

Indium Corporation offers a diverse range of career opportunities, including:

- Maintenance and skilled trades
- Engineering
- Marketing and sales
- Finance and accounting
- Machine operators and production
- Research and development
- Operations

For full job description and other immediate openings in a number of departments:

www.indium.com/jobs

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Career Opportunities

THERMAL SYSTEMS

Service Engineer Reflow Soldering Systems (m/f)

To strengthen our service team at Rehm Thermal Systems LLC. in Roswell, Georgia, we are seeking candidates to fill the position of Service Engineer—Reflow Soldering Systems.

Your area of responsibility:

- Installation of Rehm reflow soldering systems at the customers' site
- Maintenance and repair work as well as technical service for our customers in the USA and Mexico
- Execution of machine training

Your profile:

- Completed education studies as an engineer in the field of electrical engineering/mechatronics or comparable education (m/f)
- Basic and specialist knowledge in the field of electronics and electrical engineering/mechatronics
- High willingness to travel and have flexible employment
- Service-oriented and like to work independently

We offer:

- Performance-oriented, attractive compensation
- Comprehensive training
- A safe workplace in one successful group of companies
- Self-responsibility and leeway

Please send application documents online to Natalie Werner at n.werner@rehm-group.com.

apply now

Manncorp™

SMT Field Technician
Huntingdon Valley, PA

Manncorp, a leader in the electronics assembly industry, is looking for an additional SMT Field Technician to join our existing East Coast team and install and support our wide array of SMT equipment.

Duties and Responsibilities:

- Manage on-site equipment installation and customer training
- Provide post-installation service and support, including troubleshooting and diagnosing technical problems by phone, email, or on-site visit
- Assist with demonstrations of equipment to potential customers
- Build and maintain positive relationships with customers
- Participate in the ongoing development and improvement of both our machines and the customer experience we offer

Requirements and Qualifications:

- Prior experience with SMT equipment, or equivalent technical degree
- Proven strong mechanical and electrical troubleshooting skills
- Proficiency in reading and verifying electrical, pneumatic, and mechanical schematics/drawings
- Travel and overnight stays
- Ability to arrange and schedule service trips

We Offer:

- Health and dental insurance
- Retirement fund matching
- Continuing training as the industry develops

apply now

Career Opportunities

U.S. CIRCUIT

Sales Representatives (Specific Territories)

Escondido-based printed circuit fabricator U.S. Circuit is looking to hire sales representatives in the following territories:

- Florida
- Denver
- Washington
- Los Angeles

Experience:

- Candidates must have previous PCB sales experience.

Compensation:

- 7% commission

Contact Mike Fariba for more information.

mfariba@uscircuit.com

apply now

ELECTROLUBE

THE SOLUTIONS PEOPLE

We Are Recruiting!

A fantastic opportunity has arisen within Electrolube, a progressive global electro-chemicals manufacturer. This prestigious new role is for a sales development manager with a strong technical sales background (electro-chemicals industry desirable) and great commercial awareness. The key focus of this role is to increase profitable sales of the Electrolube brand within the Midwest area of the United States; this is to be achieved via a strategic program of major account development and progression of new accounts/projects. Monitoring of competitor activity and recognition of new opportunities are also integral to this challenging role. Full product training to be provided.

The successful candidate will benefit from a generous package and report directly to the U.S. general manager.

Applicants should apply with their CV to melanie.latham@hkw.co.uk (agencies welcome)

apply now

Career Opportunities

ZENTECH

Zentech Manufacturing: Hiring Multiple Positions

Are you looking to excel in your career and grow professionally in a thriving business? Zentech, established in Baltimore, Maryland, in 1998, has proven to be one of the premier electronics contract manufacturers in the U.S.

Zentech is rapidly growing and seeking to add Manufacturing Engineers, Program Managers, and Sr. Test Technicians. Offering an excellent benefit package including health/dental insurance and an employer-matched 401k program, Zentech holds the ultimate set of certifications relating to the manufacture of mission-critical printed circuit card assemblies, including: ISO:9001, AS9100, DD2345, and ISO 13485.

Zentech is an IPC Trusted Source QML and ITAR registered. U.S. citizens only need apply.

Please email resume below.

apply now

BLACKFOX
Premier Training & Certification

IPC Master Instructor

This position is responsible for IPC and skill-based instruction and certification at the training center as well as training events as assigned by company's sales/operations VP. This position may be part-time, full-time, and/or an independent contractor, depending upon the demand and the individual's situation. Must have the ability to work with little or no supervision and make appropriate and professional decisions. Candidate must have the ability to collaborate with the client managers to continually enhance the training program. Position is responsible for validating the program value and its overall success. Candidate will be trained/certified and recognized by IPC as a Master Instructor. Position requires the input and management of the training records. Will require some travel to client's facilities and other training centers.

For more information, click below.

apply now

Events Calendar

World Maker Faire New York ▶
September 21–22, 2019
Corona, Queens, New York, USA

SMTA International 2019 ▶
September 22–26, 2019
Rosemont, Illinois, USA

productronica and electronica India 2019 ▶
September 25–27, 2019
Delhi NCR, India

52nd International Symposium on Microelectronics ▶
September 29–October 3, 2019
Boston, Massachusetts, USA

Altium Live—San Diego ▶
October 9–11, 2019
San Diego, California, USA

Altium Live—Frankfurt ▶
October 21–23, 2019
Frankfurt, Germany

productronica 2019 ▶
November 12–15, 2019
Munich, Germany

PCB Carolina ▶
November 13, 2019
Raleigh, North Carolina, USA

Additional Event Calendars

Coming Soon to *DesignOO7 Magazine*

October: The Landscape of the Design Industry
In this issue, we provide a snapshot of the current PCB design industry, and we look into some of the drivers in this constantly evolving segment.

November: Voices of the Industry
Sometimes, the best view into an industry or a community is through individual voices. In this issue, we talk to members of our business community, gathering and sharing their voices and perspectives.

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